**EXPERIMENT NO**

**VERIFICATION OF** **LATCH** **AND** **FLIP** **FLOP** **OPERATION** **USING** **GATES** **AND** **FLIP** **FLOP’S** **IC**

**APPARATUS** **/** **COMPONENTS**

Digital Logic Trainer.

IC 7402, 7400 , 7404 , 7410 , 7474 & 7475

**Relevant** **Theory** **Topics**: Synchronous Sequential Logic, Latches/Flip-flops Refer Chapter 05 Digital design, 4𝑡ℎ Edition by Morris Mano)

**OBJECTIVE**

To learn about various types of Latches and Flip-Flops

**THEORY**

1. A Flip Flop is a logic circuit that has two stable states Low or High. Enable input signal may be used to enable or disable a flip flop. Clock signal is used to synchronize operations of flip-flops. Most (if not all) of thesystemoutputcanchange state only when the clock makes a transition.
2. Latches are a form of Flip Flop, which do not require clock pulse to latch or hold data present at its input.



**TASK** **1:** **SR** **(or** **RS** **or** **SC)** **Latch**

The SR is the simplest form of Flip Flop or Latch. It can be constructed from NOR gates or NAND gates. Standard logic symbol of SR flip flop and its truth table is given below:-

**NOR** **Gate** **SR** **Latch**:

**PROCEDURE**

Wire the circuit as per figure above and verify the result.

**NOTE:** NAND Gate SR Latch has active low input, hence its truth table is different from the standard i.e a **low** at the set terminal will set the latch.

**TASK** **2:** **GATED** **FLIP** **FLOPS** **Gated** **SR** **Flip** **Flop** **:**

Works only when Enable is High.

**PROCEDURE**

Wire the circuit as per figure above and verify the result.

**GATED** **D** **–** **FLIP** **FLOP**



**PROCEDURE**

Wire the circuit as per figure above and verify the result.

**GATED** **J-K** **FLIP** **FLOP**



**PROCEDURE**

Wire the circuit as per figure above and verify the result

**TASK** **3:** **D-LATCH** **AND** **D-FLIP** **FLOP** **OPERATIONS**



**PROCEDURE**

1. Wire the circuit as per figure 1 & 2 above

2. Connect +5V to Vcc and Ground to pin GND of the ICs.

**VERIFICATION** **–** **D** **LATCH:**

1. Verify that the data at the input terminal is reflected at the output only when Enable (EN) input is high.

2. Verify that for the duration that the Enable

input remains high, all changes in the data input are reflected at the output.

**VERIFICATION** **–** **D** **FLIP** **FLOP:**

1. Verify that the data at the input terminal is

reflected at the output only during Positive going edge of the Clock pulse.

2. Verify that the duration of the Clock pulse has nothing

 to do with data transfer in case of Flip Flop.

LAB ASSIGNMENT

P1. Construct SR latch using NAND gates

P2.What changes would you make in the NAND gate latch shown above, so it behaves exactly like a NOR gate S-R latch.

**ANS.**

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