**EXPERIMENT NO**

**IMPLEMENTATION OF MULTIPLEXER** **AND** **DEMULTIPLEXER** **USING** **IC74151&** **IC74138**

**COMPONENTS**

1. Digital Logic Trainer 2. IC 74151 & 74138

**RELEVANT** **THEORY** **TOPICS**

Combinational logic Decoders, Encoders Multiplexer, De-Multiplexers (Refer Chapter 4.9-4.11 Digital design, 4𝑡ℎ Edition by Morris Mano)

**OBJECTIVE**

To study Multiplexer and Demultiplexer.

**THEORY**

**MULTIPLEXER**

1. The multiplexer circuit is used to place two or more digital signals (from two or more sources) onto a single line, by placingthemthere at different time interval technically it is known as time-division- multiplexing).

2. The multiplexer (also known as data selector) will select data from several transmission lines to be gated to the single output transmission line.

3. The multiplexer will have a number of control inputs that are used to select the appropriate data channel for input.

4. The number of data inputs is equal to 2n where n is the number of control selecting leads.

5. A multiplexer can be used to convert parallel data to serial data.



**DEMULTIPLEXER**

1. A demultiplexer (data distributor) will receive information from a single line

and selectively transmits it to several output lines/channels (one at a time).

2. Demultiplexer has several control select lines which are used to determine (or select) the output transmission path.

3. The number of data output lines is **2n**, where N is the number of control select leads.

4. Demultiplexers are used to convert serial data to parallel data.

**TASK** **1:** **MULTIPLEXER**

IC 74151 is a 8-to-1-Line Multiplexer. It has following features:-

1. 8 Data Inputs (DO-D7).

2. Three Select Inputs (A,B,C). 3. An Enable (or Strobe) G

4. A one bit output Y (and its complement W)



**PROCEDURE**

1. Wire the circuit as per figure above.

2. Connect “Clock Input” (very low frequency) to Input pins of the IC (D0 – D1) and see if the Output LED is pulsating. Confirm your finding on the truth table.

Functional block diagram of IC 74151 is attached.

Connection diagram and Truth table is shown below:

|  |  |  |  |
| --- | --- | --- | --- |
| **Select** | **Strobe** | **Output** | **Output** |
| **C** | **B** | **A** | **G** (or S) | **Y** | **Observed** |
| 0 | 0 | 0 | 0 | Output **Y** is linked with input present at **D0** |  |
| 0 | 0 | 1 | 0 | Output **Y** is linked with input present at **D1** |  |
| 0 | 1 | 0 | 0 | Output **Y** is linked with input present at **D2** |  |
| 0 | 1 | 1 | 0 | Output **Y** is linked with input present at **D3** |  |
| 1 | 0 | 0 | 0 | Output **Y** is linked with input present at **D4** |  |
| 1 | 0 | 1 | 0 | Output **Y** is linked with input present at **D5** |  |
| 1 | 1 | 0 | 0 | Output **Y** is linked with input present at **D6** |  |
| 1 | 1 | 1 | 0 | Output **Y** is linked with input present at **D7** |  |

**TASK 2: DEMULTIPLEX**

A 1-Line-to-8-Line demultiplexer distributes one input to 8 output lines. IC 74138 which was used as a decoder in the last experiment will be used here as Demultiplexer. The only difference between the previous circuit and present circuit will be addition of an INPUT (through Enable AND gate) to the 4th pin of all the 8 NAND gates. The A, B and C inputs will serve as SELECT input (to select a particular output line).

Note that the Enable Inputs of IC 74138 was not used during decoder operation. We will now use **G2B** pin of the IC for **Data/Signal** **Input**. We therefore need to keep pins G1 as high and G2A as low, so that the Input Data/Signal remains present at output of Enable gate and consequently on the 4th input pin of all the 8 NAND gates.

Connection diagram and Truth table of the IC 74138 when used as demultiplexer is shown below. Clock signal (very low frequency) has been used as Input (so that blinking of the LEDs can be observed):



Note: Output of the IC 74138 is active low, so the output line having a Zero in the Truth Table will be selected

|  |  |
| --- | --- |
| **Input** | **Output** |
| **C** | **B** | **A** | **O7** | **O6** | **O5** | **O4** | **O3** | **O2** | **O1** | **O0** |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

**TASK** **3:** **DATA** **COMMUNICATION** **USING** **MULTIPLEXER** **&** **DEMULTIPLEXER.**

Multiplexer IC 74151 and Demultiplexer IC 74138 have been utilized to demonstrate single-line data communication. The 3-bit select code will determine which data input will be steered to the **Y** output of the Demultiplexer.

|  |  |  |  |
| --- | --- | --- | --- |
| Select | Applied Signal at Data Input Pin | Observed Signal Out at Output Pin | When Clock Signal is Applied At All of D Pins of MUX |
| **C** | **B** | **A** | **D** | **Y** | **Observed** **Output** **at** **Pin** **of** **DEMUX** |
| 0 | 0 | 0 | **D0** | **Y0** |  |
| 0 | 0 | 1 | **D1** | **Y1** |  |
| 0 | 1 | 0 | **D2** | **Y2** |  |
| 0 | 1 | 1 | **D3** | **Y3** |  |
| 1 | 0 | 0 | **D4** | **Y4** |  |
| 1 | 0 | 1 | **D5** | **Y5** |  |
| 1 | 1 | 0 | **D6** | **Y6** |  |
| 1 | 1 | 1 | **D7** | **Y7** |  |

**PROCEDURE**

1. Wire the circuit as per figure above and verify result first by giving clock signal to One Input pin at a time of the IC (D0 – D1) and then to all the pins simultaneously.