# EXPERIMENT NO

**CONSTRUCTION OF NOT GATE USING TRANSISTOR**

**OBJECTIVES**

* To understand the construction of NOT gate using transistorlogic
* Verify the truth tables of NOT gate

**INTRODUCTION**

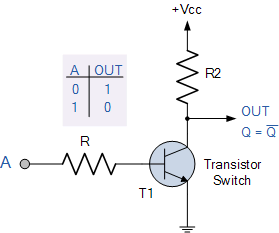
Inverting NOT gates are single input devices which have an output level that is normally at logic level “1” and goes “LOW” to a logic level “0” when its single input is at logic level “1”, in other words it “inverts” (complements) its input signal. The output from a NOT gate only returns “HIGH” again when its input is at logic level “0” giving us the Boolean expression of:  A = Q.

Then we can define the operation of a single input digital logic NOT gate as being:

“If A is NOT true, then Q is true”

**TRANSISTOR NOT GATE**

A simple 2-input logic NOT gate can be constructed using a RTL Resistor-transistor switches as shown below with the input connected directly to the transistor base. The transistor must be saturated “ON” for an inverted output “OFF” at Q.



Logic NOT Gates are available using digital circuits to produce the desired logical function. The standard NOT gate is given a symbol whose shape is of a triangle pointing to the right with a circle at its end. This circle is known as an “inversion bubble” and is used in NOT, NAND and NOR symbols at their output to represent the logical operation of the NOT function. This bubble denotes a signal inversion (complementation) of the signal and can be present on either or both the output and/or the input terminals.

**THE LOGIC NOT GATE TRUTH TABLE**

|  |  |  |
| --- | --- | --- |
| Symbol | Truth Table | |
| Inverter or NOT Gate | A | Q |
| 0 | 1 |
| 1 | 0 |
| Boolean Expression **Q = not A** | Read as inverse of **A** gives Q | |

Logic NOT gates provide the complement of their input signal and are so called because when their input signal is “HIGH” their output state will NOT be “HIGH”. Likewise, when their input signal is “LOW” their output state will NOT be “LOW”. As they are single input devices, logic NOT gates are not normally classed as “decision” making devices or even as a gate, such as the AND or OR gates which have two or more logic inputs. Commercial available NOT gates IC’s are available in either 4 or 6 individual gates within a single IC package.

The “bubble” (o) present at the end of the NOT gate symbol above denotes a signal inversion (complementation) of the output signal. But this bubble can also be present at the gates input to indicate an active-LOW input. This inversion of the input signal is not restricted to the NOT gate only but can be used on any digital circuit or gate as shown with the operation of inversion being exactly the same whether on the input or output terminal. The easiest way is to think of the bubble as simply an inverter.

**PRECAUTIONS**

* Check the power supply for correct voltage.
* Check all the wire connections and remove any possible breaks.
* Check the IC under test using truth table.