# 5 BJT AC Analysis

## CHAPTER OBJECTIVES

- Become familiar with the $r_e$, hybrid, and hybrid $\pi$ models for the BJT transistor.
- Learn to use the equivalent model to find the important ac parameters for an amplifier.
- Understand the effects of a source resistance and load resistor on the overall gain and characteristics of an amplifier.
- Become aware of the general ac characteristics of a variety of important BJT configurations.
- Begin to understand the advantages associated with the two-port systems approach to single- and multistage amplifiers.
- Develop some skill in troubleshooting ac amplifier networks.

## 5.1 INTRODUCTION

The basic construction, appearance, and characteristics of the transistor were introduced in Chapter 3. The dc biasing of the device was then examined in detail in Chapter 4. We now begin to examine the ac response of the BJT amplifier by reviewing the *models* most frequently used to represent the transistor in the sinusoidal ac domain.

One of our first concerns in the sinusoidal ac analysis of transistor networks is the magnitude of the input signal. It will determine whether *small-signal* or *large-signal* techniques should be applied. There is no set dividing line between the two, but the application—and the magnitude of the variables of interest relative to the scales of the device characteristics—will usually make it quite clear which method is appropriate. The small-signal technique is introduced in this chapter, and large-signal applications are examined in Chapter 12.

There are three models commonly used in the small-signal ac analysis of transistor networks: the $r_e$ model, the hybrid $\pi$ model, and the hybrid equivalent model. This chapter introduces all three but emphasizes the $r_e$ model.

## 5.2 AMPLIFICATION IN THE AC DOMAIN

It was demonstrated in Chapter 3 that the transistor can be employed as an amplifying device. That is, the output sinusoidal signal is greater than the input sinusoidal signal, or, stated another way, the output ac power is greater than the input ac power. The question then arises as to how the ac power output can be greater than the input ac power. Conservation of energy dictates that over time the total power output, $P_o$, of a system cannot be greater than its power

input, $P_i$, and that the efficiency defined by $\eta = P_o/P_i$ cannot be greater than 1. The factor missing from the discussion above that permits an ac power output greater than the input ac power is the applied dc power. It is the principal contributor to the total output power even though part of it is dissipated by the device and resistive elements. In other words, there is an "exchange" of dc power to the ac domain that permits establishing a higher output ac power. In fact, a *conversion efficiency* is defined by $\eta = P_{o(\text{ac})}/P_{i(\text{dc})}$, where $P_{o(\text{ac})}$ is the ac power to the load and $P_{i(\text{dc})}$ is the dc power supplied.

Perhaps the role of the dc supply can best be described by first considering the simple dc network of Fig. 5.1. The resulting direction of flow is indicated in the figure with a plot of the current $i$ versus time. Let us now insert a control mechanism such as that shown in Fig. 5.2. The control mechanism is such that the application of a relatively small signal to the control mechanism can result in a substantial oscillation in the output circuit.

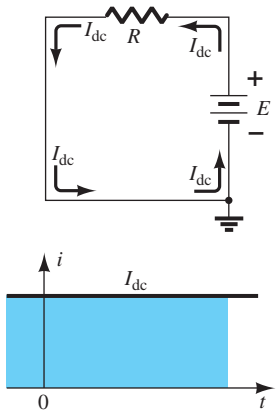



**FIG. 5.1**
*Steady current established by a dc supply.*

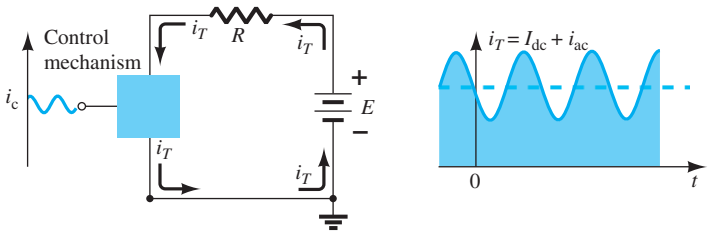



**FIG. 5.2**
*Effect of a control element on the steady-state flow of the electrical system of Fig. 5.1.*

That is, for this example,

$$i_{\text{ac(p-p)}} \gg i_{c\text{(p-p)}}$$

and amplification in the ac domain has been established. The peak-to-peak value of the output current far exceeds that of the control current.

For the system of Fig. 5.2, the peak value of the oscillation in the output circuit is controlled by the established dc level. Any attempt to exceed the limit set by the dc level will result in a "clipping" (flattening) of the peak region at the high and low end of the output signal. In general, therefore, proper amplification design requires that the dc and ac components be sensitive to each other's requirements and limitations.

However, it is extremely helpful to realize that:

***The superposition theorem is applicable for the analysis and design of the dc and ac components of a BJT network, permitting the separation of the analysis of the dc and ac responses of the system.***

In other words, one can make a complete dc analysis of a system before considering the ac response. Once the dc analysis is complete, the ac response can be determined using a completely ac analysis. It happens, however, that one of the components appearing in the ac analysis of BJT networks will be determined by the dc conditions, so there is still an important link between the two types of analysis.

## 5.3 BJT TRANSISTOR MODELING

The key to transistor small-signal analysis is the use of the equivalent circuits (models) to be introduced in this chapter.

***A model is a combination of circuit elements, properly chosen, that best approximates the actual behavior of a semiconductor device under specific operating conditions.***

Once the ac equivalent circuit is determined, the schematic symbol for the device can be replaced by this equivalent circuit and the basic methods of circuit analysis applied to determine the desired quantities of the network.

In the formative years of transistor network analysis the *hybrid equivalent network* was employed the most frequently. Specification sheets included the parameters in their listing, and analysis was simply a matter of inserting the equivalent circuit with the listed values.

The drawback to using this equivalent circuit, however, is that it is *defined for a set of operating conditions that might not match the actual operating conditions.* In most cases, this is not a serious flaw because the actual operating conditions are relatively close to the chosen operating conditions on the data sheets. In addition, there is always a variation in actual resistor values and given transistor beta values, so as an approximate approach it was quite reliable. Manufacturers continue to specify the hybrid parameter values for a particular operating point on their specification sheets. They really have no choice. They want to give the user some idea of the value of each important parameter so comparisons can be made between transistors, but they really do not know the user's actual operating conditions.

In time the use of the $r_e$ *model* became the more desirable approach because an important parameter of the equivalent circuit was determined by the actual operating conditions rather than using a data sheet value that in some cases could be quite different. Unfortunately, however, one must still turn to the data sheets for some of the other parameters of the equivalent circuit. The $r_e$ model also failed to include a feedback term, which in some cases can be important if not simply troublesome.

The $r_e$ model is really a reduced version of the *hybrid* $\pi$ *model* used almost exclusively for high-frequency analysis. This model also includes a connection between output and input to include the feedback effect of the output voltage and the input quantities. The full hybrid model is introduced in Chapter 9.

Throughout the text the $r_e$ model is the model of choice unless the discussion centers on the description of each model or a region of examination that predetermines the model that should be used. Whenever possible, however, a comparison between models will be discussed to show how closely related they really are. It is also important that once you gain a proficiency with one model it will carry over to an investigation using a different model, so moving from one to another will not be a dramatic undertaking.

In an effort to demonstrate the effect that the ac equivalent circuit will have on the analysis to follow, consider the circuit of Fig. 5.3. Let us assume for the moment that the small-signal ac equivalent circuit for the transistor has already been determined. Because we are interested only in the ac response of the circuit, all the dc supplies can be replaced by a zero-potential equivalent (short circuit) because they determine only the dc (quiescent level) of the output voltage and not the magnitude of the swing of the ac output. This is clearly demonstrated by Fig. 5.4. The dc levels were simply important for determining the proper *Q*-point of operation. Once determined, the dc levels can be ignored in the ac analysis of the network. In addition, the coupling capacitors $C_1$ and $C_2$ and bypass capacitor $C_3$ were chosen to have a very small reactance at the frequency of application. Therefore, they, too, may for all practical purposes be replaced by a low-resistance path or a short circuit. Note that this will result in the "shorting out" of the dc biasing resistor $R_E$. Recall that capacitors assume an "open-circuit" equivalent under dc steady-state conditions, permitting an isolation between stages for the dc levels and quiescent conditions.

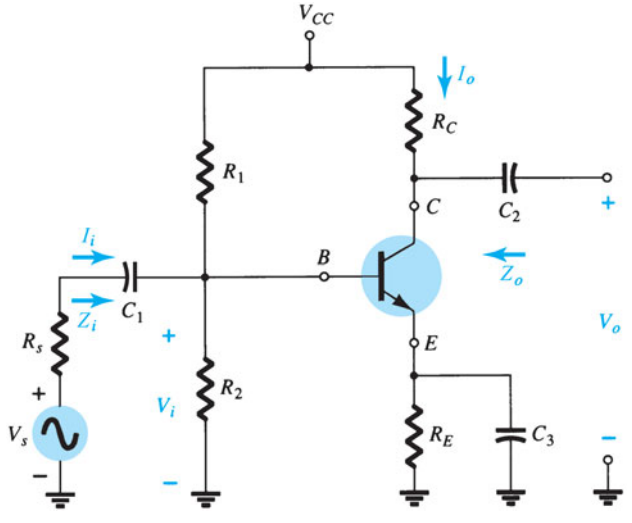



**FIG. 5.3**

*Transistor circuit under examination in this introductory discussion.*

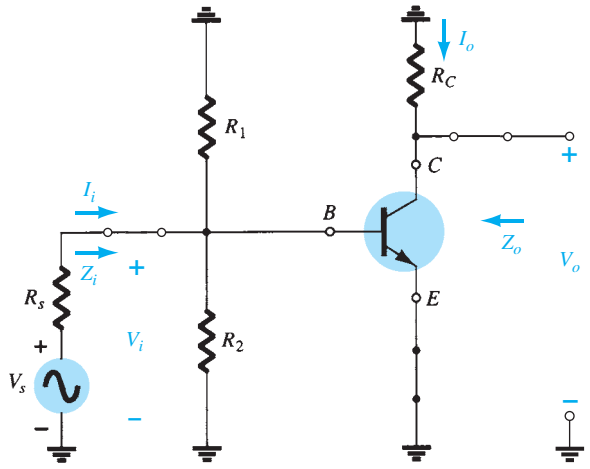



**FIG. 5.4**
*The network of Fig. 5.3 following removal of the dc supply and insertion of the short-circuit equivalent for the capacitors.*

It is important as you progress through the modifications of the network to define the ac equivalent that the parameters of interest such as $Z_i$, $Z_o$, $I_i$, and $I_o$ as defined by Fig. 5.5 be carried through properly. Even though the network appearance may change, you want to be sure the quantities you find in the reduced network are the same as defined by the original network. In both networks the input impedance is defined from base to ground, the input current as the base current of the transistor, the output voltage as the voltage from collector to ground, and the output current as the current through the load resistor $R_C$.

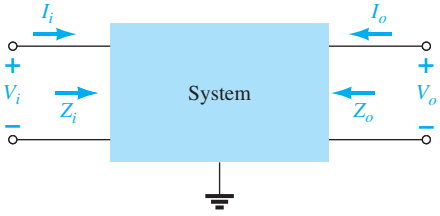



**FIG. 5.5**
*Defining the important parameters of any system.*

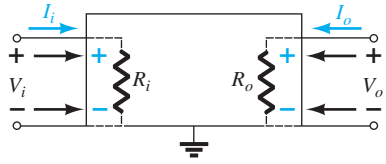



**FIG. 5.6**
*Demonstrating the reason for the defined directions and polarities.*

The parameters of Fig. 5.5 can be applied to any system whether it has one or a thousand components. For all the analysis to follow in this text, the directions of the currents, the polarities of the voltages, and the direction of interest for the impedance levels are as appearing in Fig. 5.5. In other words, the input current $I_i$ and output current $I_o$ are, by definition, defined to enter the system. If, in a particular example, the output current is leaving the system rather than entering the system as shown in Fig. 5.5, a minus sign must be applied. The defined polarities for the input and output voltages are also as appearing in Fig. 5.5. If $V_o$ has the opposite polarity, the minus sign must be applied. Note that $Z_i$ is the impedance "looking into" the system, whereas $Z_o$ is the impedance "looking back into" the system from the output side. By choosing the defined directions for the currents and voltages as appearing in Fig. 5.5, both the input impedance and output impedance are defined as having positive values. For example, in Fig. 5.6 the input and output impedances for a particular system are both resistive. For the direction of $I_i$ and $I_o$ the resulting voltage across the resistive elements will have the same polarity as $V_i$ and $V_o$, respectively. If $I_o$ had been defined as the opposite direction in Fig. 5.5 a minus sign would have to be applied. For each case $Z_i = V_i/I_i$ and $Z_o = V_o/I_o$ with positive results if they all have the defined directions and polarity of Fig. 5.5. If the output current of an actual system has a direction opposite to that

of Fig. 5.5 a minus sign must be applied to the result because $V_o$ must be defined as appearing in Fig. 5.5. Keep Fig. 5.5 in mind as you analyze the BJT networks in this chapter. It is an important introduction to "System Analysis," which is becoming so important with the expanded use of packaged IC systems.

If we establish a common ground and rearrange the elements of Fig. 5.4, $R_1$ and $R_2$ will be in parallel, and $R_C$ will appear from collector to emitter as shown in Fig. 5.7. Because the components of the transistor equivalent circuit appearing in Fig. 5.7 employ familiar components such as resistors and independent controlled sources, analysis techniques such as superposition, Thévenin's theorem, and so on, can be applied to determine the desired quantities.

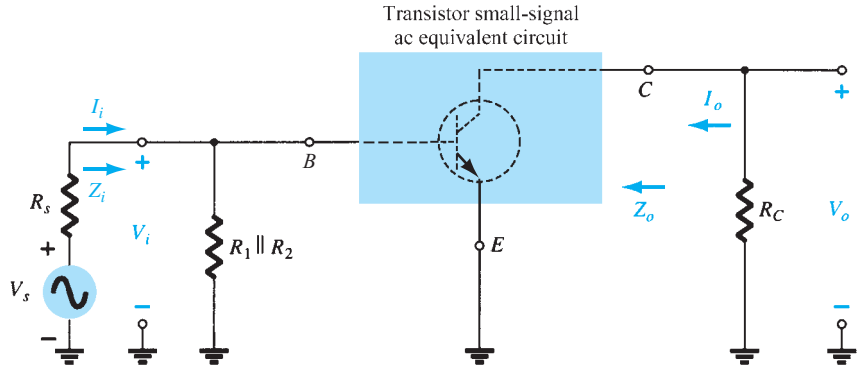



**FIG. 5.7**
*Circuit of Fig. 5.4 redrawn for small-signal ac analysis.*

Let us further examine Fig. 5.7 and identify the important quantities to be determined for the system. Because we know that the transistor is an amplifying device, we would expect some indication of how the output voltage $V_o$ is related to the input voltage $V_i$—the *voltage gain.* Note in Fig. 5.7 for this configuration that the *current gain* is defined by $A_i = I_o/I_i$.

In summary, therefore, the ac equivalent of a transistor network is obtained by:

1. ***Setting all dc sources to zero and replacing them by a short-circuit equivalent***
2. ***Replacing all capacitors by a short-circuit equivalent***
3. ***Removing all elements bypassed by the short-circuit equivalents introduced by steps 1 and 2***
4. ***Redrawing the network in a more convenient and logical form***

In the sections to follow, a transistor equivalent model will be introduced to complete the ac analysis of the network of Fig. 5.7.

## 5.4 THE $r_e$ TRANSISTOR MODEL

The $r_e$ model for the CE, CB, and CC BJT transistor configurations will now be introduced with a short description of why each is a good approximation to the actual behavior of a BJT transistor.

### Common-Emitter Configuration

The equivalent circuit for the common-emitter configuration will be constructed using the device characteristics and a number of approximations. Starting with the input side, we find the applied voltage $V_i$ is equal to the voltage $V_{be}$ with the input current being the base current $I_b$ as shown in Fig. 5.8.

Recall from Chapter 3 that because the current through the forward-biased junction of the transistor is $I_E$, the characteristics for the input side appear as shown in Fig. 5.9a for various levels of $V_{BE}$. Taking the average value for the curves of Fig. 5.9a will result in the single curve of Fig. 5.9b, which is simply that of a forward-biased diode.

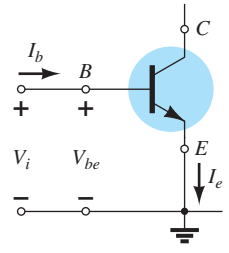



**FIG. 5.8**
*Finding the input equivalent circuit for a BJT transistor.*

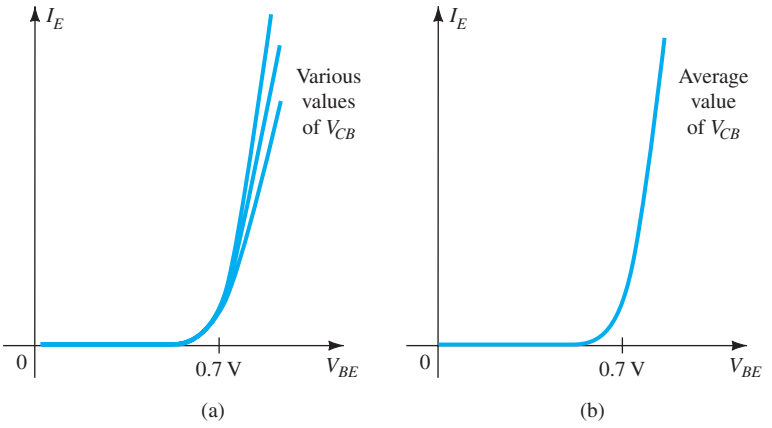



**FIG. 5.9**
*Defining the average curve for the characteristics of Fig. 5.9a.*

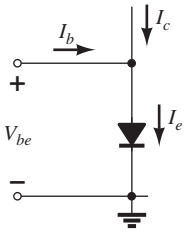



**FIG. 5.10**
*Equivalent circuit for the input side of a BJT transistor.*

For the equivalent circuit, therefore, the input side is simply a single diode with a current $I_e$, as shown in Fig. 5.10. However, we must now add a component to the network that will establish the current $I_e$ of Fig. 5.10 using the output characteristics.

If we redraw the collector characteristics to have a constant $\beta$ as shown in Fig. 5.11 (another approximation), the entire characteristics at the output section can be replaced by a controlled source whose magnitude is beta times the base current as shown in Fig. 5.11. Because all the input and output parameters of the original configuration are now present, the equivalent network for the common-emitter configuration has been established in Fig. 5.12.

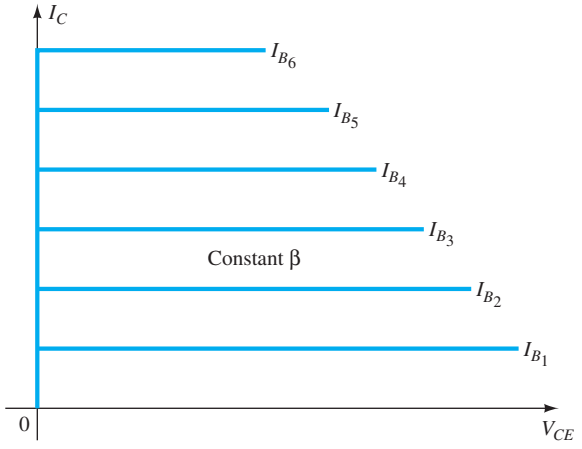



**FIG. 5.11**
*Constant β characteristics.*

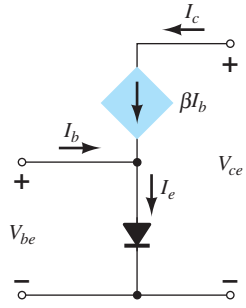



**FIG. 5.12**
*BJT equivalent circuit.*

The equivalent model of Fig. 5.12 can be awkward to work with due to the direct connection between input and output networks. It can be improved by first replacing the diode by its equivalent resistance as determined by the level of $I_E$, as shown in Fig. 5.13. Recall from Section 1.8 that the diode resistance is determined by $r_D = 26\text{ mV}/I_D$. Using the subscript $e$ because the determining current is the emitter current will result in $r_e = 26\text{ mV}/I_E$.

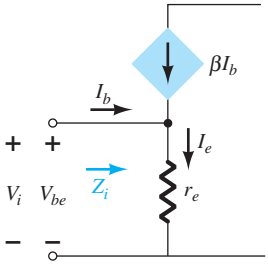



**FIG. 5.13**
*Defining the level of $Z_i$.*

Now, for the input side:
$$Z_i = \frac{V_i}{I_b} = \frac{V_{be}}{I_b}$$

Solving for $V_{be}$:
$$V_{be} = I_e r_e = (I_c + I_b) r_e = (\beta I_b + I_b) r_e$$
$$= (\beta + 1) I_b r_e$$

and
$$Z_i = \frac{V_{be}}{I_b} = \frac{(\beta + 1) I_b r_e}{I_b}$$

$$\boxed{Z_i = (\beta + 1) r_e \cong \beta r_e} \qquad \textbf{(5.1)}$$

The result is that the impedance seen "looking into" the base of the network is a resistor equal to beta times the value of $r_e$, as shown in Fig. 5.14. The collector output current is still linked to the input current by beta as shown in the same figure.

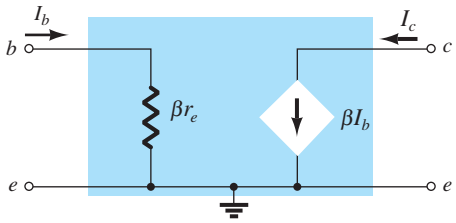



**FIG. 5.14**
*Improved BJT equivalent circuit.*

The equivalent circuit has therefore been defined for the ideal characteristics of Fig. 5.11, but now the input and output circuits are isolated and only linked by the controlled source—a form much easier to work with when analyzing networks.

## Early Voltage

We now have a good representation for the input circuit, but aside from the collector output current being defined by the level of beta and $I_B$, we do not have a good representation for the output impedance of the device. In reality the characteristics do not have the ideal appearance of Fig. 5.11. Rather, they have a slope as shown In Fig. 5.15 that defines the output impedance of the device. The steeper the slope, the less the output impedance and the less ideal the transistor. In general, it is desirable to have large output impedances to avoid loading down the next stage of a design. If the slope of the curves is extended until they reach the horizontal axis, it is interesting to note in Fig. 5.15 that they will all intersect at a voltage called the Early voltage. This intersection was first discovered by James M. Early in 1952. As the base current increases the slope of the line increases, resulting in an increase in output impedance with increase in base and collector current. For a particular collector and base current as shown in Fig. 5.15, the output impedance can be found using the following equation:

$$r_o = \frac{\Delta V}{\Delta I} = \frac{V_A + V_{CE_Q}}{I_{C_Q}} \tag{5.2}$$

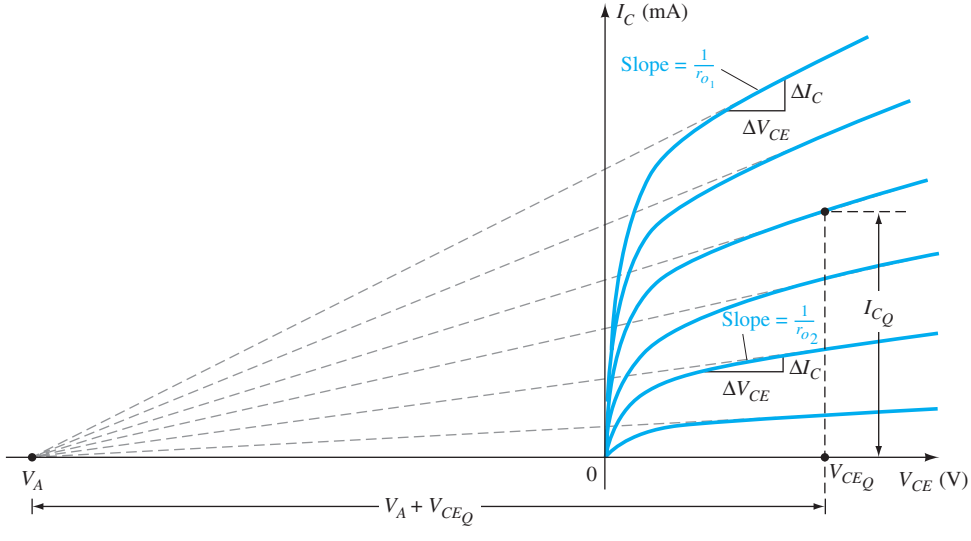



**FIG. 5.15**
*Defining the Early voltage and the output impedance of a transistor.*

Typically, however, the Early voltage is sufficiently large compared with the applied collector-to-emitter voltage to permit the following approximation.

$$r_o \cong \frac{V_A}{I_{C_Q}} \tag{5.3}$$

Clearly, since $V_A$ is a fixed voltage, the larger the collector current, the less the output impedance.

For situations where the Early voltage is not available the output impedance can be found from the characteristics at any base or collector current using the following equation:

$$\text{Slope} = \frac{\Delta y}{\Delta x} = \frac{\Delta I_C}{\Delta V_{CE}} = \frac{1}{r_o}$$

and

$$r_o = \frac{\Delta V_{CE}}{\Delta I_C} \tag{5.4}$$

For the same change in voltage in Fig. 5.15 the resulting change in current $\Delta I_C$ is significantly less for $r_{o_2}$ than $r_{o_1}$, resulting in $r_{o_2}$ being much larger than $r_{o_1}$.

In situations where the specification sheets of a transistor do not include the Early voltage or the output characteristics, the output impedance can be determined from the hybrid parameter $h_{oe}$ that is normally plotted on every specification sheet. It is a quantity that will be described in detail in Section 5.19.

In any event, an output impedance can now be defined that will appear as a resistor in parallel with the output as shown in the equivalent circuit of Fig. 5.16.

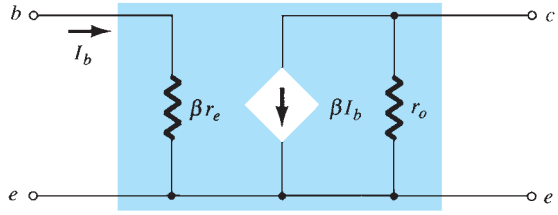



**FIG. 5.16**
*$r_e$ model for the common-emitter transistor configuration including effects of $r_o$.*

The equivalent circuit of Fig. 5.16 will be used throughout the analysis to follow for the common-emitter configuration. Typical values of beta run from 50 to 200, with values of $\beta r_e$ typically running from a few hundred ohms to a maximum of 6 kΩ to 7 kΩ. The output resistance $r$ is typically in the range of 40 kΩ to 50 kΩ.

## Common-Base Configuration

The common-base equivalent circuit will be developed in much the same manner as applied to the common-emitter configuration. The general characteristics of the input and output circuit will generate an equivalent circuit that will approximate the actual behavior of the device. Recall for the common-emitter configuration the use of a diode to represent the connection from base to emitter. For the common-base configuration of Fig. 5.17a the *pnp* transistor employed will present the same possibility at the input circuit. The result is the use of a diode in the equivalent circuit as shown in Fig. 5.17b. For the output circuit, if we return to Chapter 3 and review Fig. 3.8, we find that the collector current is related to the emitter current by alpha $\alpha$. In this case, however, the controlled source defining the collector current as inserted in Fig. 5.17b is opposite in direction to that of the controlled source of the common-emitter configuration. The direction of the collector current in the output circuit is now opposite that of the defined output current.

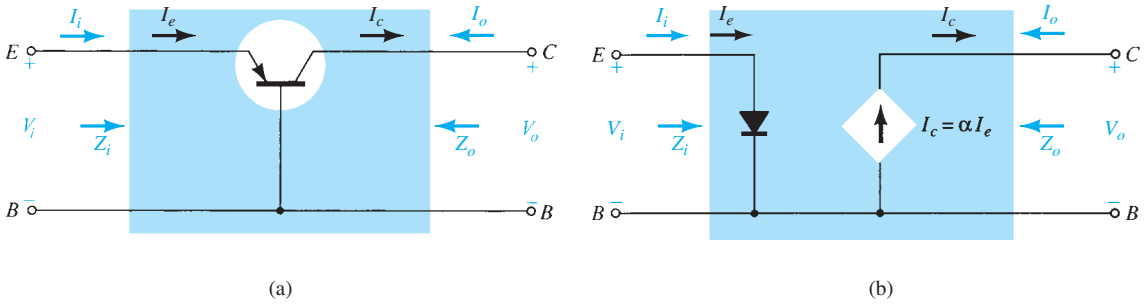



**FIG. 5.17**

*(a) Common-base BJT transistor; (b) equivalent circuit for configuration of (a).*

For the ac response, the diode can be replaced by its equivalent ac resistance determined by $r_e = 26\,\text{mV}/I_E$ as shown in Fig. 5.18. Take note of the fact that the emitter current continues to determine the equivalent resistance. An additional output resistance can be determined from the characteristics of Fig. 5.19 in much the same manner as applied to the common-emitter configuration. The almost horizontal lines clearly reveal that the output resistance $r_o$ as appearing in Fig. 5.18 will be quite high and certainly much higher than that for the typical common-emitter configuration.

The network of Fig. 5.18 is therefore an excellent equivalent circuit for the analysis of most common-base configurations. It is similar in many ways to that of the common-emitter configuration. In general, common-base configurations have very low input impedance because it is essentially simply $r_e$. Typical values extend from a few ohms to perhaps 50 Ω. The output impedance $r_o$ will typically extend into the megohm range. Because the output current is opposite to the defined $I_o$ direction, you will find in the analysis to follow that there is no phase shift between the input and output voltages. For the common-emitter configuration there is a 180° phase shift.

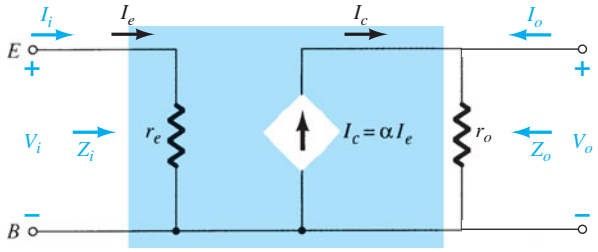



**FIG. 5.18**

*Common base $r_e$ equivalent circuit.*

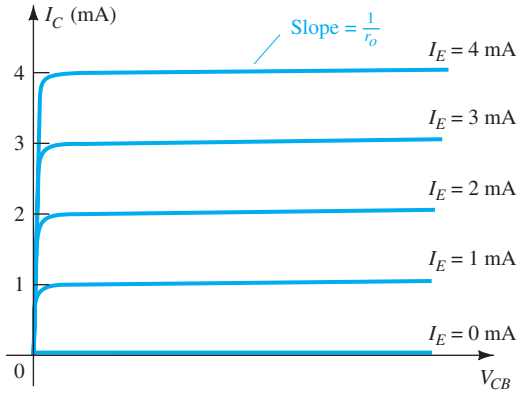



**FIG. 5.19**

*Defining $Z_o$.*

## Common-Collector Configuration

For the common-collector configuration, the model defined for the common-emitter configuration of Fig. 5.16 is normally applied rather than defining a model for the common-collector configuration. In subsequent chapters, a number of common-collector configurations will be investigated, and the effect of using the same model will become quite apparent.

### *npn* versus *pnp*

The dc analysis of *npn* and *pnp* configurations is quite different in the sense that the currents will have opposite directions and the voltages opposite polarities. However, for an ac analysis where the signal will progress between positive and negative values, the ac equivalent circuit will be the same.

## 5.5 COMMON-EMITTER FIXED-BIAS CONFIGURATION

The transistor models just introduced will now be used to perform a small-signal ac analysis of a number of standard transistor network configurations. The networks analyzed represent the majority of those appearing in practice. Modifications of the standard configurations will be relatively easy to examine once the content of this chapter is reviewed and understood. For each configuration, the effect of an output impedance is examined for completeness.

The computer analysis section includes a brief description of the transistor model employed in the PSpice and Multisim software packages. It demonstrates the range and depth of the available computer analysis systems and how relatively easy it is to enter a complex network and print out the desired results. The first configuration to be analyzed in detail is the common-emitter *fixed-bias* network of Fig. 5.20. Note that the input signal $V_i$ is applied to the base of the transistor, whereas the output $V_o$ is off the collector. In addition, recognize that the input current $I_i$ is not the base current, but the source current, and the output current $I_o$ is the collector current. The small-signal ac analysis begins by removing the dc effects of $V_{CC}$ and replacing the dc blocking capacitors $C_1$ and $C_2$ by short-circuit equivalents, resulting in the network of Fig. 5.21.

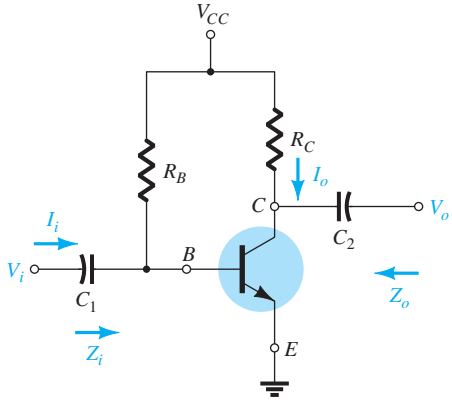



**FIG. 5.20**
*Common-emitter fixed-bias configuration.*

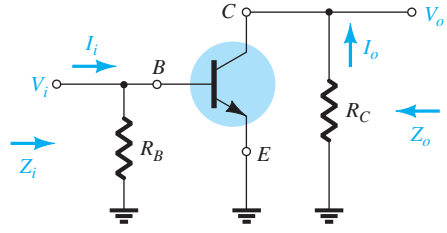



**FIG. 5.21**
*Network of Fig. 5.20 following the removal of the effects of $V_{CC}$, $C_1$, and $C_2$.*

Note in Fig. 5.21 that the common ground of the dc supply and the transistor emitter terminal permits the relocation of $R_B$ and $R_C$ in parallel with the input and output sections of the transistor, respectively. In addition, note the placement of the important network parameters $Z_i$, $Z_o$, $I_i$, and $I_o$ on the redrawn network. Substituting the $r_e$ model for the common-emitter configuration of Fig. 5.21 results in the network of Fig. 5.22.

The next step is to determine $\beta$, $r_e$, and $r_o$. The magnitude of $\beta$ is typically obtained from a specification sheet or by direct measurement using a curve tracer or transistor

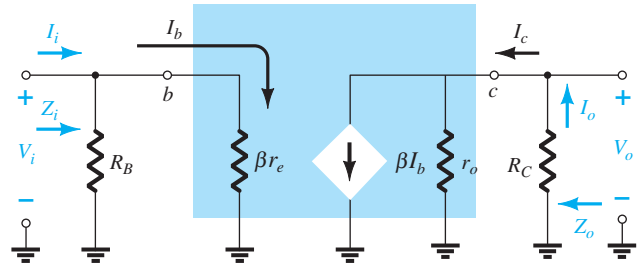



**FIG. 5.22**
*Substituting the $r_e$ model into the network of Fig. 5.21.*

testing instrument. The value of $r_e$ must be determined from a dc analysis of the system, and the magnitude of $r_o$ is typically obtained from the specification sheet or characteristics. Assuming that $\beta$, $r_e$, and $r_o$ have been determined will result in the following equations for the important two-port characteristics of the system.

**$Z_i$** Figure 5.22 clearly shows that

$$Z_i = R_B \| \beta r_e \quad \text{ohms} \tag{5.5}$$

For the majority of situations $R_B$ is greater than $\beta r_e$ by more than a factor of 10 (recall from the analysis of parallel elements that the total resistance of two parallel resistors is always less than the smallest and very close to the smallest if one is much larger than the other), permitting the following approximation:

$$Z_i \cong \beta r_e \quad \text{ohms} \qquad R_B \geq 10\beta r_e \tag{5.6}$$

**$Z_o$** Recall that the output impedance of any system is defined as the impedance $Z_o$ determined when $V_i = 0$. For Fig. 5.22, when $V_i = 0$, $I_i = I_b = 0$, resulting in an open-circuit equivalence for the current source. The result is the configuration of Fig. 5.23. We have

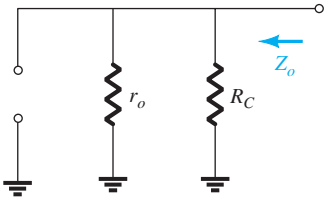



**FIG. 5.23**
*Determining $Z_o$ for the network of Fig. 5.22.*

$$Z_o = R_C \| r_o \quad \text{ohms} \tag{5.7}$$

If $r_o \geq 10R_C$, the approximation $R_C \| r_o \cong R_C$ is frequently applied, and

$$Z_o \cong R_C \qquad r_o \geq 10R_C \tag{5.8}$$

**$A_v$** The resistors $r_o$ and $R_C$ are in parallel, and

$$V_o = -\beta I_b (R_C \| r_o)$$

but

$$I_b = \frac{V_i}{\beta r_e}$$

so that

$$V_o = -\beta \left( \frac{V_i}{\beta r_e} \right) (R_C \| r_o)$$

and

$$A_v = \frac{V_o}{V_i} = -\frac{(R_C \| r_o)}{r_e} \tag{5.9}$$

If $r_o \geq 10R_C$, so that the effect of $r_o$ can be ignored,

$$A_v = -\frac{R_C}{r_e} \qquad r_o \geq 10R_C \tag{5.10}$$

Note the explicit absence of $\beta$ in Eqs. (5.9) and (5.10), although we recognize that $\beta$ must be utilized to determine $r_e$.

**Phase Relationship** The negative sign in the resulting equation for $A_v$ reveals that a 180° phase shift occurs between the input and output signals, as shown in Fig. 5.24. The is a result of the fact that $\beta I_b$ establishes a current through $R_C$ that will result in a voltage across $R_C$, the opposite of that defined by $V_o$.

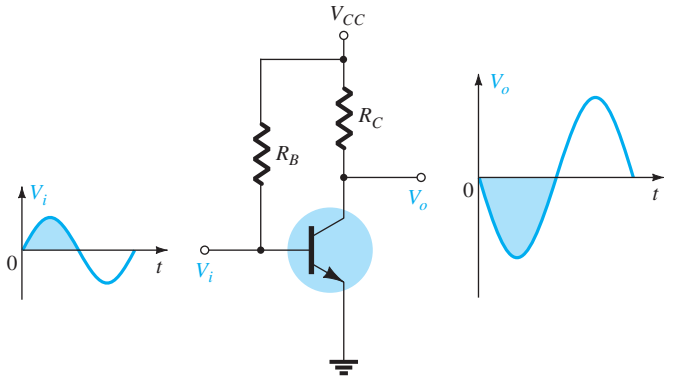



**FIG. 5.24**
*Demonstrating the 180° phase shift between input and output waveforms.*

**EXAMPLE 5.1** For the network of Fig. 5.25:

a. Determine $r_e$.
b. Find $Z_i$ (with $r_o = \infty\,\Omega$).
c. Calculate $Z_o$ (with $r_o = \infty\,\Omega$).
d. Determine $A_v$ (with $r_o = \infty\,\Omega$).
e. Repeat parts (c) and (d) including $r_o = 50\,\text{k}\Omega$ in all calculations and compare results.

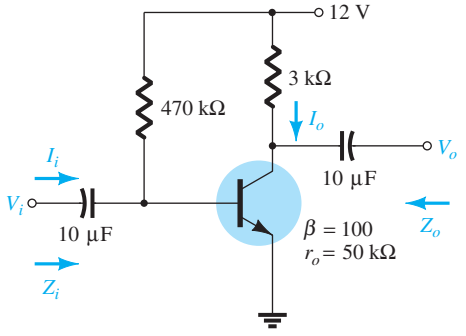



**FIG. 5.25**
*Example 5.1.*

***Solution:***

a. DC analysis:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12\text{ V} - 0.7\text{ V}}{470\,\text{k}\Omega} = 24.04\,\mu\text{A}$$

$$I_E = (\beta + 1)I_B = (101)(24.04\,\mu\text{A}) = 2.428\text{ mA}$$

$$r_e = \frac{26\text{ mV}}{I_E} = \frac{26\text{ mV}}{2.428\text{ mA}} = \mathbf{10.71\ \Omega}$$

b. $\beta r_e = (100)(10.71\ \Omega) = 1.071\,\text{k}\Omega$

$$Z_i = R_B \| \beta r_e = 470\,\text{k}\Omega \| 1.071\,\text{k}\Omega = \mathbf{1.07\,k\Omega}$$

c. $Z_o = R_C = \mathbf{3\,k\Omega}$

d. $$A_v = -\frac{R_C}{r_e} = -\frac{3\,\text{k}\Omega}{10.71\ \Omega} = \mathbf{-280.11}$$

e. $Z_o = r_o \| R_C = 50\,\text{k}\Omega \| 3\,\text{k}\Omega = \mathbf{2.83\,k\Omega}$ vs. $3\,\text{k}\Omega$

$$A_v = -\frac{r_o \| R_C}{r_e} = \frac{2.83\,\text{k}\Omega}{10.71\,\Omega} = \mathbf{-264.24} \text{ vs. } -280.11$$

## 5.6 VOLTAGE-DIVIDER BIAS

The next configuration to be analyzed is the *voltage-divider* bias network of Fig. 5.26. Recall that the name of the configuration is a result of the voltage-divider bias at the input side to determine the dc level of $V_B$.

Substituting the $r_e$ equivalent circuit results in the network of Fig. 5.27. Note the absence of $R_E$ due to the low-impedance shorting effect of the bypass capacitor, $C_E$. That is, at the frequency (or frequencies) of operation, the reactance of the capacitor is so small compared to $R_E$ that it is treated as a short circuit across $R_E$. When $V_{CC}$ is set to zero, it places one end of $R_1$ and $R_C$ at ground potential as shown in Fig. 5.27. In addition, note that $R_1$ and $R_2$ remain part of the input circuit, whereas $R_C$ is part of the output circuit. The parallel combination of $R_1$ and $R_2$ is defined by

$$R' = R_1 \| R_2 = \frac{R_1 R_2}{R_1 + R_2} \tag{5.11}$$

**$Z_i$** From Fig. 5.27

$$Z_i = R' \| \beta r_e \tag{5.12}$$

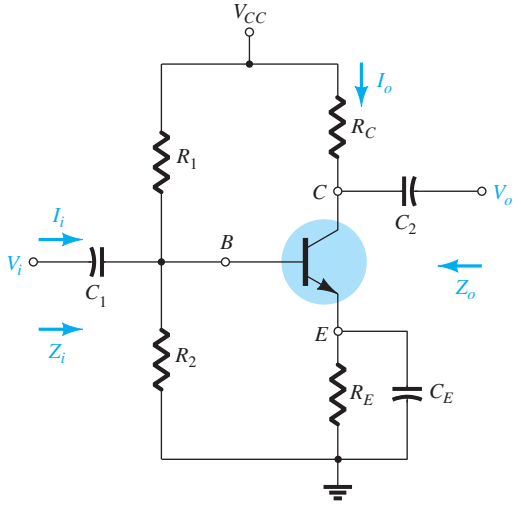



**FIG. 5.26**
*Voltage-divider bias configuration.*

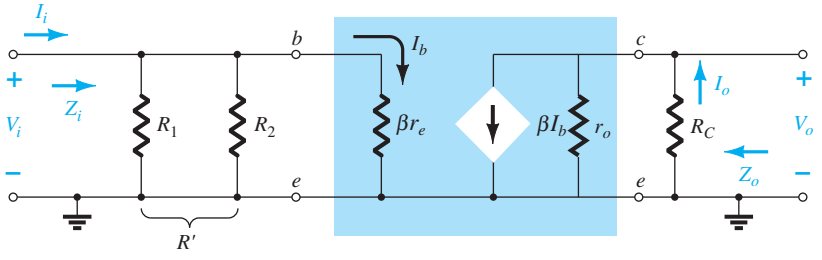



**FIG. 5.27**
*Substituting the $r_e$ equivalent circuit into the ac equivalent network of Fig. 5.26.*

**$Z_o$** From Fig. 5.27 with $V_i$ set to 0 V, resulting in $I_b = 0\ \mu A$ and $\beta I_b = 0$ mA,

$$\boxed{Z_o = R_C \| r_o} \tag{5.13}$$

If $r_o \geq 10R_C$,

$$\boxed{Z_o \cong R_C}_{r_o \geq 10R_C} \tag{5.14}$$

**$A_v$** Because $R_C$ and $r_o$ are in parallel,

$$V_o = -(\beta I_b)(R_C \| r_o)$$

and

$$I_b = \frac{V_i}{\beta r_e}$$

so that

$$V_o = -\beta\left(\frac{V_i}{\beta r_e}\right)(R_C \| r_o)$$

and

$$\boxed{A_v = \frac{V_o}{V_i} = \frac{-R_C \| r_o}{r_e}} \tag{5.15}$$

which you will note is an exact duplicate of the equation obtained for the fixed-bias configuration.

For $r_o \geq 10R_C$,

$$\boxed{A_v = \frac{V_o}{V_i} \cong -\frac{R_C}{r_e}}_{r_o \geq 10R_C} \tag{5.16}$$

**Phase Relationship** The negative sign of Eq. (5.15) reveals a 180° phase shift between $V_o$ and $V_i$.

**EXAMPLE 5.2** For the network of Fig. 5.28, determine:

a. $r_e$.
b. $Z_i$.
c. $Z_o$ ($r_o = \infty\ \Omega$).
d. $A_v$ ($r_o = \infty\ \Omega$).
e. The parameters of parts (b) through (d) if $r_o = 50\ k\Omega$ and compare results.

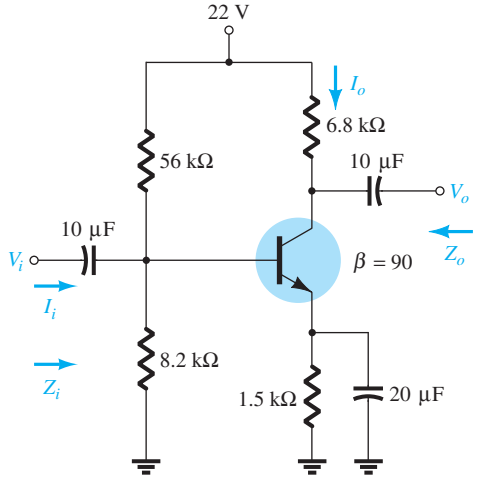



**FIG. 5.28**
*Example 5.2.*

***Solution:***

a. DC: Testing $\beta R_E > 10R_2$,

$$(90)(1.5\ \text{k}\Omega) > 10(8.2\ \text{k}\Omega)$$

$$135\ \text{k}\Omega > 82\ \text{k}\Omega\ (\textit{satisfied})$$

Using the approximate approach, we obtain

$$V_B = \frac{R_2}{R_1 + R_2} V_{CC} = \frac{(8.2\ \text{k}\Omega)(22\ \text{V})}{56\ \text{k}\Omega + 8.2\ \text{k}\Omega} = 2.81\ \text{V}$$

$$V_E = V_B - V_{BE} = 2.81\ \text{V} - 0.7\ \text{V} = 2.11\ \text{V}$$

$$I_E = \frac{V_E}{R_E} = \frac{2.11\ \text{V}}{1.5\ \text{k}\Omega} = 1.41\ \text{mA}$$

$$r_e = \frac{26\ \text{mV}}{I_E} = \frac{26\ \text{mV}}{1.41\ \text{mA}} = \mathbf{18.44\ \Omega}$$

b. $R' = R_1 \| R_2 = (56\ \text{k}\Omega) \| (8.2\ \text{k}\Omega) = 7.15\ \text{k}\Omega$

$Z_i = R' \| \beta r_e = 7.15\ \text{k}\Omega \| (90)(18.44\ \Omega) = 7.15\ \text{k}\Omega \| 1.66\ \text{k}\Omega$

$= \mathbf{1.35\ k\Omega}$

c. $Z_o = R_C = \mathbf{6.8\ k\Omega}$

d. $A_v = -\frac{R_C}{r_e} = -\frac{6.8\ \text{k}\Omega}{18.44\ \Omega} = \mathbf{-368.76}$

e. $Z_i = \mathbf{1.35\ k\Omega}$

$Z_o = R_C \| r_o = 6.8\ \text{k}\Omega \| 50\ \text{k}\Omega = \mathbf{5.98\ k\Omega}$ vs. $6.8\ \text{k}\Omega$

$A_v = -\frac{R_C \| r_o}{r_e} = -\frac{5.98\ \text{k}\Omega}{18.44\ \Omega} = \mathbf{-324.3}$ vs. $-368.76$

There was a measurable difference in the results for $Z_o$ and $A_v$, because the condition $r_o \geq 10R_C$ was *not* satisfied.

## 5.7 CE EMITTER-BIAS CONFIGURATION

The networks examined in this section include an emitter resistor that may or may not be bypassed in the ac domain. We first consider the unbypassed situation and then modify the resulting equations for the bypassed configuration.

### Unbypassed

The most fundamental of unbypassed configurations appears in Fig. 5.29. The $r_e$ equivalent model is substituted in Fig. 5.30, but note the absence of the resistance $r_o$. The effect of $r_o$ is to make the analysis a great deal more complicated, and considering the fact that in

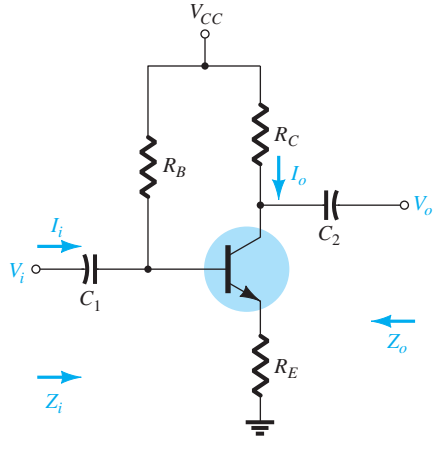



**FIG. 5.29**
*CE emitter-bias configuration.*

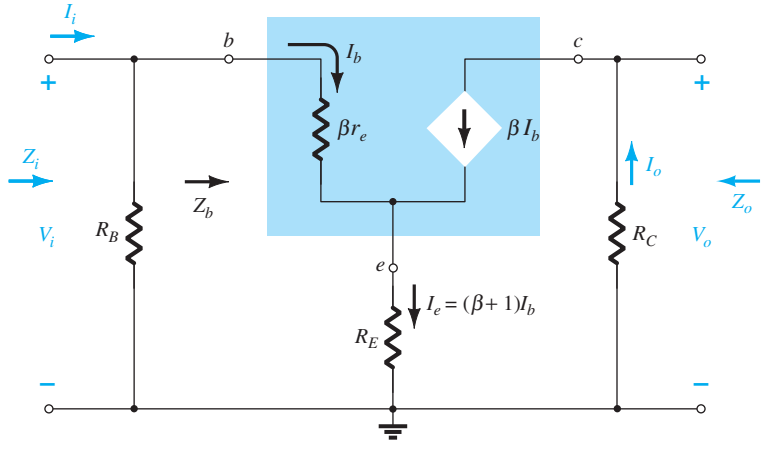



**FIG. 5.30**
*Substituting the $r_e$ equivalent circuit into the ac equivalent network of Fig. 5.29.*

most situations its effect can be ignored, it will not be included in the present analysis. However, the effect of $r_o$ will be discussed later in this section.

Applying Kirchhoff's voltage law to the input side of Fig. 5.30 results in

$$V_i = I_b\beta r_e + I_e R_E$$

or

$$V_i = I_b\beta r_e + (\beta + 1)I_b R_E$$

and the input impedance looking into the network to the right of $R_B$ is

$$Z_b = \frac{V_i}{I_b} = \beta r_e + (\beta + 1)R_E$$

The result as displayed in Fig. 5.31 reveals that the input impedance of a transistor with an unbypassed resistor $R_E$ is determined by

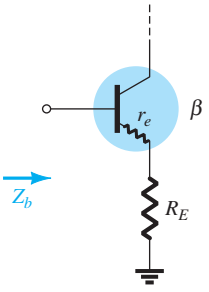



**FIG. 5.31**
*Defining the input impedance of a transistor with an unbypassed emitter resistor.*

$$\boxed{Z_b = \beta r_e + (\beta + 1)R_E} \tag{5.17}$$

Because $\beta$ is normally much greater than 1, the approximate equation is

$$Z_b \cong \beta r_e + \beta R_E$$

and

$$\boxed{Z_b \cong \beta(r_e + R_E)} \tag{5.18}$$

Because $R_E$ is usually greater than $r_e$, Eq. (5.18) can be further reduced to

$$\boxed{Z_b \cong \beta R_E} \tag{5.19}$$

**$Z_i$** Returning to Fig. 5.30, we have

$$\boxed{Z_i = R_B \| Z_b} \tag{5.20}$$

**$Z_o$** With $V_i$ set to zero, $I_b = 0$, and $\beta I_b$ can be replaced by an open-circuit equivalent. The result is

$$\boxed{Z_o = R_C} \tag{5.21}$$

**$A_v$**

$$I_b = \frac{V_i}{Z_b}$$

and

$$V_o = -I_o R_C = -\beta I_b R_C$$
$$= -\beta\left(\frac{V_i}{Z_b}\right)R_C$$

with

$$\boxed{A_v = \frac{V_o}{V_i} = -\frac{\beta R_C}{Z_b}} \tag{5.22}$$

Substituting $Z_b \cong \beta(r_e + R_E)$ gives

$$\boxed{A_v = \frac{V_o}{V_i} \cong -\frac{R_C}{r_e + R_E}} \tag{5.23}$$

and for the approximation $Z_b \cong \beta R_E$,

$$\boxed{A_v = \frac{V_o}{V_i} \cong -\frac{R_C}{R_E}} \tag{5.24}$$

Note the absence of $\beta$ from the equation for $A_v$ demonstrating an independence in variation of $\beta$.

**Phase Relationship** The negative sign in Eq. (5.22) again reveals a 180° phase shift between $V_o$ and $V_i$.

**Effect of $r_o$** The equations appearing below will clearly reveal the additional complexity resulting from including $r_o$ in the analysis. Note in each case, however, that when certain conditions are met, the equations return to the form just derived. The derivation of each equation is beyond the needs of this text and is left as an exercise for the reader. Each equation can be derived through *careful* application of the basic laws of circuit analysis such as Kirchhoff's voltage and current laws, source conversions, Thévenin's theorem, and so on. The equations were included to remove the nagging question of the effect of $r_o$ on the important parameters of a transistor configuration.

### $Z_i$

$$Z_b = \beta r_e + \left[\frac{(\beta + 1) + R_C/r_o}{1 + (R_C + R_E)/r_o}\right]R_E \tag{5.25}$$

Because the ratio $R_C/r_o$ is always much less than $(\beta + 1)$,

$$Z_b \cong \beta r_e + \frac{(\beta + 1)R_E}{1 + (R_C + R_E)/r_o}$$

For $r_o \geq 10(R_C + R_E)$,

$$Z_b \cong \beta r_e + (\beta + 1)R_E$$

which compares directly with Eq. (5.17).

In other words, if $r_o \geq 10(R_C + R_E)$, all the equations derived earlier result. Because $\beta + 1 \cong \beta$, the following equation is an excellent one for most applications:

$$Z_b \cong \beta(r_e + R_E) \qquad r_o \geq 10(R_C + R_E) \tag{5.26}$$

### $Z_o$

$$Z_o = R_C \| \left[ r_o + \frac{\beta(r_o + r_e)}{1 + \dfrac{\beta r_e}{R_E}} \right] \tag{5.27}$$

However, $r_o \gg r_e$, and

$$Z_o \cong R_C \| r_o \left[ 1 + \frac{\beta}{1 + \dfrac{\beta r_e}{R_E}} \right]$$

which can be written as

$$Z_o \cong R_C \| r_o \left[ 1 + \frac{1}{\dfrac{1}{\beta} + \dfrac{r_e}{R_E}} \right]$$

Typically $1/\beta$ and $r_e/R_E$ are less than one with a sum usually less than one. The result is a multiplying factor for $r_o$ greater than one. For $\beta = 100$, $r_e = 10\ \Omega$, and $R_E = 1\ \text{k}\Omega$,

$$\frac{1}{\dfrac{1}{\beta} + \dfrac{r_e}{R_E}} = \frac{1}{\dfrac{1}{100} + \dfrac{10\ \Omega}{1000\ \Omega}} = \frac{1}{0.02} = 50$$

and

$$Z_o = R_C \| 51 r_o$$

which is certainly simply $R_C$. Therefore,

$$Z_o \cong R_C \qquad \text{Any level of } r_o \tag{5.28}$$

which was obtained earlier.

### $A_v$

$$A_v = \frac{V_o}{V_i} = \frac{-\frac{\beta R_C}{Z_b}\left[1 + \frac{r_e}{r_o}\right] + \frac{R_C}{r_o}}{1 + \frac{R_C}{r_o}} \tag{5.29}$$

The ratio $\frac{r_e}{r_o} \ll 1$, and

$$A_v = \frac{V_o}{V_i} \cong \frac{-\frac{\beta R_C}{Z_b} + \frac{R_C}{r_o}}{1 + \frac{R_C}{r_o}}$$

For $r_o \geq 10R_C$,

$$A_v = \frac{V_o}{V_i} \cong -\frac{\beta R_C}{Z_b} \qquad r_o \geq 10R_C \tag{5.30}$$

as obtained earlier.

### Bypassed

If $R_E$ of Fig. 5.29 is bypassed by an emitter capacitor $C_E$, the complete $r_e$ equivalent model can be substituted, resulting in the same equivalent network as Fig. 5.22. Equations (5.5) to (5.10) are therefore applicable.

**EXAMPLE 5.3** For the network of Fig. 5.32, without $C_E$ (unbypassed), determine:

a. $r_e$.
b. $Z_i$.
c. $Z_o$.
d. $A_v$.

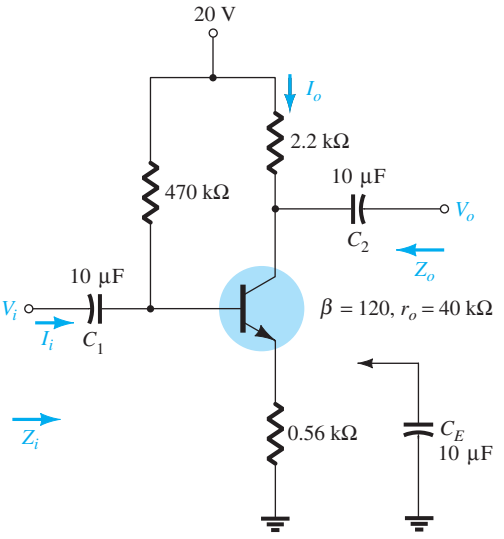



**FIG. 5.32**
*Example 5.3.*

**Solution:**

a. DC:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} = \frac{20\text{ V} - 0.7\text{ V}}{470\text{ k}\Omega + (121)0.56\text{ k}\Omega} = 35.89\ \mu\text{A}$$

$$I_E = (\beta + 1)I_B = (121)(35.89\ \mu\text{A}) = 4.34\text{ mA}$$

and

$$r_e = \frac{26\text{ mV}}{I_E} = \frac{26\text{ mV}}{4.34\text{ mA}} = \mathbf{5.99\ \Omega}$$

b. Testing the condition $r_o \geq 10(R_C + R_E)$, we obtain

$$40\,\text{k}\Omega \geq 10(2.2\,\text{k}\Omega + 0.56\,\text{k}\Omega)$$
$$40\,\text{k}\Omega \geq 10(2.76\,\text{k}\Omega) = 27.6\,\text{k}\Omega \ (\textit{satisfied})$$

Therefore,

$$Z_b \cong \beta(r_e + R_E) = 120(5.99\,\Omega + 560\,\Omega)$$
$$= 67.92\,\text{k}\Omega$$

and

$$Z_i = R_B \| Z_b = 470\,\text{k}\Omega \| 67.92\,\text{k}\Omega$$
$$= \mathbf{59.34\,k\Omega}$$

c. $Z_o = R_C = \mathbf{2.2\,k\Omega}$

d. $r_o \geq 10R_C$ is satisfied. Therefore,

$$A_v = \frac{V_o}{V_i} \cong -\frac{\beta R_C}{Z_b} = -\frac{(120)(2.2\,\text{k}\Omega)}{67.92\,\text{k}\Omega}$$
$$= \mathbf{-3.89}$$

compared to −3.93 using Eq. (5.20): $A_v \cong -R_C/R_E$.

**EXAMPLE 5.4** Repeat the analysis of Example 5.3 with $C_E$ in place.

***Solution:***

a. The dc analysis is the same, and $r_e = 5.99\,\Omega$.

b. $R_E$ is "shorted out" by $C_E$ for the ac analysis. Therefore,

$$Z_i = R_B \| Z_b = R_B \| \beta r_e = 470\,\text{k}\Omega \| (120)(5.99\,\Omega)$$
$$= 470\,\text{k}\Omega \| 718.8\,\Omega \cong \mathbf{717.70\,\Omega}$$

c. $Z_o = R_C = \mathbf{2.2\,k\Omega}$

d. $$A_v = -\frac{R_C}{r_e}$$
$$= -\frac{2.2\,\text{k}\Omega}{5.99\,\Omega} = \mathbf{-367.28}$$ (a significant increase)

**EXAMPLE 5.5** For the network of Fig. 5.33 (with $C_E$ unconnected), determine (using appropriate approximations):

a. $r_e$.
b. $Z_i$.
c. $Z_o$.
d. $A_v$.

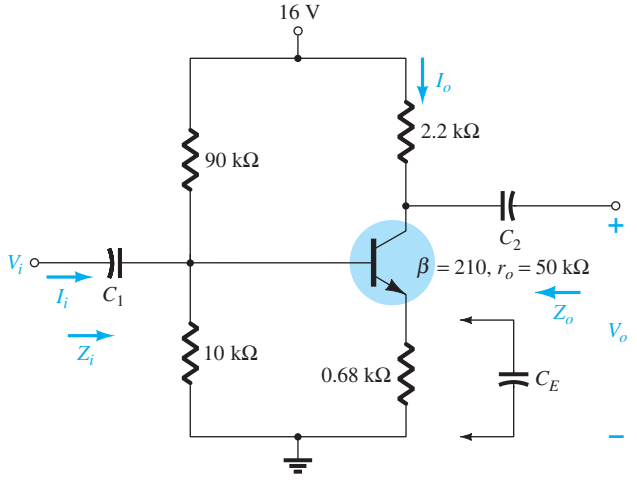



**FIG. 5.33**
*Example 5.5.*

**Solution:**

a. Testing $\beta R_E > 10R_2$,

$$(210)(0.68\ \text{k}\Omega) > 10(10\ \text{k}\Omega)$$
$$142.8\ \text{k}\Omega > 100\ \text{k}\Omega\ (\textit{satisfied})$$

we have

$$V_B = \frac{R_2}{R_1 + R_2}V_{CC} = \frac{10\ \text{k}\Omega}{90\ \text{k}\Omega + 10\ \text{k}\Omega}(16\ \text{V}) = 1.6\ \text{V}$$
$$V_E = V_B - V_{BE} = 1.6\ \text{V} - 0.7\ \text{V} = 0.9\ \text{V}$$
$$I_E = \frac{V_E}{R_E} = \frac{0.9\ \text{V}}{0.68\ \text{k}\Omega} = 1.324\ \text{mA}$$
$$r_e = \frac{26\ \text{mV}}{I_E} = \frac{26\ \text{mV}}{1.324\ \text{mA}} = \mathbf{19.64\ \Omega}$$

b. The ac equivalent circuit is provided in Fig. 5.34. The resulting configuration is different from Fig. 5.30 only by the fact that now

$$R_B = R' = R_1 \| R_2 = 9\ \text{k}\Omega$$

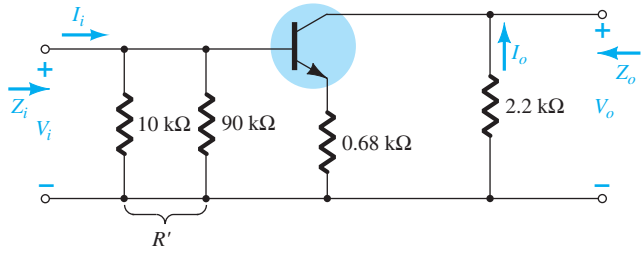



**FIG. 5.34**
*The ac equivalent circuit of Fig. 5.33.*

The testing conditions of $r_o \geq 10(R_C + R_E)$ and $r_o \geq 10R_C$ are both satisfied. Using the appropriate approximations yields

$$Z_b \cong \beta R_E = 142.8\ \text{k}\Omega$$
$$Z_i = R_B \| Z_b = 9\ \text{k}\Omega \| 142.8\ \text{k}\Omega$$
$$= \mathbf{8.47\ \text{k}\Omega}$$

c. $Z_o = R_C = \mathbf{2.2\ \text{k}\Omega}$

d. $A_v = -\frac{R_C}{R_E} = -\frac{2.2\ \text{k}\Omega}{0.68\ \text{k}\Omega} = \mathbf{-3.24}$

**EXAMPLE 5.6** Repeat Example 5.5 with $C_E$ in place.

**Solution:**

a. The dc analysis is the same, and $r_e = \mathbf{19.64\ \Omega}$.

b. $Z_b = \beta r_e = (210)(19.64\ \Omega) \cong 4.12\ \text{k}\Omega$

$$Z_i = R_B \| Z_b = 9\ \text{k}\Omega \| 4.12\ \text{k}\Omega$$
$$= \mathbf{2.83\ \text{k}\Omega}$$

c. $Z_o = R_C = \mathbf{2.2\ \text{k}\Omega}$

d. $A_v = -\frac{R_C}{r_e} = -\frac{2.2\ \text{k}\Omega}{19.64\ \Omega} = \mathbf{-112.02}$ (a significant increase)

Another variation of an emitter-bias configuration is shown in Fig. 5.35. For the dc analysis, the emitter resistance is $R_{E_1} + R_{E_2}$, whereas for the ac analysis, the resistor $R_E$ in the equations above is simply $R_{E_1}$ with $R_{E_2}$ bypassed by $C_E$.

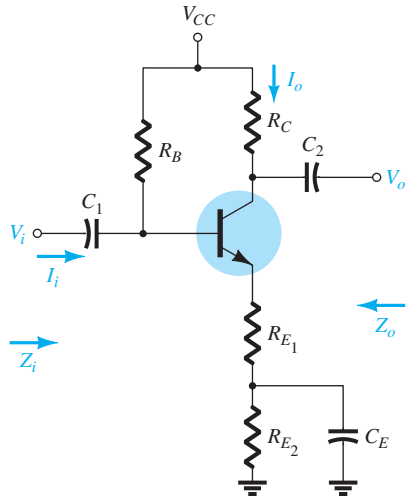



**FIG. 5.35**
*An emitter-bias configuration with a portion of the emitter-bias resistance bypassed in the ac domain.*

## 5.8 EMITTER-FOLLOWER CONFIGURATION

When the output is taken from the emitter terminal of the transistor as shown in Fig. 5.36, the network is referred to as an *emitter-follower*. The output voltage is always slightly less than the input signal due to the drop from base to emitter, but the approximation $A_v \cong 1$ is usually a good one. Unlike the collector voltage, the emitter voltage is in phase with the signal $V_i$. That is, both $V_o$ and $V_i$ attain their positive and negative peak values at the same time. The fact that $V_o$ "follows" the magnitude of $V_i$ with an in-phase relationship accounts for the terminology emitter-follower.

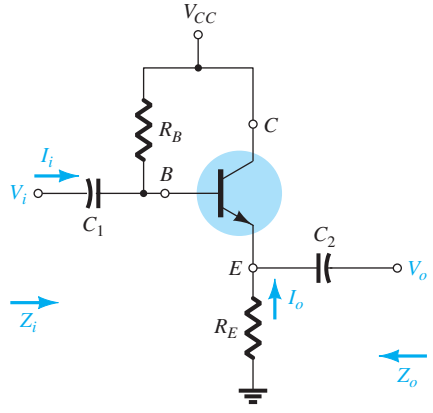



**FIG. 5.36**
*Emitter-follower configuration.*

The most common emitter-follower configuration appears in Fig. 5.36. In fact, because the collector is grounded for ac analysis, it is actually a *common-collector* configuration. Other variations of Fig. 5.36 that draw the output off the emitter with $V_o \cong V_i$ will appear later in this section.

The emitter-follower configuration is frequently used for impedance-matching purposes. It presents a high impedance at the input and a low impedance at the output, which is the direct opposite of the standard fixed-bias configuration. The resulting effect is much the same as that obtained with a transformer, where a load is matched to the source impedance for maximum power transfer through the system.

Substituting the $r_e$ equivalent circuit into the network of Fig. 5.36 results in the network of Fig. 5.37. The effect of $r_o$ will be examined later in the section.

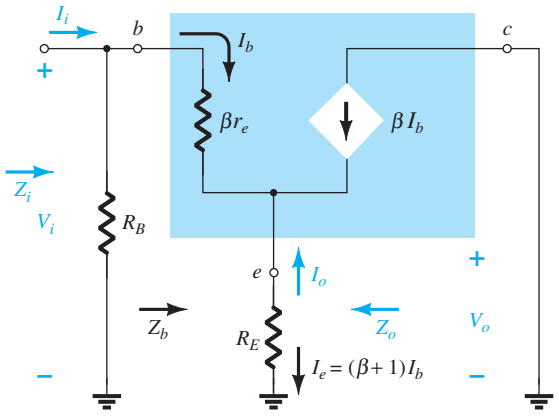



**FIG. 5.37**
*Substituting the $r_e$ equivalent circuit into the ac equivalent network of Fig. 5.36.*

**$Z_i$** The input impedance is determined in the same manner as described in the preceding section:

$$Z_i = R_B \| Z_b \tag{5.31}$$

with

$$Z_b = \beta r_e + (\beta + 1)R_E \tag{5.32}$$

or

$$Z_b \cong \beta(r_e + R_E) \tag{5.33}$$

and

$$Z_b \cong \beta R_E \quad R_E \gg r_e \tag{5.34}$$

**$Z_o$** The output impedance is best described by first writing the equation for the current $I_b$,

$$I_b = \frac{V_i}{Z_b}$$

and then multiplying by $(\beta + 1)$ to establish $I_e$. That is,

$$I_e = (\beta + 1)I_b = (\beta + 1)\frac{V_i}{Z_b}$$

Substituting for $Z_b$ gives

$$I_e = \frac{(\beta + 1)V_i}{\beta r_e + (\beta + 1)R_E}$$

or

$$I_e = \frac{V_i}{[\beta r_e/(\beta + 1)] + R_E}$$

but

$$(\beta + 1) \cong \beta$$

and

$$\frac{\beta r_e}{\beta + 1} \cong \frac{\beta r_e}{\beta} = r_e$$

so that

$$I_e \cong \frac{V_i}{r_e + R_E} \tag{5.35}$$

If we now construct the network defined by Eq. (5.35), the configuration of Fig. 5.38 results.

To determine $Z_o$, $V_i$ is set to zero and

$$Z_o = R_E \| r_e \tag{5.36}$$

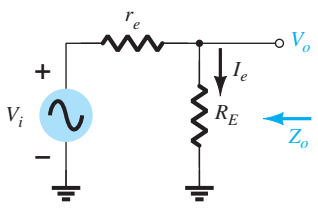



**FIG. 5.38**
*Defining the output impedance for the emitter-follower configuration.*

Because $R_E$ is typically much greater than $r_e$, the following approximation is often applied:

$$\boxed{Z_o \cong r_e} \tag{5.37}$$

**$A_v$** Figure 5.38 can be used to determine the voltage gain through an application of the voltage-divider rule:

$$V_o = \frac{R_E V_i}{R_E + r_e}$$

and

$$\boxed{A_v = \frac{V_o}{V_i} = \frac{R_E}{R_E + r_e}} \tag{5.38}$$

Because $R_E$ is usually much greater than $r_e$, $R_E + r_e \cong R_E$ and

$$\boxed{A_v = \frac{V_o}{V_i} \cong 1} \tag{5.39}$$

**Phase Relationship** As revealed by Eq. (5.38) and earlier discussions of this section, $V_o$ and $V_i$ are in phase for the emitter-follower configuration.

### Effect of $r_o$

#### $Z_i$

$$\boxed{Z_b = \beta r_e + \frac{(\beta + 1)R_E}{1 + \dfrac{R_E}{r_o}}} \tag{5.40}$$

If the condition $r_o \geq 10R_E$ is satisfied,

$$Z_b = \beta r_e + (\beta + 1)R_E$$

which matches earlier conclusions with

$$\boxed{Z_b \cong \beta(r_e + R_E)}_{\,r_o \geq 10R_E} \tag{5.41}$$

#### $Z_o$

$$\boxed{Z_o = r_o \| R_E \| \frac{\beta r_e}{(\beta + 1)}} \tag{5.42}$$

Using $\beta + 1 \cong \beta$, we obtain

$$Z_o = r_o \| R_E \| r_e$$

and because $r_o \gg r_e$,

$$\boxed{Z_o \cong R_E \| r_e}_{\text{ Any } r_o} \tag{5.43}$$

#### $A_v$

$$\boxed{A_v = \frac{(\beta + 1)R_E/Z_b}{1 + \dfrac{R_E}{r_o}}} \tag{5.44}$$

If the condition $r_o \geq 10R_E$ is satisfied and we use the approximation $\beta + 1 \cong \beta$, we find

$$A_v \cong \frac{\beta R_E}{Z_b}$$

But $$Z_b \cong \beta(r_e + R_E)$$

so that $$A_v \cong \frac{\beta R_E}{\beta(r_e + R_E)}$$

and $$\boxed{A_v \cong \frac{R_E}{r_e + R_E}}_{r_o \geq 10R_E} \tag{5.45}$$

**EXAMPLE 5.7** For the emitter-follower network of Fig. 5.39, determine:

a. $r_e$.
b. $Z_i$.
c. $Z_o$.
d. $A_v$.
e. Repeat parts (b) through (d) with $r_o = 25\ \text{k}\Omega$ and compare results.

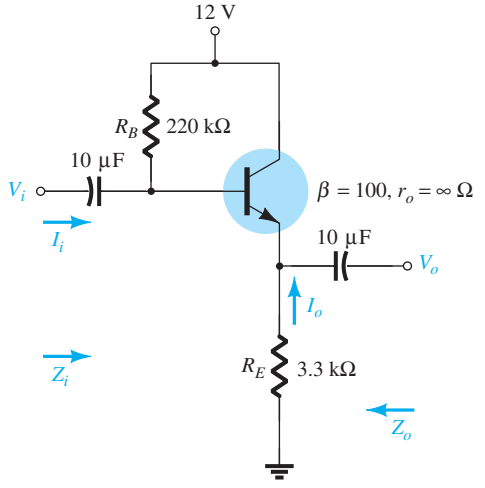



**FIG. 5.39**
*Example 5.7.*

***Solution:***

a. $$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}$$
$$= \frac{12\ \text{V} - 0.7\ \text{V}}{220\ \text{k}\Omega + (101)3.3\ \text{k}\Omega} = 20.42\ \mu\text{A}$$
$$I_E = (\beta + 1)I_B$$
$$= (101)(20.42\ \mu\text{A}) = 2.062\ \text{mA}$$
$$r_e = \frac{26\ \text{mV}}{I_E} = \frac{26\ \text{mV}}{2.062\ \text{mA}} = \mathbf{12.61\ \Omega}$$

b. $$Z_b = \beta r_e + (\beta + 1)R_E$$
$$= (100)(12.61\ \Omega) + (101)(3.3\ \text{k}\Omega)$$
$$= 1.261\ \text{k}\Omega + 333.3\ \text{k}\Omega$$
$$= 334.56\ \text{k}\Omega \cong \beta R_E$$
$$Z_i = R_B \| Z_b = 220\ \text{k}\Omega \| 334.56\ \text{k}\Omega$$
$$= \mathbf{132.72\ k\Omega}$$

c. $$Z_o = R_E \| r_e = 3.3\ \text{k}\Omega \| 12.61\ \Omega$$
$$= \mathbf{12.56\ \Omega} \cong r_e$$

d. $$A_v = \frac{V_o}{V_i} = \frac{R_E}{R_E + r_e} = \frac{3.3\ \text{k}\Omega}{3.3\ \text{k}\Omega + 12.61\ \Omega}$$
$$= \mathbf{0.996 \cong 1}$$

e. Checking the condition $r_o \geq 10R_E$, we have

$$25\ \text{k}\Omega \geq 10(3.3\ \text{k}\Omega) = 33\ \text{k}\Omega$$

which is *not* satisfied. Therefore,

$$Z_b = \beta r_e + \frac{(\beta + 1)R_E}{1 + \dfrac{R_E}{r_o}} = (100)(12.61\ \Omega) + \frac{(100 + 1)3.3\ \text{k}\Omega}{1 + \dfrac{3.3\ \text{k}\Omega}{25\ \text{k}\Omega}}$$

$$= 1.261\ \text{k}\Omega + 294.43\ \text{k}\Omega$$

$$= 295.7\ \text{k}\Omega$$

with $Z_i = R_B \| Z_b = 220\ \text{k}\Omega \| 295.7\ \text{k}\Omega$

$$= \mathbf{126.15\ k\Omega}\ \text{vs. } 132.72\ \text{k}\Omega \quad \text{obtained earlier}$$

$$Z_o = R_E \| r_e = \mathbf{12.56\ \Omega} \quad \text{as obtained earlier}$$

$$A_v = \frac{(\beta + 1)R_E/Z_b}{\left[1 + \dfrac{R_E}{r_o}\right]} = \frac{(100 + 1)(3.3\ \text{k}\Omega)/295.7\ \text{k}\Omega}{\left[1 + \dfrac{3.3\ \text{k}\Omega}{25\ \text{k}\Omega}\right]}$$

$$= \mathbf{0.996 \cong 1}$$

matching the earlier result.

In general, therefore, even though the condition $r_o \geq 10R_E$ is not satisfied, the results for $Z_o$ and $A_v$ are the same, with $Z_i$ only slightly less. The results suggest that for most applications a good approximation for the actual results can be obtained by simply ignoring the effects of $r_o$ for this configuration.

The network of Fig. 5.40 is a variation of the network of Fig. 5.36, which employs a voltage-divider input section to set the bias conditions. Equations (5.31) to (5.34) are changed only by replacing $R_B$ by $R' = R_1 \| R_2$.

The network of Fig. 5.41 also provides the input/output characteristics of an emitter-follower, but includes a collector resistor $R_C$. In this case $R_B$ is again replaced by the parallel combination of $R_1$ and $R_2$. The input impedance $Z_i$ and output impedance $Z_o$ are unaffected by $R_C$ because it is not reflected into the base or emitter equivalent networks. In fact, the only effect of $R_C$ is to determine the $Q$-point of operation.

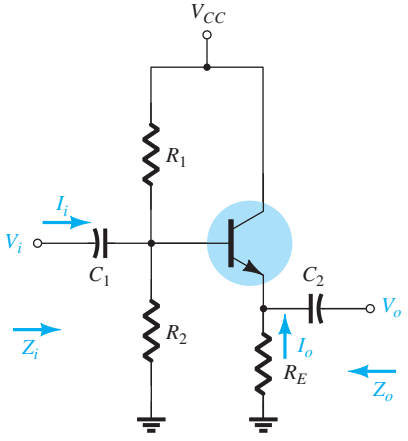



**FIG. 5.40**
*Emitter-follower configuration with a voltage-divider biasing arrangement.*

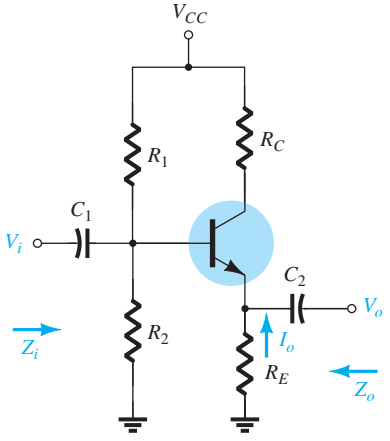



**FIG. 5.41**
*Emitter-follower configuration with a collector resistor $R_C$.*

## 5.9 COMMON-BASE CONFIGURATION

The common-base configuration is characterized as having a relatively low input and a high output impedance and a current gain less than 1. The voltage gain, however, can be quite large. The standard configuration appears in Fig. 5.42, with the common-base $r_e$ equivalent model substituted in Fig. 5.43. The transistor output impedance $r_o$ is not included for the

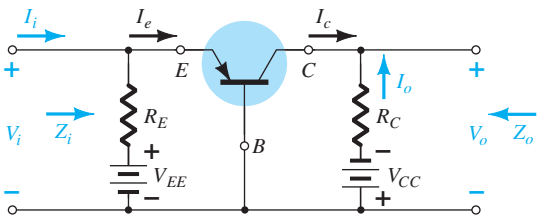



**FIG. 5.42**
*Common-base configuration.*

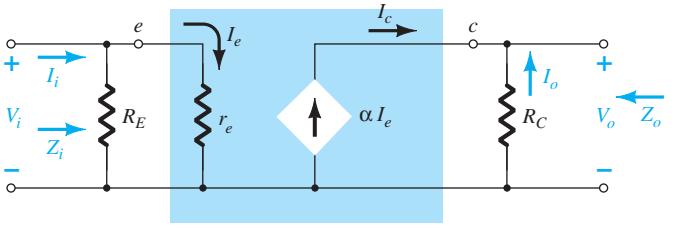



**FIG. 5.43**
*Substituting the $r_e$ equivalent circuit into the ac equivalent network of Fig. 5.44.*

common-base configuration because it is typically in the megohm range and can be ignored in parallel with the resistor $R_C$.

**$Z_i$**

$$Z_i = R_E \| r_e \tag{5.46}$$

**$Z_o$**

$$Z_o = R_C \tag{5.47}$$

**$A_v$**

$$V_o = -I_o R_C = -(-I_c)R_C = \alpha I_e R_C$$

with $$I_e = \frac{V_i}{r_e}$$

so that $$V_o = \alpha\left(\frac{V_i}{r_e}\right)R_C$$

and $$A_v = \frac{V_o}{V_i} = \frac{\alpha R_C}{r_e} \cong \frac{R_C}{r_e} \tag{5.48}$$

**$A_i$** Assuming that $R_E \gg r_e$ yields

$$I_e = I_i$$

and $$I_o = -\alpha I_e = -\alpha I_i$$

with $$A_i = \frac{I_o}{I_i} = -\alpha \cong -1 \tag{5.49}$$

**Phase Relationship** The fact that $A_v$ is a positive number shows that $V_o$ and $V_i$ are in phase for the common-base configuration.

**Effect of $r_o$** For the common-base configuration, $r_o = 1/h_{ob}$ is typically in the megohm range and sufficiently larger than the parallel resistance $R_C$ to permit the approximation $r_o \| R_C \cong R_C$.

**EXAMPLE 5.8** For the network of Fig. 5.44, determine:

a. $r_e$.
b. $Z_i$.
c. $Z_o$.
d. $A_v$.
e. $A_i$.

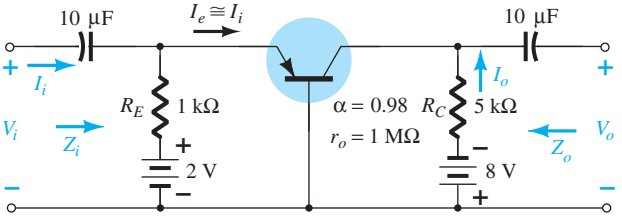



**FIG. 5.44**
*Example 5.8.*

**Solution:**

a. $I_E = \dfrac{V_{EE} - V_{BE}}{R_E} = \dfrac{2\text{ V} - 0.7\text{ V}}{1\text{ k}\Omega} = \dfrac{1.3\text{ V}}{1\text{ k}\Omega} = 1.3\text{ mA}$

$r_e = \dfrac{26\text{ mV}}{I_E} = \dfrac{26\text{ mV}}{1.3\text{ mA}} = \mathbf{20\ \Omega}$

b. $Z_i = R_E \| r_e = 1\text{ k}\Omega \| 20\ \Omega$

$= \mathbf{19.61\ \Omega} \cong r_e$

c. $Z_o = R_C = \mathbf{5\text{ k}\Omega}$

d. $A_v \cong \dfrac{R_C}{r_e} = \dfrac{5\text{ k}\Omega}{20\ \Omega} = \mathbf{250}$

e. $A_i = \mathbf{-0.98} \cong -1$

## 5.10 COLLECTOR FEEDBACK CONFIGURATION

The collector feedback network of Fig. 5.45 employs a feedback path from collector to base to increase the stability of the system as discussed in Section 4.6. However, the simple maneuver of connecting a resistor from base to collector rather than base to dc supply has a significant effect on the level of difficulty encountered when analyzing the network.

Some of the steps to be performed below are the result of experience working with such configurations. It is not expected that a new student of the subject would choose the sequence of steps described below without taking a wrong step or two. Substituting the equivalent circuit and redrawing the network results in the configuration of Fig. 5.46. The effects of a transistor output resistance $r_o$ will be discussed later in the section.

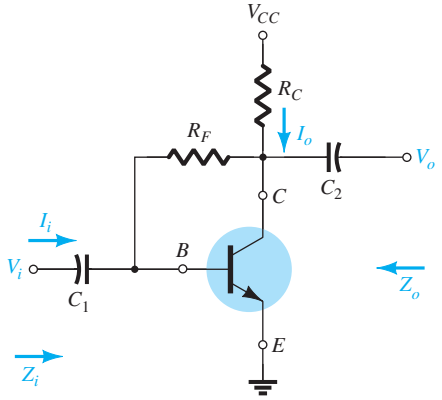



**FIG. 5.45**
*Collector feedback configuration.*

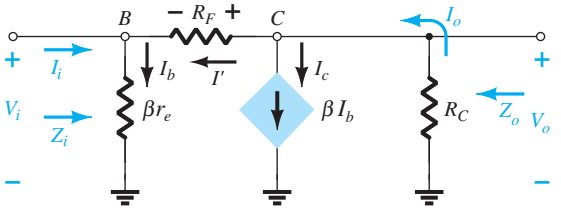



**FIG. 5.46**
*Substituting the $r_e$ equivalent circuit into the ac equivalent network of Fig. 5.45.*

### $Z_i$

$$I_o = I' + \beta I_b$$

and
$$I' = \frac{V_o - V_i}{R_F}$$

but
$$V_o = -I_o R_C = -(I' + \beta I_b)R_C$$

with
$$V_i = I_b \beta r_e$$

so that
$$I' = -\frac{(I' + \beta I_b)R_C - I_b \beta r_e}{R_F} = -\frac{I' R_C}{R_F} - \frac{\beta I_b R_C}{R_F} - \frac{I_b \beta r_e}{R_F}$$

which when rearranged in the following:

$$I'\left(1 + \frac{R_C}{R_F}\right) = -\beta I_b \frac{(R_C + r_e)}{R_F}$$

and finally,
$$I' = -\beta I_b \frac{(R_C + r_e)}{R_C + R_F}$$

Now $Z_i = \dfrac{V_i}{I_i}$:

and
$$I_i = I_b - I' = I_b + \beta I_b \frac{(R_C + r_e)}{R_C + R_F}$$

or
$$I_i = I_b\left(1 + \beta \frac{(R_C + r_e)}{R_C + R_F}\right)$$

Substituting for $V_i$ in the above equation for $Z_i$ leaves
$$Z_i = \frac{V_i}{I_i} = \frac{I_b \beta r_e}{I_b\left(1 + \beta \dfrac{(R_C + r_e)}{R_C + R_F}\right)} = \frac{\beta r_e}{1 + \beta \dfrac{(R_C + r_e)}{R_C + R_F}}$$

Since $R_C \gg r_e$
$$Z_i = \frac{\beta r_e}{1 + \dfrac{\beta R_C}{R_C + R_F}}$$

or
$$\boxed{Z_i = \frac{r_e}{\dfrac{1}{\beta} + \dfrac{R_C}{R_C + R_F}}} \qquad \textbf{(5.50)}$$

**$Z_o$** If we set $V_i$ to zero as required to define $Z_o$, the network will appear as shown in Fig. 5.47. The effect of $\beta r_e$ is removed, and $R_F$ appears in parallel with $R_C$ and

$$\boxed{Z_o \cong R_C \| R_F} \qquad \textbf{(5.51)}$$

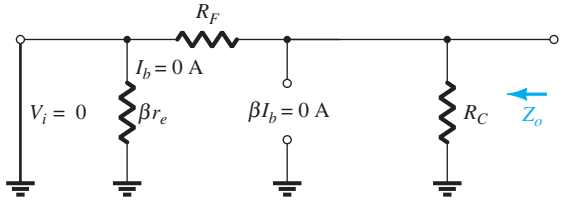



**FIG. 5.47**
*Defining $Z_o$ for the collector feedback configuration.*

**$A_v$**
$$V_o = -I_o R_C = -(I' + \beta I_b) R_C$$
$$= -\left(-\beta I_b \frac{(R_C + r_e)}{R_C + R_F} + \beta I_b\right) R_C$$

or
$$V_o = -\beta I_b\left(1 - \frac{(R_C + r_e)}{R_C + R_F}\right) R_C$$

Then
$$A_v = \frac{V_o}{V_i} = \frac{-\beta \cancel{I_b}\left(1 - \dfrac{(R_C + r_e)}{R_C + R_F}\right) R_C}{\beta r_e \cancel{I_b}}$$
$$= -\left(1 - \frac{(R_C + r_e)}{R_C + R_F}\right)\frac{R_C}{r_e}$$

For $R_C \gg r_e$
$$A_v = -\left(1 - \frac{R_C}{R_C + R_F}\right)\frac{R_C}{r_e}$$

or
$$A_v = -\frac{(\cancel{R_C} + R_F - \cancel{R_C})R_C}{R_C + R_F \qquad r_e}$$

and
$$\boxed{A_v = -\left(\frac{R_F}{R_C + R_F}\right)\frac{R_C}{r_e}} \tag{5.52}$$

For $R_F \gg R_C$

$$\boxed{A_v \cong -\frac{R_C}{r_e}} \tag{5.53}$$

**Phase Relationship** The negative sign of Eq. (5.52) indicates a 180° phase shift between $V_o$ and $V_i$.

## Effect of $r_o$

**$Z_i$** A complete analysis without applying approximations results in

$$\boxed{Z_i = \frac{1 + \dfrac{R_C \| r_o}{R_F}}{\dfrac{1}{\beta r_e} + \dfrac{1}{R_F} + \dfrac{R_C \| r_o}{\beta r_e R_F} + \dfrac{R_C \| r_o}{R_F r_e}}} \tag{5.54}$$

Applying the condition $r_o \geq 10R_C$, we obtain

$$Z_i = \frac{1 + \dfrac{R_C}{R_F}}{\dfrac{1}{\beta r_e} + \dfrac{1}{R_F} + \dfrac{R_C}{\beta r_e R_F} + \dfrac{R_C}{R_F r_e}} = \frac{r_e\left[1 + \dfrac{R_C}{R_F}\right]}{\dfrac{1}{\beta} + \dfrac{1}{R_F}\left[r_e + \dfrac{R_C}{\beta} + R_C\right]}$$

Applying $R_C \gg r_e$ and $\dfrac{R_C}{\beta}$,

$$Z_i \cong \frac{r_e\left[1 + \dfrac{R_C}{R_F}\right]}{\dfrac{1}{\beta} + \dfrac{R_C}{R_F}} = \frac{r_e\left[\dfrac{R_F + R_C}{\cancel{R_F}}\right]}{\dfrac{R_F + \beta R_C}{\beta \cancel{R_F}}} = \frac{r_e}{\dfrac{1}{\beta}\left(\dfrac{R_F}{R_F + R_C}\right) + \dfrac{R_C}{R_C + R_F}}$$

but, since $R_F$ typically $\gg R_C$, $R_F + R_C \cong R_F$ and $\dfrac{R_F}{R_F + R_C} = 1$

$$\boxed{Z_i \cong \frac{r_e}{\dfrac{1}{\beta} + \dfrac{R_C}{R_C + R_F}}}_{r_o \gg R_C,\ R_F > R_C} \tag{5.55}$$

as obtained earlier.

**$Z_o$** Including $r_o$ in parallel with $R_C$ in Fig. 5.47 results in

$$\boxed{Z_o = r_o \| R_C \| R_F} \tag{5.56}$$

For $r_o \geq 10R_C$,

$$\boxed{Z_o \cong R_C \| R_F}_{r_o \geq 10R_C} \tag{5.57}$$

as obtained earlier. For the common condition of $R_F \gg R_C$,

$$\boxed{Z_o \cong R_C}_{r_o \geq 10R_C,\ R_F \gg R_C} \tag{5.58}$$

### $A_v$

$$A_v = -\left(\frac{R_F}{R_C \| r_o + R_F}\right)\frac{R_C \| r_o}{r_e} \tag{5.59}$$

For $r_o \geq 10R_C$,

$$A_v \cong -\left(\frac{R_F}{R_C + R_F}\right)\frac{R_C}{r_e} \quad r_o \geq 10R_C \tag{5.60}$$

and for $R_F \gg R_C$

$$A_v \cong -\frac{R_C}{r_e} \quad r_o \geq 10R_C,\ R_F \geq R_C \tag{5.61}$$

as obtained earlier.

**EXAMPLE 5.9** For the network of Fig. 5.48. determine:

a. $r_e$.
b. $Z_i$.
c. $Z_o$.
d. $A_v$.
e. Repeat parts (b) through (d) with $r_o = 20\ \text{k}\Omega$ and compare results.

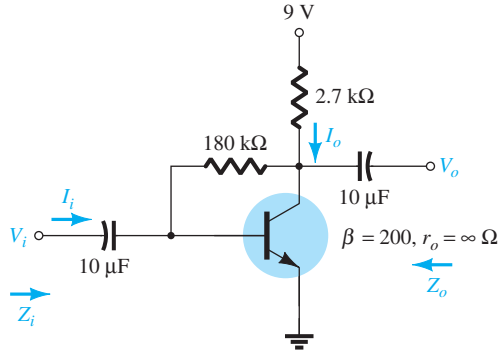



**FIG. 5.48**
*Example 5.9.*

**Solution:**

a. $$I_B = \frac{V_{CC} - V_{BE}}{R_F + \beta R_C} = \frac{9\ \text{V} - 0.7\ \text{V}}{180\ \text{k}\Omega + (200)2.7\ \text{k}\Omega}$$
$$= 11.53\ \mu\text{A}$$
$$I_E = (\beta + 1)I_B = (201)(11.53\ \mu\text{A}) = 2.32\ \text{mA}$$
$$r_e = \frac{26\ \text{mV}}{I_E} = \frac{26\ \text{mV}}{2.32\ \text{mA}} = \mathbf{11.21\ \Omega}$$

b. $$Z_i = \frac{r_e}{\frac{1}{\beta} + \frac{R_C}{R_C + R_F}} = \frac{11.21\ \Omega}{\frac{1}{200} + \frac{2.7\ \text{k}\Omega}{182.7\ \text{k}\Omega}} = \frac{11.21\ \Omega}{0.005 + 0.0148}$$
$$= \frac{11.21\ \Omega}{0.0198} = \mathbf{566.16\ \Omega}$$

c. $$Z_o = R_C \| R_F = 2.7\ \text{k}\Omega \| 180\ \text{k}\Omega = \mathbf{2.66\ \text{k}\Omega}$$

d. $$A_v = -\frac{R_C}{r_e} = -\frac{2.7\ \text{k}\Omega}{11.21\ \Omega} = \mathbf{-240.86}$$

e. $Z_i$: The condition $r_o \geq 10R_C$ is *not* satisfied. Therefore,

$$Z_i = \frac{1 + \dfrac{R_C \| r_o}{R_F}}{\dfrac{1}{\beta r_e} + \dfrac{1}{R_F} + \dfrac{R_C \| r_o}{\beta r_e R_F} + \dfrac{R_C \| r_o}{R_F r_e}} = \frac{1 + \dfrac{2.7\,\text{k}\Omega \| 20\,\text{k}\Omega}{180\,\text{k}\Omega}}{\dfrac{1}{(200)(11.21)} + \dfrac{1}{180\,\text{k}\Omega} + \dfrac{2.7\,\text{k}\Omega \| 20\,\text{k}\Omega}{(200)(11.21\,\Omega)(180\,\text{k}\Omega)} + \dfrac{2.7\,\text{k}\Omega \| 20\,\text{k}\Omega}{(180\,\text{k}\Omega)(11.21\,\Omega)}}$$

$$= \frac{1 + \dfrac{2.38\,\text{k}\Omega}{180\,\text{k}\Omega}}{0.45 \times 10^{-3} + 0.006 \times 10^{-3} + 5.91 \times 10^{-6} + 1.18 \times 10^{-3}} = \frac{1 + 0.013}{1.64 \times 10^{-3}}$$

$$= \mathbf{617.7\ \Omega} \text{ vs. } 566.16\ \Omega \text{ above}$$

**$Z_o$:**

$$Z_o = r_o \| R_C \| R_F = 20\,\text{k}\Omega \| 2.7\,\text{k}\Omega \| 180\,\text{k}\Omega$$

$$= \mathbf{2.35\ k\Omega} \text{ vs. } 2.66\,\text{k}\Omega \text{ above}$$

**$A_v$:**

$$= -\left(\frac{R_F}{R_C \| r_o + R_F}\right)\frac{R_C \| r_o}{r_e} = -\left[\frac{180\,\text{k}\Omega}{2.38\,\text{k}\Omega + 180\,\text{k}\Omega}\right]\frac{2.38\,\text{k}\Omega}{11.21}$$

$$= -[0.987]212.3$$

$$= \mathbf{-209.54}$$

For the configuration of Fig. 5.49, Eqs. (5.61) through (5.63) determine the variables of interest. The derivations are left as an exercise at the end of the chapter.

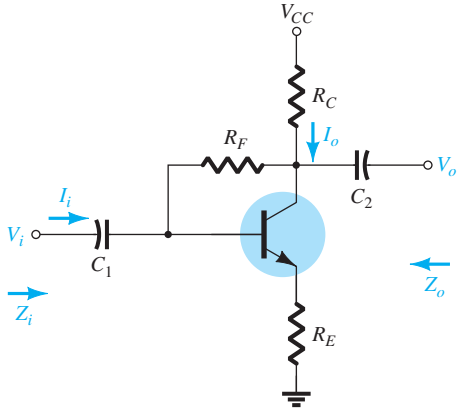



**FIG. 5.49**

*Collector feedback configuration with an emitter resistor $R_E$.*

**$Z_i$**

$$Z_i \cong \frac{R_E}{\left[\dfrac{1}{\beta} + \dfrac{(R_E + R_C)}{R_F}\right]} \tag{5.62}$$

**$Z_o$**

$$Z_o = R_C \| R_F \tag{5.63}$$

**$A_v$**

$$A_v \cong -\frac{R_C}{R_E} \tag{5.64}$$

## 5.11 COLLECTOR DC FEEDBACK CONFIGURATION

The network of Fig. 5.50 has a dc feedback resistor for increased stability, yet the capacitor $C_3$ will shift portions of the feedback resistance to the input and output sections of the network in the ac domain. The portion of $R_F$ shifted to the input or output side will be determined by the desired ac input and output resistance levels.

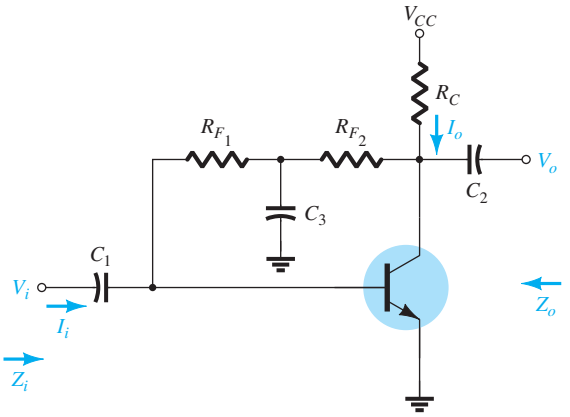



**FIG. 5.50**
*Collector dc feedback configuration.*

At the frequency or frequencies of operation, the capacitor will assume a short-circuit equivalent to ground due to its low impedance level compared to the other elements of the network. The small-signal ac equivalent circuit will then appear as shown in Fig. 5.51.

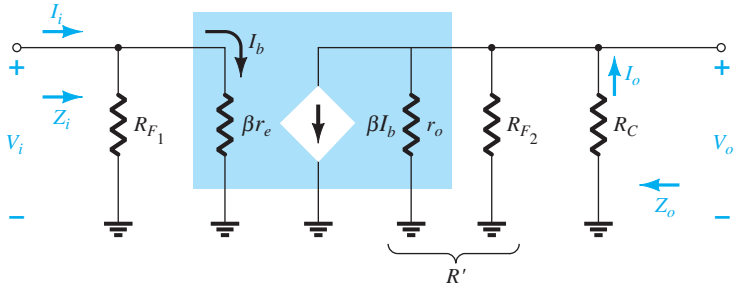



**FIG. 5.51**
*Substituting the $r_e$ equivalent circuit into the ac equivalent network of Fig. 5.50.*

### $Z_i$

$$Z_i = R_{F_1} \| \beta r_e \tag{5.65}$$

### $Z_o$

$$Z_o = R_C \| R_{F_2} \| r_o \tag{5.66}$$

For $r_o \geq 10R_C$,

$$Z_o \cong R_C \| R_{F_2} \quad r_o \geq 10R_C \tag{5.67}$$

### $A_v$

$$R' = r_o \| R_{F_2} \| R_C$$

and

$$V_o = -\beta I_b R'$$

but

$$I_b = \frac{V_i}{\beta r_e}$$

and $$V_o = -\beta \frac{V_i}{\beta r_e} R'$$

so that

$$\boxed{A_v = \frac{V_o}{V_i} = -\frac{r_o \| R_{F_2} \| R_C}{r_e}} \tag{5.68}$$

For $r_o \geq 10R_C$,

$$\boxed{A_v = \frac{V_o}{V_i} \cong -\frac{R_{F_2} \| R_C}{r_e}}_{r_o \geq 10R_C} \tag{5.69}$$

**Phase Relationship** The negative sign in Eq. (5.68) clearly reveals a 180° phase shift between input and output voltages.

**EXAMPLE 5.10** For the network of Fig. 5.52, determine:

a. $r_e$.
b. $Z_i$.
c. $Z_o$.
d. $A_v$.
e. $V_o$ if $V_i = 2$ mV

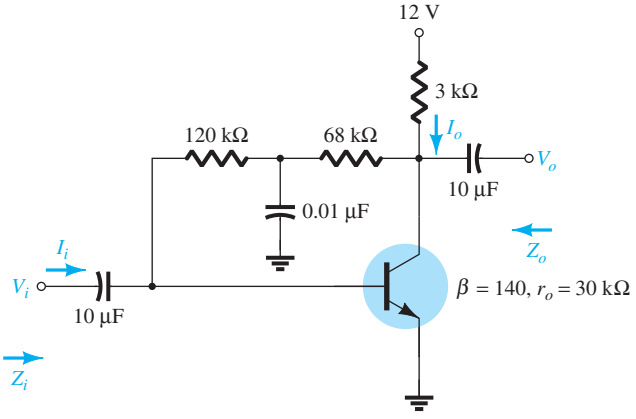



**FIG. 5.52**
*Example 5.10.*

***Solution:***

a. DC: $$I_B = \frac{V_{CC} - V_{BE}}{R_F + \beta R_C}$$

$$= \frac{12\text{ V} - 0.7\text{ V}}{(120\text{ k}\Omega + 68\text{ k}\Omega) + (140)3\text{ k}\Omega}$$

$$= \frac{11.3\text{ V}}{608\text{ k}\Omega} = 18.6\ \mu\text{A}$$

$$I_E = (\beta + 1)I_B = (141)(18.6\ \mu\text{A})$$

$$= 2.62\text{ mA}$$

$$r_e = \frac{26\text{ mV}}{I_E} = \frac{26\text{ mV}}{2.62\text{ mA}} = \mathbf{9.92\ \Omega}$$

b. $\beta r_e = (140)(9.92\ \Omega) = 1.39\text{ k}\Omega$

The ac equivalent network appears in Fig. 5.53.

$$Z_i = R_{F_1} \| \beta r_e = 120\text{ k}\Omega \| 1.39\text{ k}\Omega$$

$$\cong \mathbf{1.37\ k\Omega}$$

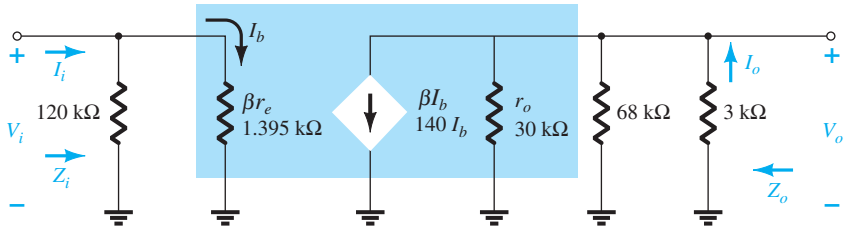



**FIG. 5.53**

*Substituting the $r_e$ equivalent circuit into the ac equivalent network of Fig. 5.52.*

c. Testing the condition $r_o \geq 10R_C$, we find

$$30\ \text{k}\Omega \geq 10(3\ \text{k}\Omega) = 30\ \text{k}\Omega$$

which is satisfied through the equals sign in the condition. Therefore,

$$Z_o \cong R_C \| R_{F_2} = 3\ \text{k}\Omega \| 68\ \text{k}\Omega$$
$$= \mathbf{2.87\ k\Omega}$$

d. $r_o \geq 10R_C$; therefore,

$$A_v \cong -\frac{R_{F_2} \| R_C}{r_e} = -\frac{68\ \text{k}\Omega \| 3\ \text{k}\Omega}{9.92\ \Omega}$$
$$\cong -\frac{2.87\ \text{k}\Omega}{9.92\ \Omega}$$
$$\cong \mathbf{-289.3}$$

e. $|A_v| = 289.3 = \dfrac{V_o}{V_i}$

$$V_o = 289.3V_i = 289.3(2\ \text{mV}) = \mathbf{0.579\ V}$$

## 5.12 EFFECT OF $R_L$ AND $R_S$

All the parameters determined in the last few sections have been for an unloaded amplifier with the input voltage connected directly to a terminal of the transistor. In this section the effect of applying a load to the output terminal and the effect of using a source with an internal resistance will be investigated. The network of Fig. 5.54a is typical of those investigated in the previous section. Because a resistive load was not attached to the output terminal, the gain is commonly referred to as the no-load gain and given the following notation:

$$A_{v_{\text{NL}}} = \frac{V_o}{V_i} \tag{5.70}$$

In Fig. 5.54b a load has been added in the form of a resistor $R_L$, which will change the overall gain of the system. This loaded gain is typically given the following notation:

$$A_{v_L} = \frac{V_o}{V_i} \quad \text{with } R_L \tag{5.71}$$

In Fig. 5.54c both a load and a source resistance have been introduced, which will have an additional effect on the gain of the system. The resulting gain is typically given the following notation:

$$A_{v_s} = \frac{V_o}{V_s} \quad \text{with } R_L \text{ and } R_s \tag{5.72}$$

The analysis to follow will show that:

***The loaded voltage gain of an amplifier is always less than the no-load gain.***

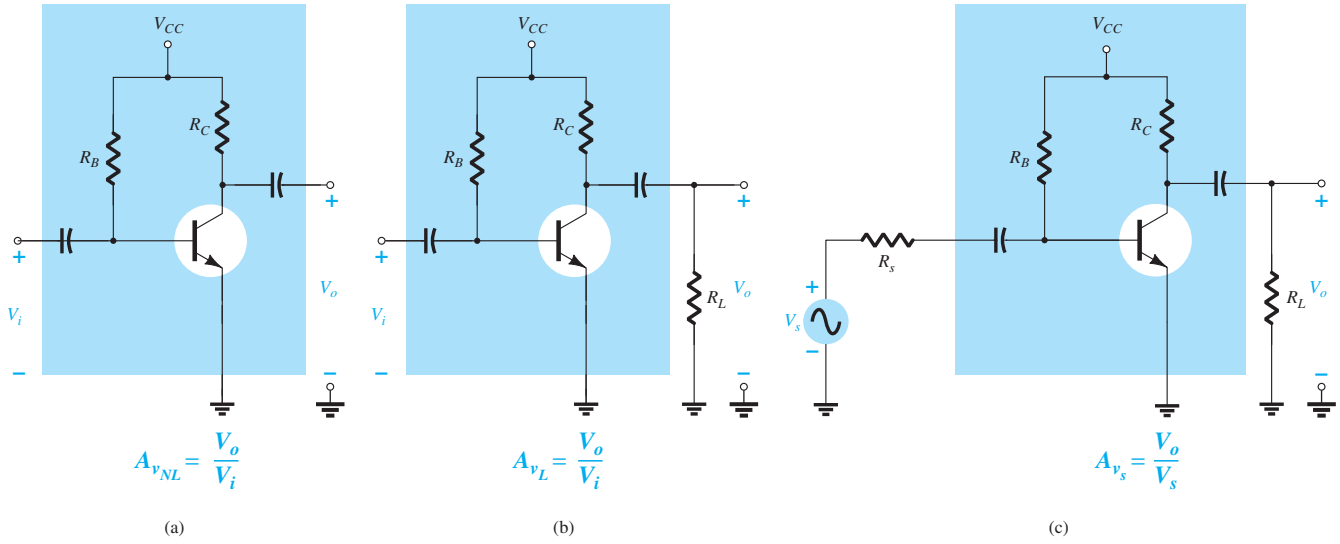



**FIG. 5.54**

*Amplifier configurations: (a) unloaded; (b) loaded; (c) loaded with a source resistance.*

In other words, the addition of a load resistor $R_L$ to the configuration of Fig. 5.54a will always have the effect of reducing the gain below the no-load level.

Furthermore:

***The gain obtained with a source resistance in place will always be less than that obtained under loaded or unloaded conditions due to the drop in applied voltage across the source resistance.***

In total, therefore, the highest gain is obtained under no-load conditions and the lowest gain with a source impedance and load in place. That is:

***For the same configuration*** $A_{v_{NL}} > A_{v_L} > A_{v_s}$.

It will also be interesting to verify that:

***For a particular design, the larger the level of*** $R_L$***, the greater is the level of ac gain.***

In other words, the larger the load resistance, the closer it is to an open-circuit approximation that would result in the higher no-load gain.

In addition:

***For a particular amplifier, the smaller the internal resistance of the signal source, the greater is the overall gain.***

In other words, the closer the source resistance is to a short-circuit approximation, the greater is the gain because the effect of $R_s$ will essentially be eliminated.

***For any network, such as those shown in Fig. 5.54 that have coupling capacitors, the source and load resistance do not affect the dc biasing levels.***

The conclusions listed above are all quite important in the amplifier design process. When one purchases a packaged amplifier, the listed gain and all the other parameters are for the *unloaded situation.* The gain that results due to the application of a load or source resistance can have a dramatic effect on all the amplifier parameters, as will be demonstrated in the examples to follow.

In general, there are two directions one can take to analyze networks with an applied load and/or source resistance. One approach is to simply insert the equivalent circuit, as was demonstrated in Section 5.11, and use methods of analysis to determine the quantities of interest. The second is to define a two-port equivalent model and use the parameters determined for the no-load situation. The analysis to follow in this section will use the first approach, leaving the second method for Section 5.14.

For the fixed-bias transistor amplifier of Fig. 5.54c, substituting the $r_e$ equivalent circuit for the transistor and removing the dc parameters results in the configuration of Fig. 5.55.

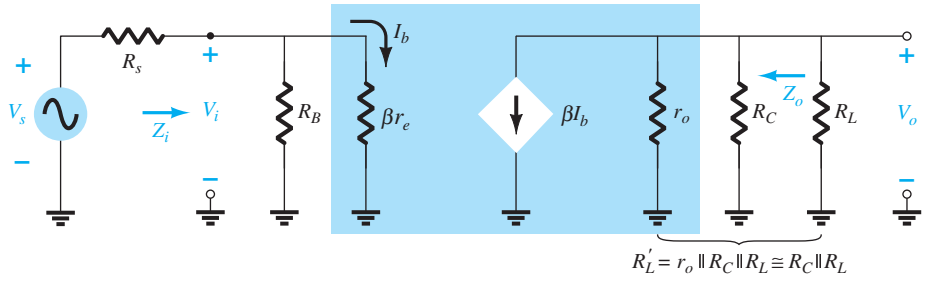



**FIG. 5.55**
*The ac equivalent network for the network of Fig. 5.54c.*

It is particularly interesting that Fig. 5.55 is exactly the same in appearance as Fig. 5.22 except that now there is a load resistance in parallel with $R_C$ and a source resistance has been introduced in series with a source $V_s$.

The parallel combination of

$$R'_L = r_o \| R_C \| R_L \cong R_C \| R_L$$

and

$$V_o = -\beta I_b R'_L = -\beta I_b (R_C \| R_L)$$

with

$$I_b = \frac{V_i}{\beta r_e}$$

gives

$$V_o = -\beta \left( \frac{V_i}{\beta r_e} \right) (R_C \| R_L)$$

so that

$$\boxed{A_{v_L} = \frac{V_o}{V_i} = -\frac{R_C \| R_L}{r_e}} \tag{5.73}$$

The only difference in the gain equation using $V_i$ as the input voltage is the fact that $R_C$ of Eq. (5.10) has been replaced by the parallel combination of $R_C$ and $R_L$. This makes good sense because the output voltage of Fig. 5.55 is now across the parallel combination of the two resistors.

The input impedance is

$$\boxed{Z_i = R_B \| \beta r_e} \tag{5.74}$$

as before, and the output impedance is

$$\boxed{Z_o = R_C \| r_o} \tag{5.75}$$

as before.

If the overall gain from signal source $V_s$ to output voltage $V_o$ is desired, it is only necessary to apply the voltage-divider rule as follows:

$$V_i = \frac{Z_i V_s}{Z_i + R_s}$$

and

$$\frac{V_i}{V_s} = \frac{Z_i}{Z_i + R_s}$$

or

$$A_{v_S} = \frac{V_o}{V_s} = \frac{V_o}{V_i} \cdot \frac{V_i}{V_s} = A_{v_L} \frac{Z_i}{Z_i + R_s}$$

so that

$$\boxed{A_{v_S} = \frac{Z_i}{Z_i + R_s} A_{v_L}} \tag{5.76}$$

Because the factor $Z_i/(Z_i + R_s)$ must always be less than one, Eq. (5.76) clearly supports the fact that the signal gain $A_{v_S}$ is always less than the loaded gain $A_{v_L}$.

**EXAMPLE 5.11** Using the parameter values for the fixed-bias configuration of Example 5.1 with an applied load of 4.7 kΩ and a source resistance of 0.3 kΩ, determine the following and compare to the no-load values:

a. $A_{v_L}$.
b. $A_{v_s}$.
c. $Z_i$.
d. $Z_o$.

***Solution:***

a. Eq. (5.73): $$A_{v_L} = -\frac{R_C \| R_L}{r_e} = -\frac{3\,\text{k}\Omega \| 4.7\,\text{k}\Omega}{10.71\ \Omega} = -\frac{1.831\,\text{k}\Omega}{10.71\ \Omega} = \mathbf{-170.98}$$

which is significantly less than the no-load gain of −280.11.

b. Eq. (5.76): $$A_{v_s} = \frac{Z_i}{Z_i + R_s} A_{v_L}$$

With $Z_i = 1.07\,\text{k}\Omega$ from Example 5.1, we have

$$A_{v_s} = \frac{1.07\,\text{k}\Omega}{1.07\,\text{k}\Omega + 0.3\,\text{k}\Omega}(-170.98) = \mathbf{-133.54}$$

which again is significantly less than $A_{v_{\text{NL}}}$ or $A_{v_L}$.

c. $Z_i = \mathbf{1.07\,k\Omega}$ as obtained for the no-load situation.

d. $Z_o = R_C = \mathbf{3\,k\Omega}$ as obtained for the no-load situation.

The example clearly demonstrates that $A_{v_{\text{NL}}} > A_{v_L} > A_{v_s}$.

For the voltage-divider configuration of Fig. 5.56 with an applied load and series source resistor the ac equivalent network is as shown in Fig. 5.57.

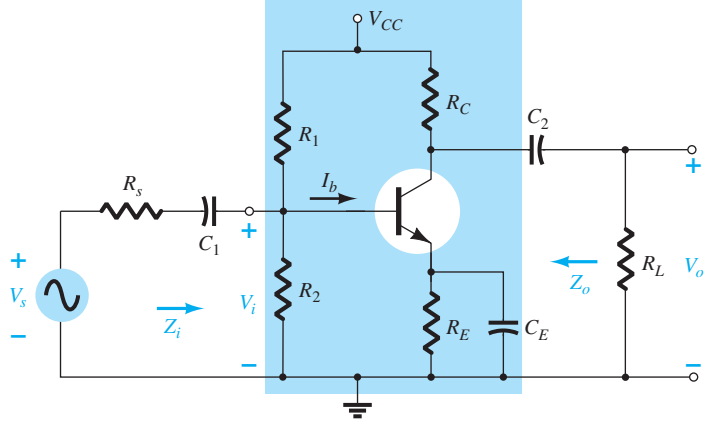



**FIG. 5.56**
*Voltage-divider bias configuration with $R_s$ and $R_L$.*

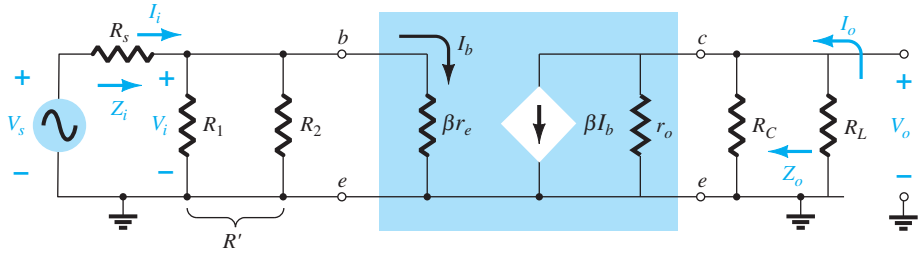



**FIG. 5.57**
*Substituting the $r_e$ equivalent circuit into the ac equivalent network of Fig. 5.56.*

First note the strong similarities with Fig. 5.55, with the only difference being the parallel connection of $R_1$ and $R_2$ instead of just $R_B$. Everything else is exactly the same. The following equations result for the important parameters of the configuration:

$$A_{v_L} = \frac{V_o}{V_i} = -\frac{R_C \| R_L}{r_e} \tag{5.77}$$

$$Z_i = R_1 \| R_2 \| \beta r_e \tag{5.78}$$

$$Z_o = R_C \| r_o \tag{5.79}$$

For the emitter-follower configuration of Fig. 5.58 the small-signal ac equivalent network is as shown in Fig. 5.59. The only difference between Fig. 5.59 and the unloaded configuration of Fig. 5.37 is the parallel combination of $R_E$ and $R_L$ and the addition of the source resistor $R_s$. The equations for the quantities of interest can therefore be determined by simply replacing $R_E$ by $R_E \| R_L$ wherever $R_E$ appears. If $R_E$ does not appear in an equation, the load resistor $R_L$ does not affect that parameter. That is,

$$A_{v_L} = \frac{V_o}{V_i} = \frac{R_E \| R_L}{R_E \| R_L + r_e} \tag{5.80}$$

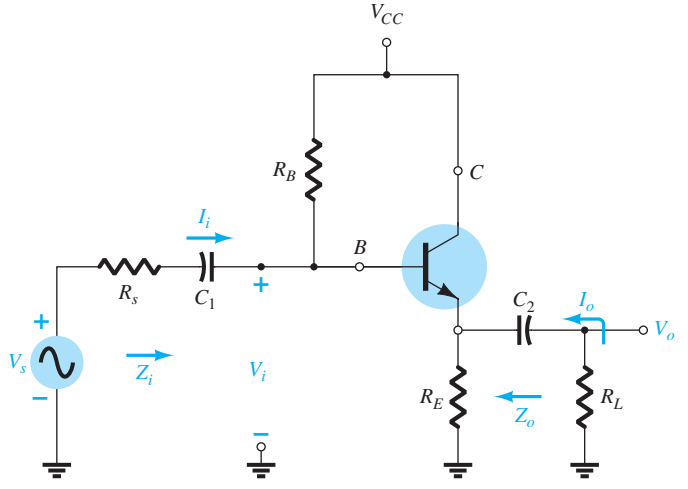



**FIG. 5.58**
*Emitter-follower configuration with $R_s$ and $R_L$.*

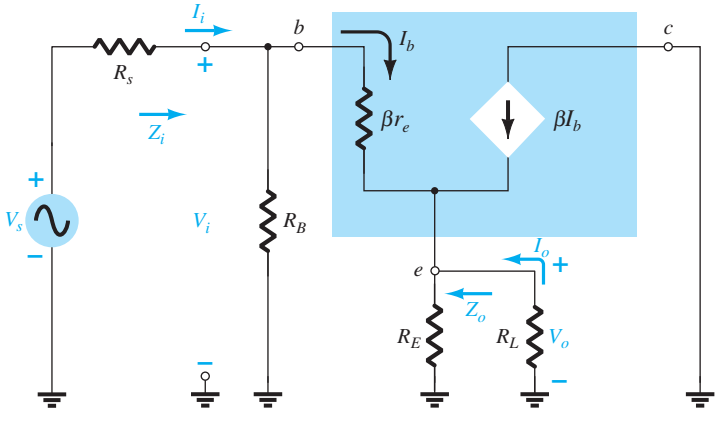



**FIG. 5.59**
*Substituting the $r_e$ equivalent circuit into the ac equivalent network of Fig. 5.58.*

$$Z_i = R_B \| Z_b \tag{5.81}$$

$$Z_b \cong \beta(R_E \| R_L) \tag{5.82}$$

$$Z_o \cong r_e \tag{5.83}$$

The effect of a load resistor and a source impedance on the remaining BJT configurations will not be examined in detail here, although Table 5.1 in Section 5.14 will review the results for each configuration.

## 5.13 DETERMINING THE CURRENT GAIN

You may have noticed in the previous sections that the current gain was not determined for each configuration. Earlier editions of this text did have the details of finding that gain, but in reality the voltage gain is usually the gain of most importance. The absence of the derivations should not cause concern because:

***For each transistor configuration, the current gain can be determined directly from the voltage gain, the defined load, and the input impedance.***

The derivation of the equation linking the voltage and current gains can be derived using the two-port configuration of Fig. 5.60.

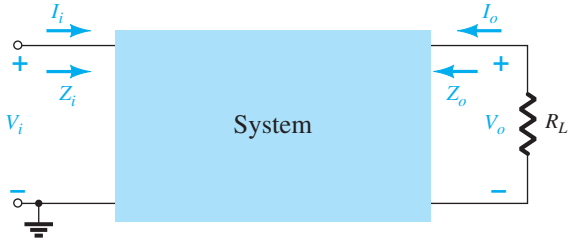



**FIG. 5.60**
*Determining the current gain using the voltage gain.*

The current gain is defined by

$$A_i = \frac{I_o}{I_i} \tag{5.84}$$

Applying Ohm's law to the input and output circuits results in

$$I_i = \frac{V_i}{Z_i} \quad \text{and} \quad I_o = -\frac{V_o}{R_L}$$

The minus sign associated with the output equation is simply there to indicate that the polarity of the output voltage is determined by an output current having the opposite direction. By definition, the input and output currents have a direction entering the two-port configuration.

Substituting into Eq. (5.84) then results in

$$A_{i_L} = \frac{I_o}{I_i} = \frac{-\dfrac{V_o}{R_L}}{\dfrac{V_i}{Z_i}} = -\frac{V_o}{V_i} \cdot \frac{Z_i}{R_L}$$

and the following important equation:

$$A_{i_L} = -A_{v_L}\frac{Z_i}{R_L} \tag{5.85}$$

The value of $R_L$ is defined by the location of $V_o$ and $I_o$.

To demonstrate the validity of Eq. (5.82), consider the voltage-divider bias configuration of Fig. 5.28.

Using the results of Example 5.2, we find

$$I_i = \frac{V_i}{Z_i} = \frac{V_i}{1.35\,\text{k}\Omega} \text{ and } I_o = -\frac{V_o}{R_L} = -\frac{V_o}{6.8\,\text{k}\Omega}$$

so that

$$A_{i_L} = \frac{I_o}{I_i} = \frac{\left(-\dfrac{V_o}{6.8\,\text{k}\Omega}\right)}{\dfrac{V_i}{1.35\,\text{k}\Omega}} = -\left(\frac{V_o}{V_i}\right)\left(\frac{1.35\,\text{k}\Omega}{6.8\,\text{k}\Omega}\right)$$

$$= -(-368.76)\left(\frac{1.35\,\text{k}\Omega}{6.8\,\text{k}\Omega}\right) = \mathbf{73.2}$$

Using Eq. 5.82:

$$A_{i_L} = -A_{v_L}\frac{Z_i}{R_L} = -(-368.76)\left(\frac{1.35\,\text{k}\Omega}{6.8\,\text{k}\Omega}\right) = \mathbf{73.2}$$

which has the same format as the resulting equation above and the same result.

The solution to the current gain in terms of the network parameters will be more complicated for some configurations if a solution is desired in terms of the network parameters. However, if a numerical solution is all that is desired, it is simply a matter of substituting the value of the three parameters from an analysis of the voltage gain.

As a second example, consider the common-base bias configuration of Section 5.9. In this case the voltage gain is

$$A_{v_L} \cong \frac{R_C}{r_e}$$

and the input impedance is

$$Z_i \cong R_E \| r_e \cong r_e$$

with $R_L$ defined as $R_C$ due to the location of $I_o$.

The result is the following:

$$A_{i_L} = -A_{v_L}\frac{Z_i}{R_L} = \left(-\frac{\cancel{R_C}}{\cancel{r_e}}\right)\left(\frac{\cancel{r_e}}{\cancel{R_C}}\right) \cong -1$$

which agrees with the solution of that section because $I_c \cong I_e$. Note, in this case, that the output current has the opposite direction to that appearing in the networks of that section due to the minus sign.

## 5.14 SUMMARY TABLES

The last few sections have included a number of derivations for unloaded and loaded BJT configurations. The material is so extensive that it seemed appropriate to review most of the conclusions for the various configurations in summary tables for quick comparisons. Although the equations using the hybrid parameters have not been discussed in detail at this point, they are included to make the tables complete. The use of hybrid parameters will be considered in a later section of this chapter. In each case the waveforms included demonstrate the phase relationship between input and output voltages. They also reveal the relative magnitude of the voltages at the input and output terminals.

Table 5.1 is for the unloaded situation, whereas Table 5.2 includes the effect of $R_s$ and $R_L$.

## 5.15 TWO-PORT SYSTEMS APPROACH

In the design process, it is often necessary to work with the terminal characteristics of a device rather then the individual components of the system. In other words, the designer is handed a packaged product with a list of data regarding its characteristics but has no access to the internal construction. This section will relate the important parameters determined for a number of configurations in the previous sections to the important parameters of this packaged system. The result will be an understanding of how each parameter of the

**TABLE 5.1**

*Unloaded BJT Transistor Amplifiers*

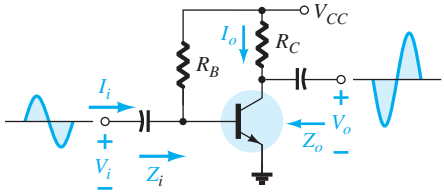
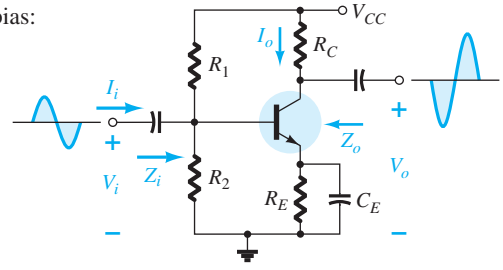
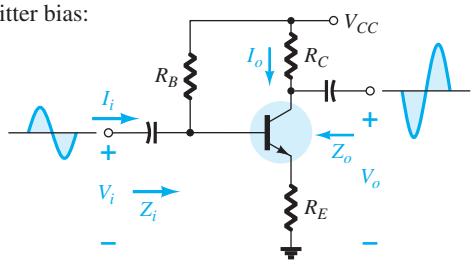
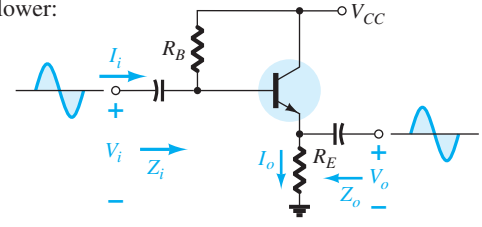
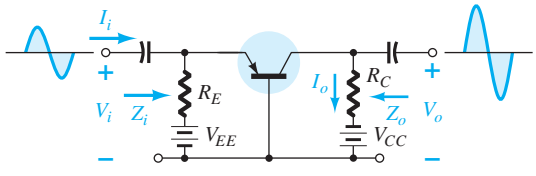
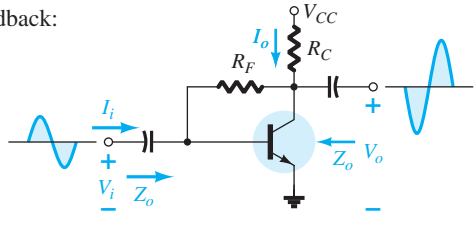
| Configuration | $Z_i$ | $Z_o$ | $A_v$ | $A_i$ |
|---|---|---|---|---|
| Fixed-bias:  | Medium (1 kΩ)<br>$= \boxed{R_B \| \beta r_e}$<br>$\cong \boxed{\beta r_e}$<br>$(R_B \geq 10\beta r_e)$ | Medium (2 kΩ)<br>$= \boxed{R_C \| r_o}$<br>$\cong \boxed{R_C}$<br>$(r_o \geq 10R_C)$ | High (−200)<br>$= \boxed{-\frac{(R_C \| r_o)}{r_e}}$<br>$\cong \boxed{-\frac{R_C}{r_e}}$<br>$(r_o \geq 10R_C)$ | High (100)<br>$= \boxed{\frac{\beta R_B r_o}{(r_o + R_C)(R_B + \beta r_e)}}$<br>$\cong \boxed{\beta}$<br>$(r_o \geq 10R_C,$<br>$R_B \geq 10\beta r_e)$ |
| Voltage-divider bias:  | Medium (1 kΩ)<br>$= \boxed{R_1 \| R_2 \| \beta r_e}$ | Medium (2 kΩ)<br>$= \boxed{R_C \| r_o}$<br>$\cong \boxed{R_C}$<br>$(r_o \geq 10R_C)$ | High (−200)<br>$= \boxed{-\frac{R_C \| r_o}{r_e}}$<br>$\cong \boxed{-\frac{R_C}{r_e}}$<br>$(r_o \geq 10R_C)$ | High (50)<br>$= \boxed{\frac{\beta(R_1 \| R_2) r_o}{(r_o + R_C)(R_1 \| R_2 + \beta r_e)}}$<br>$\cong \boxed{\frac{\beta(R_1 \| R_2)}{R_1 \| R_2 + \beta r_e}}$<br>$(r_o \geq 10R_C)$ |
| Unbypassed emitter bias:  | High (100 kΩ)<br>$= \boxed{R_B \| Z_b}$<br>$Z_b \cong \beta(r_e + R_E)$<br>$\cong \boxed{R_B \| \beta R_E}$<br>$(R_E \gg r_e)$ | Medium (2 kΩ)<br>$= \boxed{R_C}$<br>(any level of $r_o$) | Low (−5)<br>$= \boxed{-\frac{R_C}{r_e + R_E}}$<br>$\cong \boxed{-\frac{R_C}{R_E}}$<br>$(R_E \gg r_e)$ | High (50)<br>$\cong \boxed{-\frac{\beta R_B}{R_B + Z_b}}$ |
| Emitter-follower:  | High (100 kΩ)<br>$= \boxed{R_B \| Z_b}$<br>$Z_b \cong \beta(r_e + R_E)$<br>$\cong \boxed{R_B \| \beta R_E}$<br>$(R_E \gg r_e)$ | Low (20 Ω)<br>$= \boxed{R_E \| r_e}$<br>$\cong \boxed{r_e}$<br>$(R_E \gg r_e)$ | Low ($\cong$1)<br>$= \boxed{\frac{R_E}{R_E + r_e}}$<br>$\cong \boxed{1}$ | High (−50)<br>$\cong \boxed{-\frac{\beta R_B}{R_B + Z_b}}$ |
| Common-base:  | Low (20 Ω)<br>$= \boxed{R_E \| r_e}$<br>$\cong \boxed{r_e}$<br>$(R_E \gg r_e)$ | Medium (2 kΩ)<br>$= \boxed{R_C}$ | High (200)<br>$\cong \boxed{\frac{R_C}{r_e}}$ | Low (−1)<br>$\cong \boxed{-1}$ |
| Collector feedback:  | Medium (1 kΩ)<br>$= \boxed{\frac{r_e}{\frac{1}{\beta} + \frac{R_C}{R_F}}}$<br>$(r_o \geq 10R_C)$ | Medium (2 kΩ)<br>$\cong \boxed{R_C \| R_F}$<br>$(r_o \geq 10R_C)$ | High (−200)<br>$\cong \boxed{-\frac{R_C}{r_e}}$<br>$(r_o \geq 10R_C)$<br>$(R_F \gg R_C)$ | High (50)<br>$= \boxed{\frac{\beta R_F}{R_F + \beta R_C}}$<br>$\cong \boxed{\frac{R_F}{R_C}}$ |

**TABLE 5.2**

*BJT Transistor Amplifiers Including the Effect of $R_s$ and $R_L$*

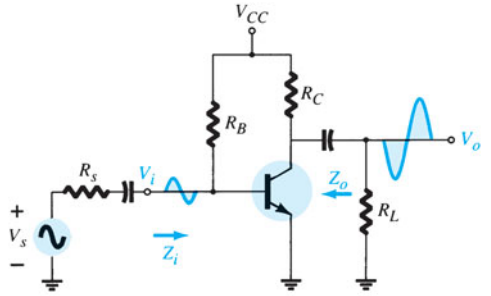
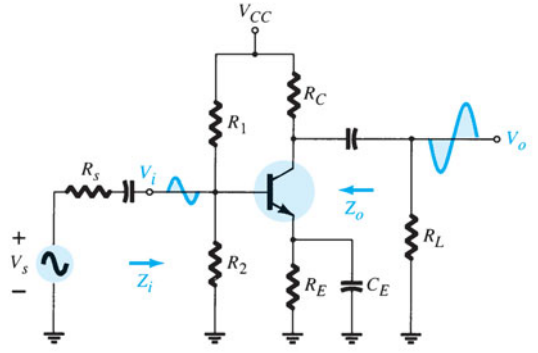
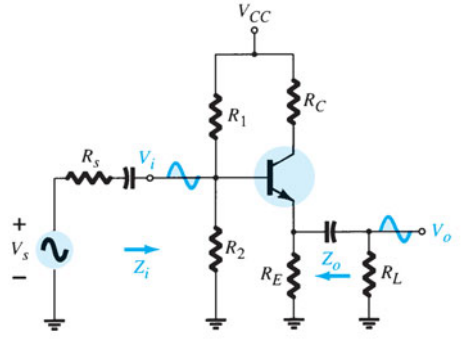
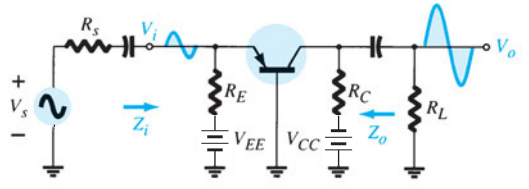
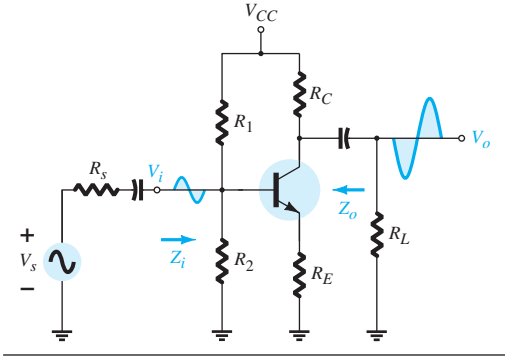
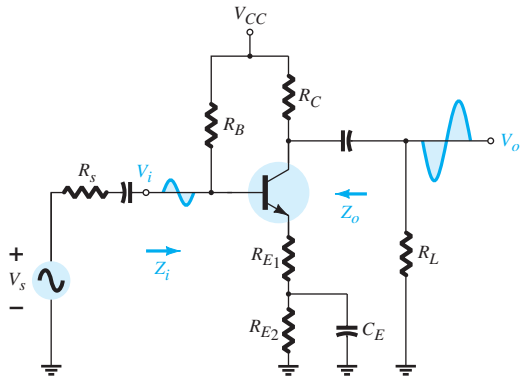
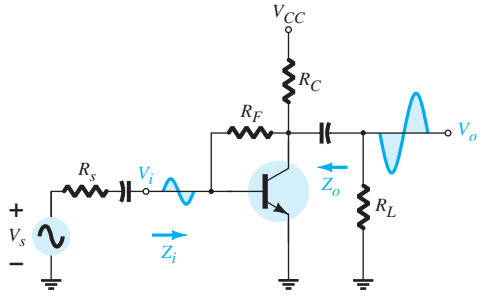
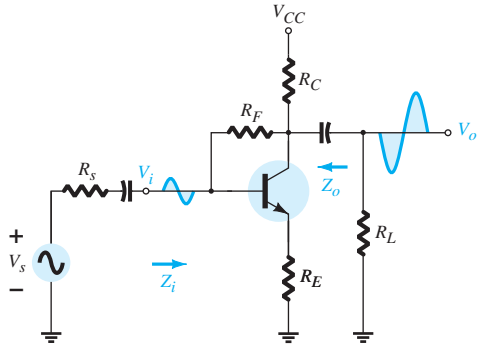
| Configuration | $A_{v_L} = V_o/V_i$ | $Z_i$ | $Z_o$ |
|---|---|---|---|
|  | $\dfrac{-(R_L \| R_C)}{r_e}$ | $R_B \| \beta r_e$ | $R_C$ |
| | Including $r_o$: $\dfrac{-(R_L \| R_C \| r_o)}{r_e}$ | $R_B \| \beta r_e$ | $R_C \| r_o$ |
|  | $\dfrac{-(R_L \| R_C)}{r_e}$ | $R_1 \| R_2 \| \beta r_e$ | $R_C$ |
| | Including $r_o$: $\dfrac{-(R_L \| R_C \| r_o)}{r_e}$ | $R_1 \| R_2 \| \beta r_e$ | $R_C \| r_o$ |
|  | $\cong 1$ | $R'_E = R_L \| R_E$<br>$R_1 \| R_2 \| \beta(r_e + R'_E)$ | $R'_s = R_s \| R_1 \| R_2$<br>$R_E \| \left(\dfrac{R'_s}{\beta} + r_e\right)$ |
| | Including $r_o$: $\cong 1$ | $R_1 \| R_2 \| \beta(r_e + R'_E)$ | $R_E \| \left(\dfrac{R'_s}{\beta} + r_e\right)$ |
|  | $\cong \dfrac{-(R_L \| R_C)}{r_e}$ | $R_E \| r_e$ | $R_C$ |
| | Including $r_o$: $\cong \dfrac{-(R_L \| R_C \| r_o)}{r_e}$ | $R_E \| r_e$ | $R_C \| r_o$ |
|  | $\dfrac{-(R_L \| R_C)}{R_E}$ | $R_1 \| R_2 \| \beta(r_e + R_E)$ | $R_C$ |
| | Including $r_o$: $\dfrac{-(R_L \| R_C)}{R_E}$ | $R_1 \| R_2 \| \beta(r_e + R_e)$ | $\cong R_C$ |

**TABLE 5.2 *(Continued)***

*BJT Transistor Amplifiers Including the Effect of $R_s$ and $R_L$*

| Configuration | $A_{v_L} = V_o/V_i$ | $Z_i$ | $Z_o$ |
|---|---|---|---|
|  | $\dfrac{-(R_L \| R_C)}{R_{E_1}}$ | $R_B \| \beta(r_e + R_{E_1})$ | $R_C$ |
| | Including $r_o$: $\dfrac{-(R_L \| R_C)}{R_{E_t}}$ | $R_B \| \beta(r_e + R_E)$ | $\cong R_C$ |
|  | $\dfrac{-(R_L \| R_C)}{r_e}$ | $\beta r_e \| \dfrac{R_F}{\lvert A_v \rvert}$ | $R_C$ |
| | Including $r_o$: $\dfrac{-(R_L \| R_C \| r_o)}{r_e}$ | $\beta r_e \| \dfrac{R_F}{\lvert A_v \rvert}$ | $R_C \| R_F \| r_o$ |
|  | $\dfrac{-(R_L \| R_C)}{R_E}$ | $\beta R_E \| \dfrac{R_F}{\lvert A_v \rvert}$ | $\cong R_C \| R_F$ |
| | Including $r_o$: $\cong \dfrac{-(R_L \| R_C)}{R_E}$ | $\cong \beta R_E \| \dfrac{R_F}{\lvert A_v \rvert}$ | $\cong R_C \| R_F$ |

packaged system relates to the actual amplifier or network. The system of Fig. 5.61 is called a two-port system because there are two sets of terminals—one at the input and the other at the output. At this point it is particularly important to realize that

***the data surrounding a packaged system is the no-load data.***

This should be fairly obvious because the load has not been applied, nor does it come with the load attached to the package.

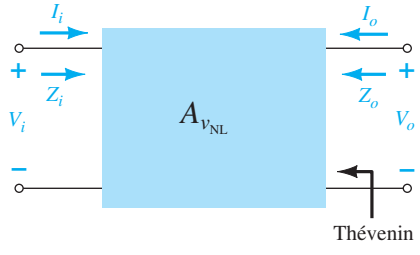



**FIG. 5.61**

*Two-port system.*

For the two-port system of Fig. 5.61 the polarity of the voltages and the direction of the currents are as defined. If the currents have a different direction or the voltages have a different polarity from that appearing in Fig. 5.61, a negative sign must be applied. Note again the use of the label $A_{v_{NL}}$ to indicate that the provided voltage gain will be the no-load value.

For amplifiers the parameters of importance have been sketched within the boundaries of the two-port system as shown in Fig. 5.62. The input and output resistance of a packaged amplifier are normally provided along with the no-load gain. They can then be inserted as shown in Fig. 5.62 to represent the seated package.

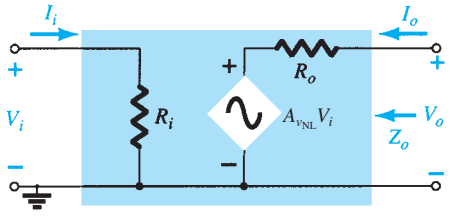



**FIG. 5.62**

*Substituting the internal elements for the two-port system of Fig. 5.61.*

For the no-load situation the output voltage is

$$V_o = A_{v_{NL}} V_i \tag{5.86}$$

due to the fact that $I = 0A$, resulting in $I_o R_o = 0V$.

The output resistance is defined by $V_i = 0V$. Under such conditions the quantity $A_{v_{NL}} V_i$ is zero volts also and can be replaced by a short-circuit equivalent. The result is

$$Z_o = R_o \tag{5.87}$$

Finally, the input impedance $Z_i$ simply relates the applied voltage to the resulting input current and

$$Z_i = R_i \tag{5.88}$$

For the no-load situation, the current gain is undefined because the load current is zero. There is, however, a no-load voltage gain equal to $A_{v_{NL}}$.

The effect of applying a load to a two-port system will result in the configuration of Fig. 5.63. Ideally, all the parameters of the model are unaffected by changing loads and levels of source resistance. However, for some transistor configurations the applied load can affect the input resistance, whereas for others the output resistance can be affected by the source resistance. In all cases, however, by simple definition, the no-load gain is unaffected by the application of any load. In any case, once $A_{v_{NL}}$, $R_i$, and $R_o$ are defined for a particular configuration, the equations about to be derived can be employed.

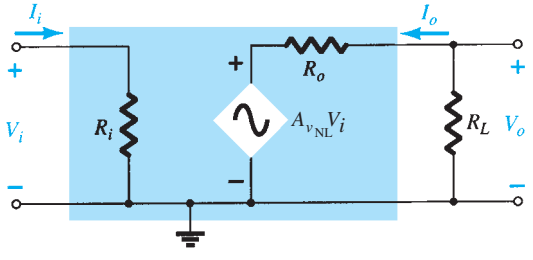



**FIG. 5.63**

*Applying a load to the two-port system of Fig. 5.62.*

Applying the voltage-divider rule to the output circuit results in

$$V_o = \frac{R_L A_{v_{NL}} V_i}{R_L + R_o}$$

and

$$\boxed{A_{v_L} = \frac{V_o}{V_i} = \frac{R_L}{R_L + R_o} A_{v_{NL}}} \qquad \textbf{(5.89)}$$

Because the ratio $R_L/(R_L + R_o)$ is always less than 1, we have further evidence that the loaded voltage gain of an amplifier is always less than the no-load level.

The current gain is then determined by

$$A_{i_L} = \frac{I_o}{I_i} = \frac{-V_o/R_L}{V_i/Z_i} = -\frac{V_o}{V_i}\frac{Z_i}{R_L}$$

and

$$\boxed{A_{i_L} = -A_{v_L}\frac{Z_i}{R_L}} \qquad \textbf{(5.90)}$$

as obtained earlier. In general, therefore, the current gain can be obtained from the voltage gain and impedance parameters $Z_i$ and $R_L$. The next example will demonstrate the usefulness and validity of Eqs. (5.89) and (5.90).

Our attention will now turn to the input side of the two-port system and the effect of an internal source resistance on the gain of an amplifier. In Fig. 5.64, a source with an internal resistance has been applied to the basic two-port system. The definitions of $Z_i$ and $A_{v_{NL}}$ are such that:

***The parameters $Z_i$ and $A_{v_{NL}}$ of a two-port system are unaffected by the internal resistance of the applied source.***

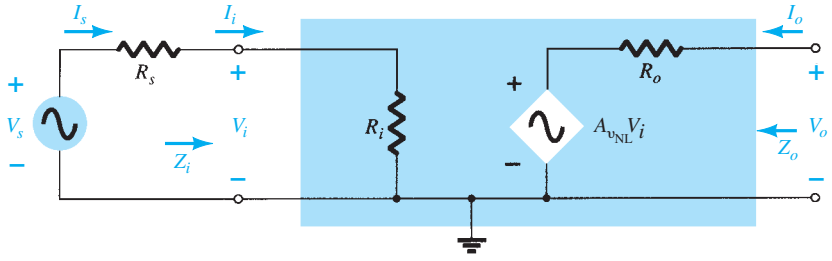



**FIG. 5.64**

*Including the effects of the source resistance $R_s$.*

However:

***The output impedance may be affected by the magnitude of $R_s$.***

The fraction of the applied signal reaching the input terminals of the amplifier of Fig. 5.64 is determined by the voltage-divider rule. That is,

$$\boxed{V_i = \frac{R_i V_s}{R_i + R_s}} \qquad \textbf{(5.91)}$$

Equation (5.91) clearly shows that the larger the magnitude of $R_s$, the lower is the voltage at the input terminals of the amplifier. In general, therefore, as mentioned earlier, for a particular amplifier, the larger the internal resistance of a signal source, the lower is the overall gain of the system.

For the two-port system of Fig. 5.64,

$$V_o = A_{v_{NL}} V_i$$

and

$$V_i = \frac{R_i V_s}{R_i + R_s}$$

so that $$V_o = A_{v_{NL}} \frac{R_i}{R_i + R_s} V_s$$

and $$\boxed{A_{v_s} = \frac{V_o}{V_s} = \frac{R_i}{R_i + R_s} A_{v_{NL}}} \tag{5.92}$$

The effects of $R_s$ and $R_L$ have now been demonstrated on an individual basis. The next natural question is how the presence of both factors in the same network will affect the total gain. In Fig. 5.65, a source with an internal resistance $R_s$ and a load $R_L$ have been applied to a two-port system for which the parameters $Z_i$, $A_{v_{NL}}$, and $Z_o$ have been specified. For the moment, let us assume that $Z_i$ and $Z_o$ are unaffected by $R_L$ and $R_s$, respectively.

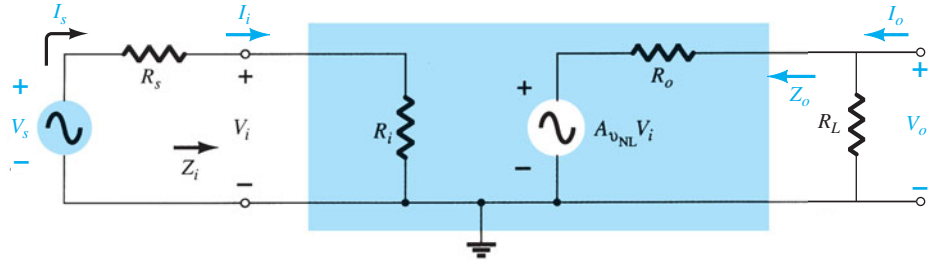



**FIG. 5.65**
*Considering the effects of $R_s$ and $R_L$ on the gain of an amplifier.*

At the input side we find

$$\text{Eq. (5.91):} \quad V_i = \frac{R_i V_s}{R_i + R_s}$$

or $$\boxed{\frac{V_i}{V_s} = \frac{R_i}{R_i + R_s}} \tag{5.93}$$

and at the output side,

$$V_o = \frac{R_L}{R_L + R_o} A_{v_{NL}} V_i$$

or $$A_{v_L} = \frac{V_o}{V_i} = \frac{R_L A_{v_{NL}}}{R_L + R_o} = \frac{R_L}{R_L + R_o} A_{v_{NL}} \tag{5.94}$$

For the total gain $A_{v_s} = V_o/V_s$, the following mathematical steps can be performed:

$$\boxed{A_{v_s} = \frac{V_o}{V_s} = \frac{V_o}{V_i} \cdot \frac{V_i}{V_s}} \tag{5.95}$$

and substituting Eqs. (5.93) and (5.94) results in

$$\boxed{A_{v_s} = \frac{V_o}{V_s} = \frac{R_i}{R_i + R_s} \cdot \frac{R_L}{R_L + R_o} A_{v_{NL}}} \tag{5.96}$$

Because $I_i = V_i/R_i$, as before,

$$\boxed{A_{i_L} = -A_{v_L} \frac{R_i}{R_L}} \tag{5.97}$$

or, using $I_s = V_s/(R_s + R_i)$,

$$\boxed{A_{i_s} = -A_{v_s} \frac{R_s + R_i}{R_L}} \tag{5.98}$$

However, $I_i = I_s$, so Eqs. (5.97) and (5.98) generate the same result. Equation (5.96) clearly reveals that both the source and the load resistance will reduce the overall gain of the system.

The two reduction factors of Eq. (5.96) form a product that has to be carefully considered in any design procedure. It is not sufficient to ensure that $R_s$ is relatively small if the effect of the magnitude of $R_L$ is ignored. For instance, in Eq. (5.96), if the first factor is 0.9 and the second factor is 0.2, the product of the two results in an overall reduction factor equal to $(0.9)(0.2) = 0.18$, which is close to the lower factor. The effect of the excellent 0.9 level was completely wiped out by the significantly lower second multiplier. If both were 0.9-level factors, the net result would be $(0.9)(0.9) = 0.81$, which is still quite high. Even if the first were 0.9 and the second 0.7, the net result of 0.63 would still be respectable. In general, therefore, for good overall gain the effects of $R_s$ and $R_L$ must be evaluated individually and as a product.

**EXAMPLE 5.12** Determine $A_{v_L}$ and $A_{v_s}$ for the network of Example 5.11 and compare solutions. Example 5.1 showed that $A_{v_{NL}} = -280$, $Z_i = 1.07\,\text{k}\Omega$, and $Z_o = 3\,\text{k}\Omega$. In Example 5.11, $R_L = 4.7\,\text{k}\Omega$ and $R_s = 0.3\,\text{k}\Omega$.

***Solution:***

a. Eq. (5.89): $A_{v_L} = \dfrac{R_L}{R_L + R_o} A_{v_{NL}}$

$$= \frac{4.7\,\text{k}\Omega}{4.7\,\text{k}\Omega + 3\,\text{k}\Omega}(-280.11)$$

$$= \mathbf{-170.98}$$

as in Example 5.11.

b. Eq. (5.96): $A_{v_s} = \dfrac{R_i}{R_i + R_s} \cdot \dfrac{R_L}{R_L + R_o} A_{v_{NL}}$

$$= \frac{1.07\,\text{k}\Omega}{1.07\,\text{k}\Omega + 0.3\,\text{k}\Omega} \cdot \frac{4.7\,\text{k}\Omega}{4.7\,\text{k}\Omega + 3\,\text{k}\Omega}(-280.11)$$

$$= (0.781)(0.610)(-280.11)$$

$$= \mathbf{-133.45}$$

as in Example 5.11.

**EXAMPLE 5.13** Given the packaged (no-entry-possible) amplifier of Fig. 5.66:

a. Determine the gain $A_{v_L}$ and compare it to the no-load value with $R_L = 1.2\,\text{k}\Omega$.
b. Repeat part (a) with $R_L = 5.6\,\text{k}\Omega$ and compare solutions.
c. Determine $A_{v_s}$ with $R_L = 1.2\,\text{k}\Omega$.
d. Find the current gain $A_i = \dfrac{I_o}{I_i} = \dfrac{I_o}{I_s}$ with $R_L = 5.6\,\text{k}\Omega$.

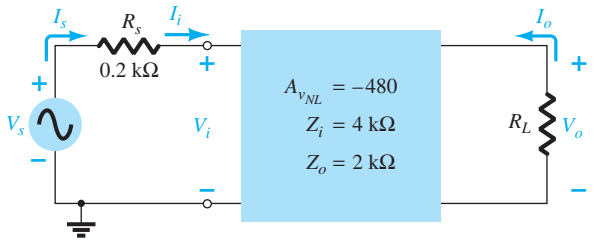



**FIG. 5.66**
*Amplifier for Example 5.13.*

***Solution:***

a. Eq. (5.89): $A_{v_L} = \dfrac{R_L}{R_L + R_o} A_{v_{NL}}$

$$= \frac{1.2\,\text{k}\Omega}{1.2\,\text{k}\Omega + 2\,\text{k}\Omega}(-480) = (0.375)(-480)$$

$$= \mathbf{-180}$$

which is a dramatic drop from the no-load value.

b. Eq. (5.89): $A_{v_L} = \dfrac{R_L}{R_L + R_o} A_{v_{NL}}$

$$= \frac{5.6\,\text{k}\Omega}{5.6\,\text{k}\Omega + 2\,\text{k}\Omega}(-480) = (0.737)(-480)$$

$$= \mathbf{-353.76}$$

which clearly reveals that the larger the load resistor, the better is the gain.

c. Eq. (5.96): $A_{v_s} = \dfrac{R_i}{R_i + R_s} \cdot \dfrac{R_L}{R_L + R_o} A_{v_{NL}}$

$$= \frac{4\,\text{k}\Omega}{4\,\text{k}\Omega + 0.2\,\text{k}\Omega} \cdot \frac{1.2\,\text{k}\Omega}{1.2\,\text{k}\Omega + 2\,\text{k}\Omega}(-480)$$

$$= (0.952)(0.375)(-480)$$

$$= \mathbf{-171.36}$$

which is fairly close to the loaded gain $A_v$ because the input impedance is considerably more than the source resistance. In other words, the source resistance is relatively small compared to the input impedance of the amplifier.

d. $A_{i_L} = \dfrac{I_o}{I_i} = \dfrac{I_o}{I_s} = -A_{v_L}\dfrac{Z_i}{R_L}$

$$= -(-353.76)\left(\frac{4\,\text{k}\Omega}{5.6\,\text{k}\Omega}\right) = -(-353.76)(0.714)$$

$$= \mathbf{252.6}$$

It is important to realize that when using the two-port equations in some configurations the input impedance is sensitive to the applied load (such as the emitter-follower and collector feedback) and in some the output impedance is sensitive to the applied source resistance (such as the emitter-follower). In such cases the no-load parameters for $Z_i$ and $Z_o$ have to first be calculated before substituting into the two-port equations. For most packaged systems such as op-amps this sensitivity of the input and output parameters to the applied load or source resistance is minimized to eliminate the need to be concerned about changes from the no-load levels when using the two-port equations.

## 5.16 CASCADED SYSTEMS

The two-port systems approach is particularly useful for cascaded systems such as that appearing in Fig. 5.67, where $A_{v_1}, A_{v_2}, A_{v_3}$, and so on, are the voltage gains of each stage *under loaded conditions.* That is, $A_{v_1}$ is determined with the *input impedance to* $A_{v_2}$ *acting as the load on* $A_{v_1}$. For $A_{v_2}$, $A_{v_1}$ will determine the signal strength and source impedance at the input to $A_{v_2}$. The total gain of the system is then determined by the product of the individual gains as follows:

$$A_{v_T} = A_{v_1} \cdot A_{v_2} \cdot A_{v_3} \cdots \tag{5.99}$$

and the total current gain is given by

$$A_{i_T} = -A_{v_T}\frac{Z_{i_1}}{R_L} \tag{5.100}$$

No matter how perfect the system design, the application of a succeeding stage or load to a two-port system will affect the voltage gain. Therefore, there is no possibility of a situation where $A_{v_1}$, $A_{v_2}$, and so on, of Fig. 5.67 are simply the no-load values. The no-load parameters can be used to determine the loaded gains of each stage, but Eq. (5.99) requires the loaded values. The load on stage 1 is $Z_{i_2}$, on stage 2 $Z_{i_3}$, on stage 3 $Z_{i_n}$, and so on.

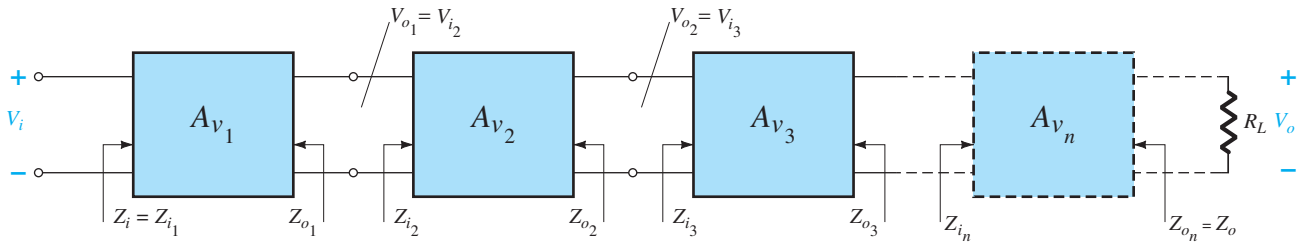



**FIG. 5.67**
*Cascaded system.*

**EXAMPLE 5.14** The two-stage system of Fig. 5.68 employs a transistor emitter-follower configuration prior to a common-base configuration to ensure that the maximum percentage of the applied signal appears at the input terminals of the common-base amplifier. In Fig. 5.68, the no-load values are provided for each system, with the exception of $Z_i$ and $Z_o$ for the emitter-follower, which are the loaded values. For the configuration of Fig. 5.68, determine:

a. The loaded gain for each stage.
b. The total gain for the system, $A_v$ and $A_{v_s}$.
c. The total current gain for the system.
d. The total gain for the system if the emitter-follower configuration were removed.

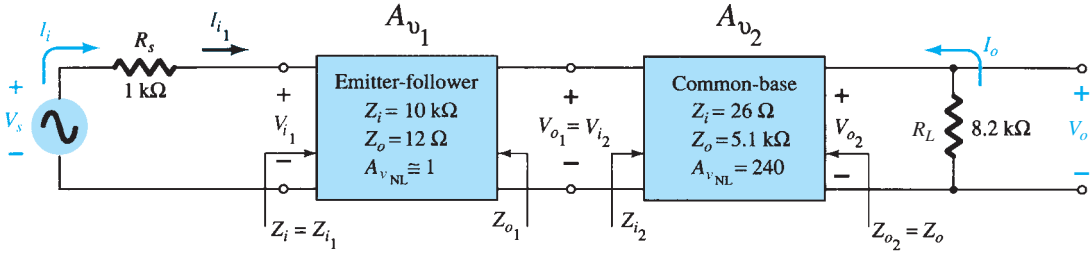



**FIG. 5.68**
*Example 5.14.*

***Solution:***

a. For the emitter-follower configuration, the loaded gain is (by Eq. (5.94))

$$V_{o_1} = \frac{Z_{i_2}}{Z_{i_2} + Z_{o_1}} A_{v_{NL}} V_{i_1} = \frac{26\ \Omega}{26\ \Omega + 12\ \Omega}(1)\, V_{i_1} = 0.684\, V_{i_1}$$

and $$A_{V_i} = \frac{V_{o_1}}{V_{i_1}} = \mathbf{0.684}$$

For the common-base configuration,

$$V_{o_2} = \frac{R_L}{R_L + R_{o_2}} A_{v_{NL}} V_{i_2} = \frac{8.2\ \text{k}\Omega}{8.2\ \text{k}\Omega + 5.1\ \text{k}\Omega}(240)\, V_{i_2} = 147.97\, V_{i_2}$$

and $$A_{v_2} = \frac{V_{o_2}}{V_{i_2}} = \mathbf{147.97}$$

b. Eq. (5.99): $A_{v_T} = A_{v_1} A_{v_2}$
$= (0.684)(147.97)$
$= \mathbf{101.20}$

Eq. (5.91): $$A_{v_s} = \frac{Z_{i_1}}{Z_{i_1} + R_s} A_{v_T} = \frac{(10\,\text{k}\Omega)(101.20)}{10\,\text{k}\Omega + 1\,\text{k}\Omega}$$
$$= \mathbf{92}$$

c. Eq. (5.100): $$A_{i_T} = -A_{v_T}\frac{Z_{i_1}}{R_L} = -(101.20)\left(\frac{10\,\text{k}\Omega}{8.2\,\text{k}\Omega}\right)$$
$$= \mathbf{-123.41}$$

d. Eq. (5.91): $$V_i = \frac{Z_{i_{CB}}}{Z_{i_{CB}} + R_s} V_s = \frac{26\ \Omega}{26\ \Omega + 1\,\text{k}\Omega} V_s = 0.025\ V_s$$

and $$\frac{V_i}{V_s} = 0.025 \quad \text{with} \quad \frac{V_o}{V_i} = 147.97 \quad \text{from above}$$

and $$A_{v_s} = \frac{V_o}{V_s} = \frac{V_i}{V_s} \cdot \frac{V_o}{V_i} = (0.025)(147.97) = \mathbf{3.7}$$

In total, therefore, the gain is about 25 times greater with the emitter-follower configuration to draw the signal to the amplifier stages. Note, however, that it is also important that the output impedance of the first stage is relatively close to the input impedance of the second stage, otherwise the signal would have been "lost" again by the voltage-divider action.

## *RC*-Coupled BJT Amplifiers

One popular connection of amplifier stages is the *RC*-coupled variety shown in Fig. 5.69 in the next example. The name is derived from the capacitive coupling capacitor $C_c$ and the fact that the load on the first stage is an *RC* combination. The coupling capacitor isolates the two stages from a dc viewpoint but acts as a short-circuit equivalent for the ac response. The input impedance of the second stage acts as a load on the first stage, permitting the same approach to the analysis as described in the last two sections.

### EXAMPLE 5.15

a. Calculate the no-load voltage gain and output voltage of the *RC*-coupled transistor amplifiers of Fig. 5.69.
b. Calculate the overall gain and output voltage if a 4.7 kΩ load is applied to the second stage, and compare to the results of part (a).
c. Calculate the input impedance of the first stage and the output impedance of the second stage.

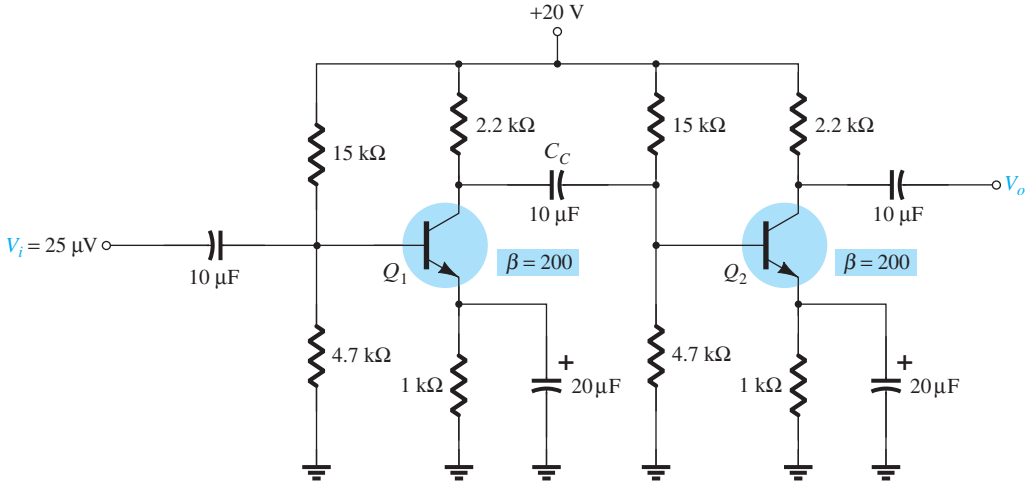



**FIG. 5.69**
*RC-coupled BJT amplifier for Example 5.15.*

### Solution:

a. The dc bias analysis results in the following for each transistor:

$$V_B = 4.8\ \text{V}, \quad V_E = 4.1\ \text{V}, \quad V_C = 11\ \text{V}, \quad I_E = 4.1\ \text{mA}$$

At the bias point,

$$r_e = \frac{26\text{ mV}}{I_E} = \frac{26\text{ mV}}{4.1\text{ mA}} = 6.34\ \Omega$$

The loading of the second stage is

$$Z_{i_2} = R_1 \| R_2 \| \beta r_e$$

which results in the following gain for the first stage:

$$A_{v_1} = -\frac{R_C \| (R_1 \| R_2 \| \beta r_e)}{r_e}$$

$$= -\frac{(2.2\text{ k}\Omega) \| [15\text{ k}\Omega \| 4.7\text{ k}\Omega \| (200)(6.34\ \Omega)]}{6.34\ \Omega}$$

$$= -\frac{659.2\ \Omega}{6.34\ \Omega} = -104$$

For the unloaded second stage the gain is

$$A_{v_{2(\text{NL})}} = -\frac{R_C}{r_e} = -\frac{2.2\text{ k}\Omega}{6.34\ \Omega} = -347$$

resulting in an overall gain of

$$A_{v_{T(\text{NL})}} = A_{v_1} A_{v_{2(\text{NL})}} = (-104)(-347) \cong \mathbf{36.1 \times 10^3}$$

The output voltage is then

$$V_o = A_{v_{T(\text{NL})}} V_i = (36.1 \times 10^3)(25\ \mu\text{V}) \cong \mathbf{902.5\text{ mV}}$$

b. The overall gain with the 10-kΩ load applied is

$$A_{v_T} = \frac{V_o}{V_i} = \frac{R_L}{R_L + Z_o} A_{v_{T(\text{NL})}} = \frac{4.7\text{ k}\Omega}{4.7\text{ k}\Omega + 2.2\text{ k}\Omega}(36.1 \times 10^3) \cong \mathbf{24.6 \times 10^3}$$

which is considerably less than the unloaded gain because $R_L$ is relatively close to $R_C$.

$$V_o = A_{v_T} V_i$$

$$= (24.6 \times 10^3)(25\ \mu\text{V})$$

$$= \mathbf{615\text{ mV}}$$

c. The input impedance of the first stage is

$$Z_{i_1} = R_1 \| R_2 \| \beta r_e = 4.7\text{ k}\Omega \| 15\text{ k}\Omega \| (200)(6.34\ \Omega) = \mathbf{0.94\text{ k}\Omega}$$

whereas the output impedance for the second stage is

$$Z_{o_2} = R_C = \mathbf{2.2\text{ k}\Omega}$$

## Cascode Connection

The cascode configuration has one of two configurations. In each case the collector of the leading transistor is connected to the emitter of the following transistor. One possible arrangement appears in Fig. 5.70; the second is shown in Fig. 5.71 in the following example.

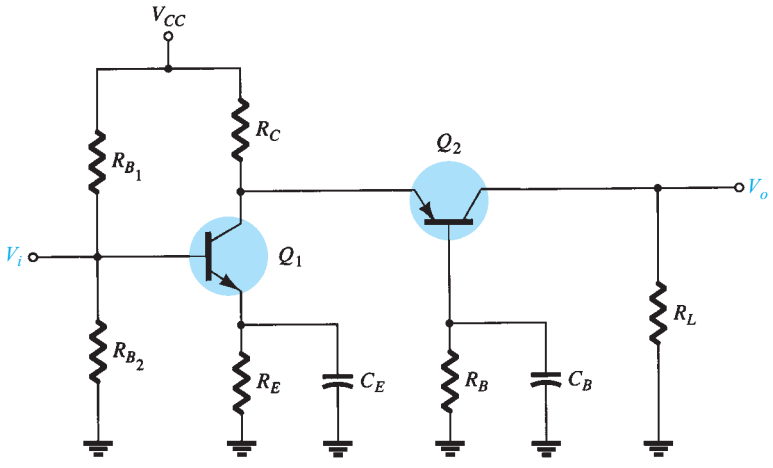



**FIG. 5.70**
*Cascode configuration.*

The arrangements provide a relatively high-input impedance with low voltage gain for the first stage to ensure the input Miller capacitance (to be discussed in Section 9.9) is at a minimum, whereas the following CB stage provides an excellent high-frequency response.

**EXAMPLE 5.16** Calculate the no-load voltage gain for the cascode configuration of Fig. 5.71.

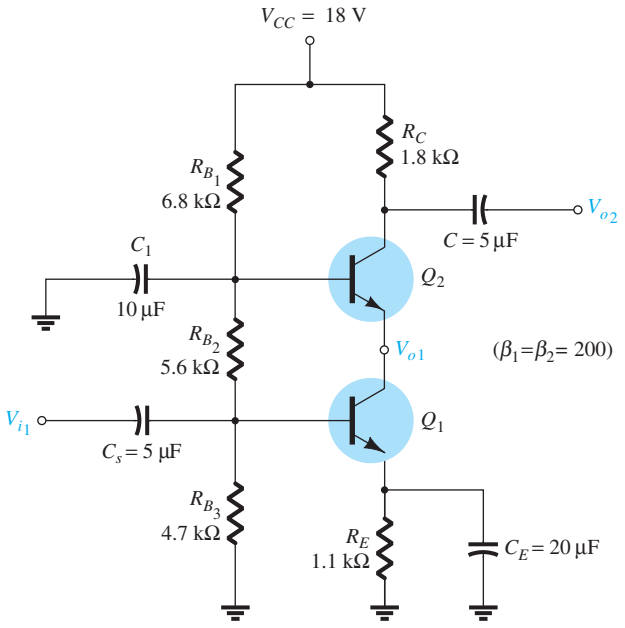



**FIG. 5.71**
*Practical cascode circuit for Example 5.16.*

***Solution:*** The dc analysis results in

$$V_{B_1} = 4.9\text{ V}, \quad V_{B_2} = 10.8\text{ V}, \quad I_{C_1} \cong I_{C_2} = 3.8\text{ mA}$$

because $I_{E_1} \cong I_{E_2}$ the dynamic resistance for each transistor is

$$r_e = \frac{26\text{ mV}}{I_E} \cong \frac{26\text{ mV}}{3.8\text{ mA}} = 6.8\ \Omega$$

The loading on the transistor $Q_1$ is the input impedance of the $Q_2$ transistor in the CB configuration as shown by $r_e$ in Fig 5.72.

The result is the replacement of $R_C$ in the basic no-load equation for the gain of the CB configuration, with the input impedance of a CB configuration as follows:

$$A_{v_1} = -\frac{R_C}{r_e} = -\frac{r_e}{r_e} = -1$$

with the voltage gain for the second stage (common base) of

$$A_{v_2} = \frac{R_C}{r_e} = \frac{1.8\text{ k}\Omega}{6.8\ \Omega} = 265$$

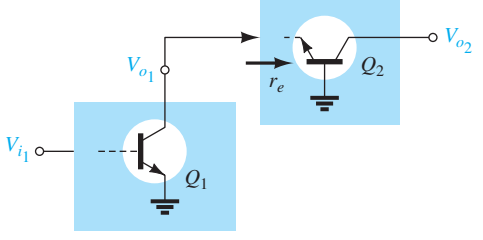



**FIG. 5.72**
*Defining the load of $Q_1$.*

The overall no-load gain is

$$A_{v_T} = A_{v_1}A_{v_2} = (-1)(265) = \mathbf{-265}$$

As expected, in Example 5.16, the CE stage provides a higher input impedance than can be expected from the CB stage. With a voltage gain of about 1 for the first stage, the Miller-effect input capacitance is kept quite low to support a good high-frequency response. A large voltage gain of 265 was provided by the CB stage to give the overall design a good input impedance level with desirable gain levels.

## 5.17 DARLINGTON CONNECTION

A very popular connection of two bipolar junction transistors for operation as one "super-beta" transistor is the Darlington connection shown in Fig. 5.73. The main feature of the Darlington connection is that the composite transistor acts as a single unit with a current gain that is the product of the current gains of the individual transistors. If the connection is made using two separate transistors having current gains of $\beta_1$ and $\beta_2$, the Darlington connection provides a current gain of

$$\beta_D = \beta_1\beta_2 \tag{5.101}$$

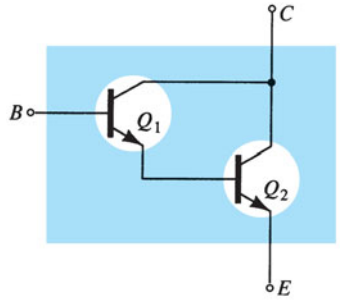



**FIG. 5.73**
*Darlington combination.*

The configuration was first introduced by Dr. Sidney Darlington in 1953. A short biography appears as Fig 5.74.

### Emitter-Follower Configuration

A Darlington amplifier used in an emitter-follower configuration appears in Fig. 5.75. The primary impact of using the Darlington configuration is an input impedance much larger than

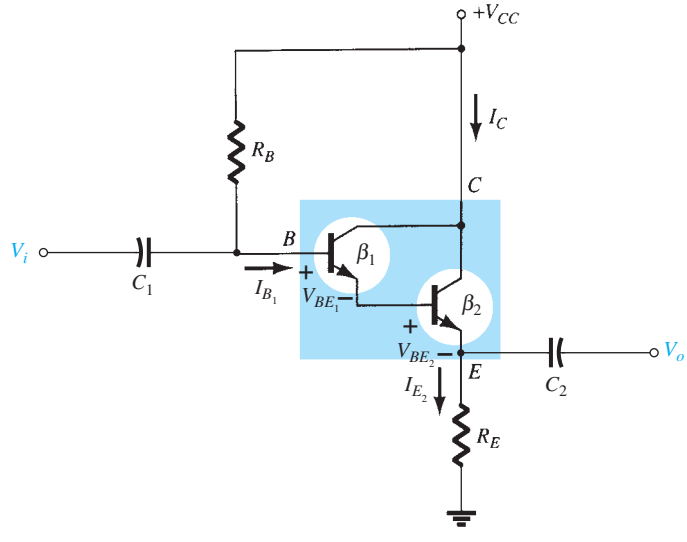
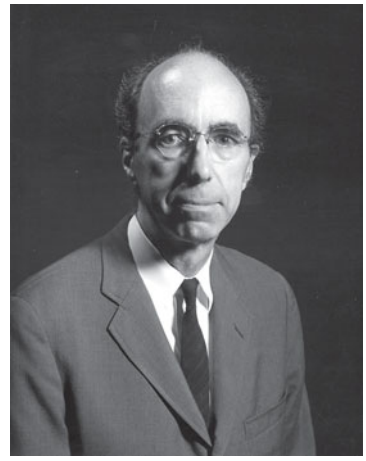



**FIG. 5.75**
*Emitter-follower configuration with a Darlington amplifier.*



**American** (Pittsburgh, PA; Exeter, NH) **(1906–1997)**

**Department Head at Bell Laboratories**
**Professor**, Department of Electrical and Computer Engineering, University of New Hampshire

Dr. Sidney Darlington earned his B.S. in physics at Harvard, his B.S. in electrical communication at MIT, and his Ph.D. at Columbia University. In 1929 he joined Bell Laboratories, where he was head of the Circuits and Control Department. During that period he became good friends with other important contributors such as Edward Norton and Hendrik Bode. A holder of 24 U.S. patents, he was awarded the Presidential Medal of Freedom, the highest civilian honor in the United States, in 1945 for his contributions to network design during World War II. An elected member of the National Academy of Engineering, he also received the IEEE Edison Medal in 1975 and the IEEE Medal of Honor in 1981. His U.S. patent 2 663 806 titled "Semiconductor Signal Translating Device" was issued on December 22, 1953, describing how two transistors could be constructed in the Darlington configuration on the same substrate—often looked upon as the beginnings of compound IC construction. Dr. Darlington was also responsible for the introduction and development of the Chirp technique, used throughout the world in waveguide transmission and radar systems. He is a primary contributor to the Bell Laboratories Command Guidance System that guides most of the rockets used today to place satellites in orbit. It uses a combination of radar tracking on the ground with inertial control in the rocket itself. Dr. Darlington was an avid outdoorsman as a hiker and member of the Appalachian Mountain Club. One of his proudest accomplishments was being able to climb Mt. Washington at the age of 80.

**FIG. 5.74**
*Sidney Darlington (Courtesy of AT&T Archives and History Center.)*

that obtained with a single-transistor network. The current gain is also larger, but the voltage gain for a single-transistor or Darlington configuration remains slightly less than one.

**DC Bias** The case current is determined using a modified version of Eq. 4.44. There are now two base-to-emitter voltage drops to include and the beta of a single transistor is replaced by the Darlington combination of Eq. 5.101.

$$I_{B_1} = \frac{V_{CC} - V_{BE_1} - V_{BE_2}}{R_B + \beta_D R_E} \tag{5.102}$$

The emitter current of $Q_1$ is equal to the base current of $Q_2$ so that

$$I_{E_2} = \beta_2 I_{B_2} = \beta_2 I_{E_1} = \beta_2(\beta_1 I_{E_1}) = \beta_1\beta_2 I_{B_1}$$

resulting in

$$I_{C_2} \cong I_{E_2} = \beta_D I_{B_1} \tag{5.103}$$

The collector voltage of both transistors is

$$V_{C_1} = V_{C_2} = V_{CC} \tag{5.104}$$

the emitter voltage of $Q_2$

$$V_{E_2} = I_{E_2} R_E \tag{5.105}$$

the base voltage of $Q_1$

$$V_{B_1} = V_{CC} - I_{B_1} R_B = V_{E_2} + V_{BE_1} + V_{BE_2} \tag{5.106}$$

the collector-emitter voltage of $Q$

$$V_{CE_2} = V_{C_2} - V_{E_2} = V_{CC} - V_{E_2} \tag{5.107}$$

**EXAMPLE 5.17** Calculate the dc bias voltages and currents for the Darlington configuration of Fig. 5.76.

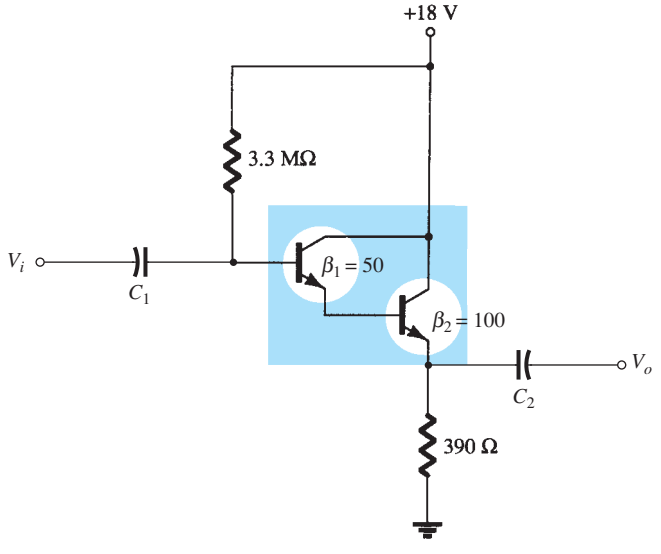



**FIG. 5.76**
*Circuit for Example 5.17.*

**Solution:**

$$\beta_D = \beta_1\beta_2 = (50)(100) = \mathbf{5000}$$

$$I_{B_1} = \frac{V_{CC} - V_{BE_1} - V_{BE_2}}{R_B + \beta_D R_E} = \frac{18\text{ V} - 0.7\text{ V} - 0.7\text{ V}}{3.3\text{ M}\Omega + (5000)(390\ \Omega)}$$

$$= \frac{18\text{ V} - 1.4\text{ V}}{3.3\text{ M}\Omega + 1.95\text{ M}\Omega} = \frac{16.6\text{ V}}{5.25\text{ M}\Omega} = \mathbf{3.16\ \mu A}$$

$$I_{C_2} \cong I_{E_2} = \beta_D I_{B_1} = (5000)(3.16\text{ mA}) = \mathbf{15.80\text{ mA}}$$

$$V_{C_1} = V_{C_2} = \mathbf{18\text{ V}}$$

$$V_{E_2} = I_{E_2}R_E = (15.80\text{ mA})(390\ \Omega) = \mathbf{6.16\text{ V}}$$

$$V_{B_1} = V_{E_2} + V_{BE_1} + V_{BE_2} = 6.16\text{ V} + 0.7\text{ V} + 0.7\text{ V} = \mathbf{7.56\text{ V}}$$

$$V_{CE_2} = V_{CC} - V_{E_2} = 18\text{ V} - 6.16\text{ V} = \mathbf{11.84\text{ V}}$$

**AC Input Impedance** The ac input impedance can be determined using the ac equivalent network of Fig. 5.77.

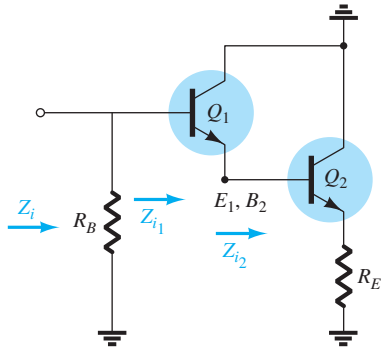



**FIG. 5.77**
*Finding $Z_i$.*

As defined in Fig. 5.77:

$$Z_{i_2} = \beta_2(r_{e_2} + R_E)$$

$$Z_{i_1} = \beta_1(r_{e_1} + Z_{i_2})$$

so that $$Z_{i_1} = \beta_1(r_{e_1} + \beta_2(r_{e_2} + R_E))$$

Assuming $$R_E \gg r_{e_2}$$

and $$Z_{i_1} = \beta_1(r_{e_1} + \beta_2 R_E)$$

Since $$\beta_2 R_E \gg r_{e_1}$$

$$Z_{i_1} \cong \beta_1\beta_2 R_E$$

and since $$Z_i = R_B \| Z_i$$

$$\boxed{Z_i = R_B \| \beta_1\beta_2 R_E = R_B \| \beta_D R_E} \qquad \textbf{(5.108)}$$

For the network of Fig. 5.76

$$Z_i = R_B \| \beta_D R_E$$

$$= 3.3\text{ M}\Omega \| (5000)(390\ \Omega) = 3.3\text{ M}\Omega \| 1.95\text{ M}\Omega$$

$$= \mathbf{1.38\text{ M}\Omega}$$

Note in the preceding analysis that the values of $r_e$ were not compared but dropped compared to much larger quantites. In a Darlington configuration the values of $r_e$ will be different because the emitter current through each transistor will be different. Also, keep in mind that chances are the beta values for each transistor will be different because thay deal with different current levels. The fact remains, however, that the product of the two beta values will equal $\beta_D$, as indicated on the specification sheet.

**AC Current Gain** The current gain can be determined from the equivalent network of Fig. 5.78. The output impedance of each transistor is ignored and the parameters for each transistor are employed.

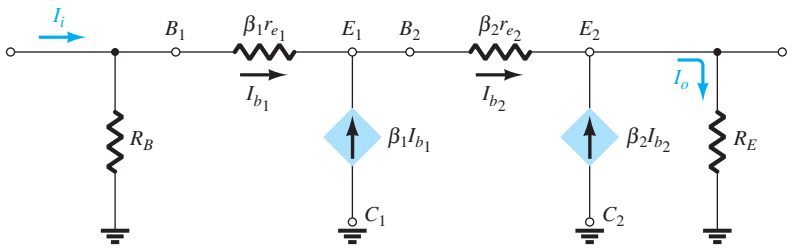



**FIG. 5.78**
*Determining $A_i$ for the network of Fig. 5.75.*

Solving for the output current: $I_o = I_{b_2} + \beta_2 I_{b_2} = (\beta_2 + 1)I_{b_2}$

with $I_{b_2} = \beta_1 I_{b_1} + I_{b_1} = (\beta_1 + 1)I_{b_1}$

Then $I_o = (\beta_2 + 1)(\beta_1 + 1)I_{b_1}$

Using the current-divider rule on the input circuit:

$$I_{b_1} = \frac{R_B}{R_B + Z_i} I_i = \frac{R_B}{R_B + \beta_1\beta_2 R_E} I_i$$

and

$$I_o = (\beta_2 + 1)(\beta_1 + 1)\left(\frac{R_B}{R_B + \beta_1\beta_2 R_E}\right) I_i$$

so that

$$A_i = \frac{I_o}{I_i} = \frac{(\beta_1 + 1)(\beta_2 + 1)R_B}{R_B + \beta_1\beta_2 R_E}$$

Using $\beta_1, \beta_2 \gg 1$

$$\boxed{A_i = \frac{I_o}{I_i} \cong \frac{\beta_1\beta_2 R_B}{R_B + \beta_1\beta_2 R_E}} \qquad \textbf{(5.109)}$$

or

$$\boxed{A_i = \frac{I_o}{I_i} \cong \frac{\beta_D R_B}{R_B + \beta_D R_E}} \qquad \textbf{(5.110)}$$

For Fig. 5.76:

$$A_i = \frac{I_o}{I_i} = \frac{\beta_D R_B}{R_B + \beta_D R_E} = \frac{(5000)(3.3\ \text{M}\Omega)}{3.3\ \text{M}\Omega + 1.95\ \text{M}\Omega}$$
$$= \mathbf{3.14 \times 10^3}$$

**AC Voltage Gain** The voltage gain can be determined using Fig. 5.77 and the following derivation:

$$V_o = I_o R_E$$
$$V_i = I_i(R_B \| Z_i)$$
$$R_B \| Z_i = R_B \| \beta_D R_E = \frac{\beta_D R_B R_E}{R_B + \beta_D R_E}$$

and

$$A_v = \frac{V_o}{V_i} = \frac{I_o R_E}{I_i(R_B \| Z_i)} = (A_i)\left(\frac{R_E}{R_B \| Z_i}\right)$$
$$= \left[\frac{\beta_D R_B}{R_B + \beta_D R_E}\right]\left[\frac{R_E}{\frac{\beta_D R_B R_E}{R_B + \beta_D R_E}}\right]$$

and

$$\boxed{A_v \cong 1 \text{ (in reality less than one)}} \qquad \textbf{(5.111)}$$

an expected result for the emitter-follower configuration.

**AC Output Impedance** The output impedance will be determined by going back to Fig. 5.78 and setting $V_i$ to zero volts as shown in Fig. 5.79. The resistor $R_B$ is "shorted out," resulting in the configuration of Fig. 5.80. Note in Figs. 5.82 and 5.83 that the output current has been redefined to match standard nomenclature and properly defined $Z_o$.

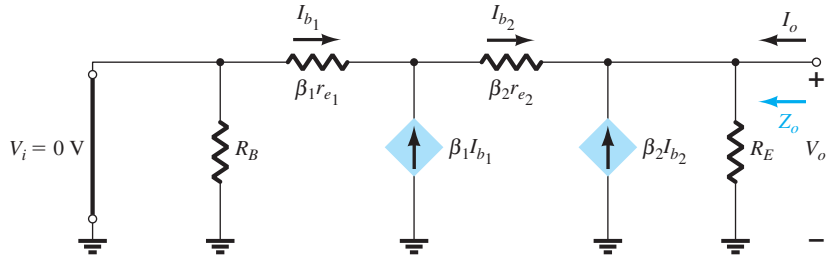



**FIG. 5.79**
*Determining $Z_o$.*

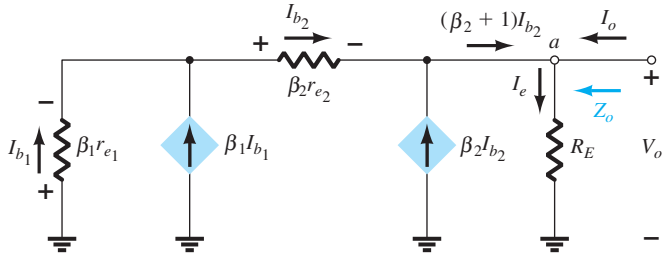



**FIG. 5.80**
*Redrawn of network of Fig. 5.79.*

At point *a* Kirchhoff's current law will result in $I_o + (\beta_2 + 1)I_{b_2} = I_e$:

$$I_o = I_e - (\beta_2 + 1)I_{b_2}$$

Applying Kirchhoff's voltage law around the entire outside loop will result in

$$-I_{b_1}\beta_1 r_{e_1} - I_{b_2}\beta_2 r_{e_2} - V_o = 0$$

and $$V_o = I_{b_1}\beta_1 r_{e_1} + I_{b_2}\beta_2 r_{e_2}$$

Substituting $$I_{b_2} = (\beta_1 + 1)I_{b_1}$$

$$V_o = -I_{b_1}\beta_1 r_{e_1} - (\beta_1 + 1)I_{b_1}\beta_2 r_{e_2}$$

$$= -I_{b_1}[\beta_1 r_{e_1} + (\beta_1 + 1)\beta_2 r_{e_2}]$$

and $$I_{b_1} = -\frac{V_o}{\beta_1 r_{e_1} + (\beta_1 + 1)\beta_2 r_{e_2}}$$

with $$I_{b_2} = (\beta_1 + 1)I_{b_1} = (\beta_1 + 1)\left[-\frac{V_o}{\beta_1 r_{e_1} + (\beta_1 + 1)\beta_2 r_{e_2}}\right]$$

so that $$I_{b_2} = -\left[\frac{\beta_1 + 1}{\beta_1 r_{e_1} + (\beta_1 + 1)\beta_2 r_{e_2}}\right]V_o$$

Going back $$I_o = I_e - (\beta_2 + 1)I_{b_2} = I_e - (\beta_2 + 1)\left(-\frac{(\beta_1 + 1)V_o}{\beta_1 r_{e_1} + (\beta_1 + 1)\beta_2 r_{e_2}}\right)$$

or $$I_o = \frac{V_o}{R_E} + \frac{(\beta_1 + 1)(\beta_2 + 1)V_o}{\beta_1 r_{e_1} + (\beta_1 + 1)\beta_2 r_{e_2}}$$

Because $\beta_1, \beta_2 \gg 1$

$$I_o = \frac{V_o}{R_E} + \frac{\beta_1\beta_2 V_o}{\beta_1 r_{e_1} + \beta_1\beta_2 r_{e_2}} = \frac{V_o}{R_E} + \frac{V_o}{\frac{\beta_1 r_{e_1}}{\beta_1\beta_2} + \frac{\beta_1\beta_2 r_{e_2}}{\beta_1\beta_2}}$$

$$I_o = \frac{V_o}{R_E} + \frac{V_o}{\frac{r_{e_1}}{\beta_2} + r_{e_2}}$$

which defines the parallel resistance network of Fig. 5.81.

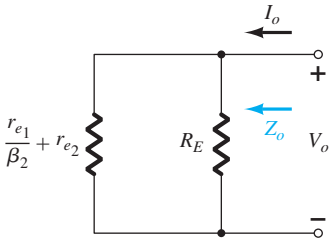



**FIG. 5.81**
*Resulting network defined by $Z_o$.*

In general, $R_E \gg \left(\frac{r_{e_1}}{\beta_2} + r_{e_2}\right)$ so the output impedance is defined by

$$Z_o = \frac{r_{e_1}}{\beta_2} + r_{e_2} \tag{5.112}$$

Using the dc results, the value of $r_{e_2}$ and $r_{e_1}$ can be determined as follows.

$$r_{e_2} = \frac{26\text{ mV}}{I_{E_2}} = \frac{26\text{ mV}}{15.80\text{ mA}} = 1.65\ \Omega$$

and

$$I_{E_1} = I_{B_2} = \frac{I_{E_2}}{\beta_2} = \frac{15.80\text{ mA}}{100} = 0.158\text{ mA}$$

so that

$$r_{e_1} = \frac{26\text{ mV}}{0.158\text{ mA}} = 164.5\ \Omega$$

The output impedance for the network of Fig. 5.78 is therefore:

$$Z_o \cong \frac{r_{e_1}}{\beta_2} + r_{e_2} = \frac{164.5\ \Omega}{100} + 1.65\ \Omega = 1.645\ \Omega + 1.65\ \Omega = \mathbf{3.30\ \Omega}$$

In general, the output impedance for the configuration of Fig. 5.78 is very low—in the order of a few ohms at most.

## Voltage-Divider Amplifier

**DC Bias** Let us now investigate the effect of the Darlington configuration in a basic amplifier configuration as shown in Fig. 5.82. Note that now there is a collector resistor $R_C$, and the emitter terminal of the Darlington circuit is connected to ground for ac conditions. As noted on Fig. 5.82, the beta of each transistor is provided along with the resulting voltage from base to emitter.

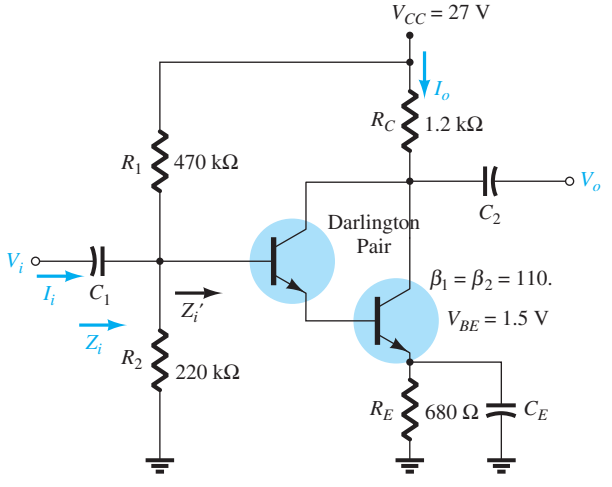



**FIG. 5.82**
*Amplifier configuration using a Darlington pair.*

The dc analysis can proceed as follows:

$$\beta_D = \beta_1\beta_2 = (110 \times 110) = 12{,}100$$

$$V_B = \frac{R_2}{R_2 + R_1}V_{CC} = \frac{220\,\text{k}\Omega(27\text{ V})}{220\,\text{k}\Omega + 470\,\text{k}\Omega} = \mathbf{8.61\text{ V}}$$

$$V_E = V_B - V_{BE} = 8.61\text{ V} - 1.5\text{ V} = \mathbf{7.11\text{ V}}$$

$$I_E = \frac{V_E}{R_E} = \frac{7.11\text{ V}}{680\,\Omega} = \mathbf{10.46\text{ mA}}$$

$$I_B = \frac{I_E}{\beta_D} = \frac{10.46\text{ mA}}{12{,}100} = \mathbf{0.864\ \mu A}$$

Using the preceding results the values of $r_{e_2}$ and $r_{e_1}$ can be determined:

$$r_{e_2} = \frac{26\text{ mV}}{I_{E_2}} = \frac{26\text{ mV}}{10.46\text{ mA}} = \mathbf{2.49\ \Omega}$$

$$I_{E_1} = I_{B_2} = \frac{I_{E_2}}{\beta_2} = \frac{10.46\text{ mA}}{110} = 0.095\text{ mA}$$

and

$$r_{e_1} = \frac{26\text{ mV}}{I_{E_1}} = \frac{26\text{ mV}}{0.095\text{ mA}} = \mathbf{273.7\ \Omega}$$

**AC Input Impedance** The ac equivalent of Fig. 5.82 appears as Fig. 5.83. The resistors $R_1$ and $R_2$ are in parallel with the input impedance to the Darlington pair, assuming the second transistor found by assuming the second transistor acts like an $R_E$ load on the first as shown in Fig. 5.83.

That is, $Z_i' = \beta_1 r_{e_1} + \beta_1(\beta_2 r_{e_2})$

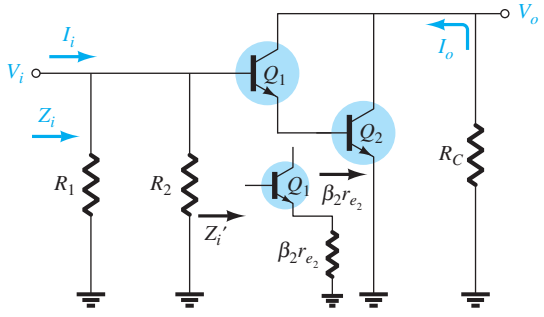



**FIG. 5.83**
*Defining $Z'_i$ and $Z_i$.*

and

$$\boxed{Z_i' = \beta_1[r_{e_1} + \beta_2 r_{e_2}]} \qquad \textbf{(5.113)}$$

For the network of Fig. 5.82:

$$Z_i' = 110[273.7\ \Omega + (110)(2.49\ \Omega)]$$
$$= 110[273.7\ \Omega + 273.9\ \Omega]$$
$$= 110[547.6\ \Omega]$$
$$= \mathbf{60.24\ k\Omega}$$

and

$$Z_i = R_1 \| R_2 \| Z_i'$$
$$= 470\,\text{k}\Omega \| 220\,\text{k}\Omega \| 60.24\,\text{k}\Omega$$
$$= 149.86\,\text{k}\Omega \| 60.24\,\text{k}\Omega$$
$$= \mathbf{42.97\ k\Omega}$$

**AC Current Gain** The complete ac equivalent of Fig. 5.82 appears as Fig. 5.84.

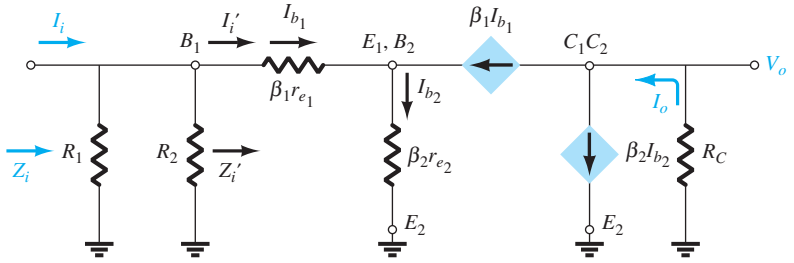



**FIG. 5.84**
*ac equivalent network for Fig. 5.82.*

The output current $I_o = \beta_1 I_{b_1} + \beta_2 I_{b_2}$

with $I_{b_2} = (\beta_1 + 1) I_{b_1}$

so that $I_o = \beta_1 I_{b_1} + \beta_2(\beta_1 + 1) I_{b_1}$

and with $I_{b_1} = I_i'$

we find $I_o = \beta_1 I_i' + \beta_2(\beta_1 + 1) I_i'$

and
$$A_i' = \frac{I_o}{I_i} = \beta_1 + \beta_2(\beta + 1)$$
$$\cong \beta_1 + \beta_2\beta_1 = \beta_1(1 + \beta_2)$$
$$\cong \beta_1\beta_2$$

and finally
$$\boxed{A_i' = \frac{I_o}{I_i'} = \beta_1\beta_2 = \beta_D} \qquad \textbf{(5.114)}$$

For the original structure:
$$I_i' = \frac{R_1 \| R_2 I_i}{R_1 \| R_2 + Z_i'} \quad \text{or} \quad \frac{I_i'}{I_i} = \frac{R_1 \| R_2}{R_1 \| R_2 + Z_i'}$$

but
$$A_i = \frac{I_o}{I_i} = \left(\frac{I_o}{I_i'}\right)\left(\frac{I_i'}{I_i}\right)$$

so that
$$\boxed{A_i = \frac{\beta_D(R_1 \| R_2)}{R_1 \| R_2 + Z_i'}} \qquad \textbf{(5.115)}$$

For Fig. 5.82
$$A_i = \frac{(12{,}100)(149.86\ \text{k}\Omega)}{149.86\ \text{k}\Omega + 60.24\ \text{k}\Omega}$$
$$= \mathbf{8630.7}$$

Note the significant drop in current gain due to $R_1$ and $R_2$.

**AC Voltage Gain** The input voltage is the same across $R_1$ and $R_2$ and at the base of the first transistor as shown in Fig. 5.84.

The result is
$$A_v = \frac{V_o}{V_i} = -\frac{I_o R_C}{I_i' Z_i'} = -A_i\left(\frac{R_C}{Z_i'}\right)$$

and
$$\boxed{A_v = -\frac{\beta_D R_C}{Z_i'}} \qquad \textbf{(5.116)}$$

For the network of Fig. 5.82,
$$A_v = -\frac{\beta_D R_C}{Z_i'} = -\frac{(12{,}000)(1.2\ \text{k}\Omega)}{60.24\ \text{k}\Omega} = \mathbf{-241.04}$$

**AC Output Impedence** Because the output impedance in $R_C$ is parallel with the collector to emitter terminals of the transistor, we can look back on similar situations and find that the output impedance is defined by

$$Z_o \cong R_C \| r_{o_2} \tag{5.117}$$

where $r_{o_2}$ is the output resistance of the transistor $Q_2$.

## Packaged Darlington Amplifier

Because the Darlington connection is so popular, a number of manufacturers provide packaged units such as shown in Fig. 5.85. Typically, the two BJTs are constructed on a single chip rather than separate BJT units. Note that only one set of collector, base, and emitter terminals is provided for each configuration. These, of course, are the base of the transistor $Q_1$, the collector of $Q_1$ and $Q_2$, and the emitter of $Q_2$.

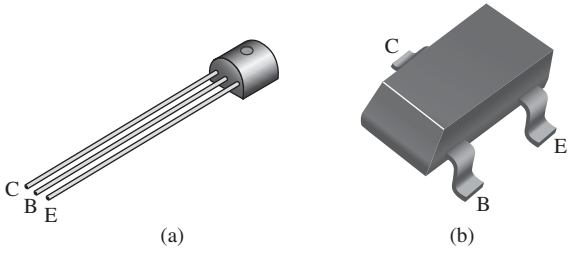



**FIG. 5.85**
*Packaged Darlington amplifiers: (a) TO-92 package; (b) Super SOT™-3 package.*

In Fig. 5.86 some of the ratings for an MPSA28 Fairchild Semiconductor Darlington amplifier are provided. In particular, note that the maximum collector-to-emitter voltage of 80 V is also the breakdown voltage. The same is true for the collector-to-base and emitter-to-base voltages, although notice how much lower the maximum ratings are for the base-to-emitter junction. Because of the Darlington configuration, the maximum current rating for the collector current has jumped to 800 mA—far exceeding levels we have encountered

| | | |
|---|---|---|
| ***Absolute Maximum Ratings*** | | |
| $V_{CES}$ | Collector-Emitter Voltage | 80 V |
| $V_{CBO}$ | Collector-Base Voltage | 80 V |
| $V_{EBO}$ | Emitter-Base Voltage | 12 V |
| $I_C$ | Collector Current–Continuous | 800 mA |
| ***Electrical Characteristics*** | | |
| $V_{(BR)CES}$ | Collector-Emitter Breakdown Voltage | 80 V |
| $V_{(BR)CBO}$ | Collector-Base Breakdown Voltage | 80 V |
| $V_{(BR)EBO}$ | Emitter-Base Breakdown Voltage | 12 V |
| $I_{CBO}$ | Collector Cutoff Current | 100 mA |
| $I_{EBO}$ | Emitter Cutoff Current | 100 mA |
| ***On Characteristics*** | | |
| $h_{FE}$ | DC Current Gain | 10,000 |
| $V_{CE(\text{sat})}$ | Collector-Emitter Saturation Voltage | 1.2 V |
| $V_{BE(\text{on})}$ | Base-Emitter on Voltage | 2.0 V |

**FIG. 5.86**
*MPSA 28 Fairchild Semiconductor Darlington amplifier ratings.*

for single-transistor networks. The dc current gain is rated at the high level of 10,000 and the base-to-emitter potential in the "on" state is 2 V, which certainly exceeds the 1.4 V we have used for individual transistors. Finally, it is interesting to note that the level of $I_{CEO}$ is much higher at 500 nA than for a typical single-transistor unit.

In the packaged format the network of Fig. 5.75 would appear as shown in Fig. 5.87. Using $\beta_D$ and the provided value of $V_{BE}$ ($=V_{BE_1} + V_{BE_2}$), all the equations appearing in this section can be applied.

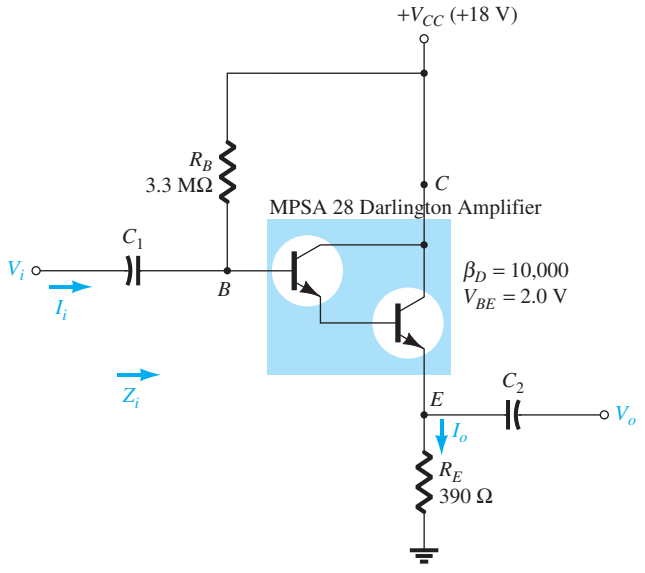



**FIG. 5.87**
*Darlington emitter-follower circuit.*

## 5.18 FEEDBACK PAIR

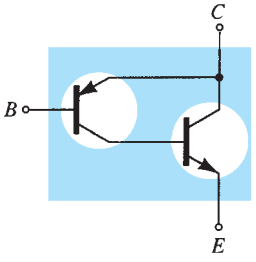



**FIG. 5.88**
*Feedback pair connection.*

The feedback pair connection (see Fig. 5.88) is a two-transistor circuit that operates like the Darlington circuit. Notice that the feedback pair uses a *pnp* transistor driving an *npn* transistor, the two devices acting effectively much like one *pnp* transistor. As with a Darlington connection, the feedback pair provides very high current gain (the product of the transistor current gains), high input impedance, low output impedance, and a voltage gain slightly less than one. Initially, it may appear that it would have a high voltage gain because the output is taken off the collector with a resistor $R_C$ in place. However, the *pnp–npn* combination results in terminal characteristics very similar to that of the emitter–follower configuration. A typical application (see Chapter 12) uses a Darlington and a feedback-pair connection to provide complementary transistor operation. A practical network employing a feedback pair is provided in Fig. 5.89 for investigation.

### DC Bias

The dc bias calculations that follow use practical simplifications wherever possible to provide simpler results. From the $Q_1$ base–emitter loop, one obtains

$$V_{CC} - I_C R_C - V_{EB_1} - I_{B_1} R_B = 0$$
$$V_{CC} - (\beta_1 \beta_2 I_{B_1}) R_C - V_{EB_1} - I_{B_1} R_B = 0$$

The base current is then

$$I_{B_1} = \frac{V_{CC} - V_{BE_1}}{R_B + \beta_1 \beta_2 R_C} \tag{5.118}$$

The collector current of $Q_1$ is

$$I_{C_1} = \beta_1 I_{B_1} = I_{B_2}$$

which is also the base $Q_2$ current. The transistor $Q_2$ collector current is

$$I_{C_2} = \beta_2 I_{B_2} \approx I_{E_2}$$

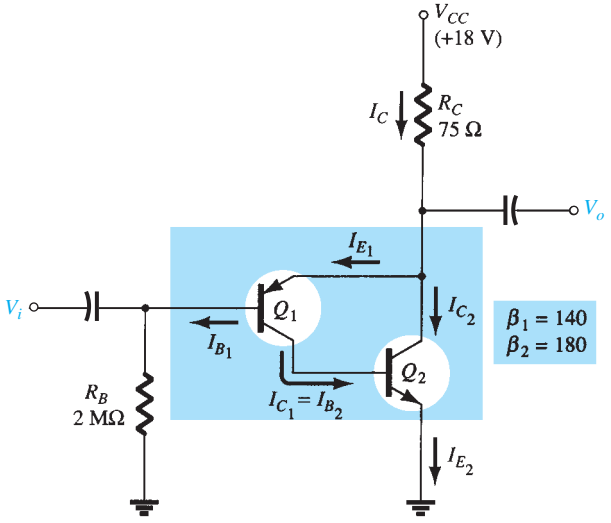



**FIG. 5.89**
*Operation of a feedback pair.*

so that the current through $R_C$ is

$$I_C = I_{E_1} + I_{C_2} \approx I_{B_2} + I_{C_2} \tag{5.119}$$

The voltages

$$V_{C_2} = V_{E_1} = V_{CC} - I_C R_C \tag{5.120}$$

and

$$V_{B_1} = I_{B_1} R_B \tag{5.121}$$

with

$$V_{BC_1} = V_{B_1} - V_{BE_2} = V_{B_1} - 0.7\text{ V} \tag{5.122}$$

**EXAMPLE 5.18** Calculate the dc bias currents and voltages for the circuit of Fig. 5.89 to provide $V_o$ at one-half the supply voltage (9 V).

***Solution:***

$$I_{B_1} = \frac{18\text{ V} - 0.7\text{ V}}{2\text{ M}\Omega + (140)(180)(75\ \Omega)} = \frac{17.3\text{ V}}{3.89 \times 10^6} = \mathbf{4.45\ \mu A}$$

The base $Q_2$ current is then

$$I_{B_2} = I_{C_1} = \beta_1 I_{B_1} = 140(4.45\ \mu\text{A}) = \mathbf{0.623\text{ mA}}$$

resulting in a $Q_2$ collector current of

$$I_{C_2} = \beta_2 I_{B_2} = 180(0.623\text{ mA}) = \mathbf{112.1\text{ mA}}$$

and the current through $R_C$ is then

$$\text{Eq. (5.119): } I_C = I_{E_1} + I_{C_2} = 0.623\text{ mA} + 112.1\text{ mA} \approx I_{C_2} = \mathbf{112.1\text{ mA}}$$

$$V_{C_2} = V_{E_1} = 18\text{ V} - (112.1\text{ mA})(75\ \Omega)$$
$$= 18\text{ V} - 8.41\text{ V}$$
$$= \mathbf{9.59\text{ V}}$$

$$V_{B_1} = I_{B_1} R_B = (4.45\ \mu\text{A})(2\text{ M}\Omega)$$
$$= \mathbf{8.9\text{ V}}$$

$$V_{BC_1} = V_{B_1} - 0.7\text{ V} = 8.9\text{ V} - 0.7\text{ V}$$
$$= \mathbf{8.2\text{ V}}$$

## AC Operation

The ac equivalent circuit for that of Fig. 5.89 is drawn in Fig. 5.90.

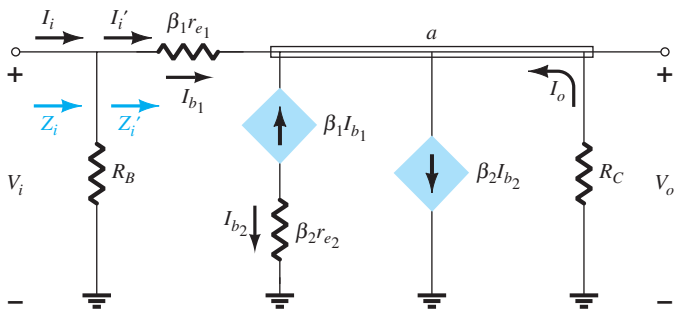



**FIG. 5.90**
*ac equivalent for the network of Fig. 5.89.*

**Input Impedance, $Z_i$** The ac input impedance seen looking into the base of transistor $Q_1$ is determined as follows:

$$Z_i' = \frac{V_i}{I_i'}$$

Applying Kirchhoff's current law at node $a$ and defining $I_c = I_o$:

$$I_{b_1} + \beta_1 I_{b_1} - \beta_2 I_{b_2} + I_o = 0$$

with $I_{b_2} = -\beta_1 I_{b_1}$ as noted in Fig. 5.90.

The result is
$$I_{b_1} + \beta_1 I_{b_1} - \beta_2(-\beta_1 I_{b_1}) + I_o = 0$$

and
$$I_o = -I_{b_1} - \beta_1 I_{b_1} - \beta_1\beta_2 I_{b_1}$$

or
$$I_o = -I_{b_1}(1 + \beta_1) - \beta_1\beta_2 I_{b_1}$$

but
$$\beta_1 \gg 1$$

and
$$I_o = -\beta_1 I_{b_1} - \beta_1\beta_2 I_{b_1} = -I_{b_1}(\beta_1 + \beta_1\beta_2)$$
$$= -I_{b_1}\beta_1(1 + \beta_2)$$

resulting in:
$$\boxed{I_o \cong -\beta_1\beta_2 I_{b_1}} \qquad \textbf{(5.123)}$$

Now, $I_{b_1} = \dfrac{V_i - V_o}{\beta_1 r_{e_1}}$ from Fig. 5.90

and
$$V_o = -I_o R_C = -(-\beta_1\beta_2 I_{b_1})R_C = \beta_1\beta_2 I_{b_1} R_C$$

so
$$I_{b_1} = \frac{V_i - \beta_1\beta_2 I_{b_1} R_C}{\beta_1 r_{e_1}}$$

Rearranging:
$$I_{b_1}\beta_1 r_{e_1} = V_i - \beta_1\beta_2 I_{b_1} R_C$$

and
$$I_{b_1}(\beta_1 r_{e_1} + \beta_1\beta_2 R_C) = V_i$$

so
$$I_{b_1} = I_i' = \frac{V_i}{\beta_1 r_{e_1} + \beta_1\beta_2 R_C}$$

and
$$V_i' = \frac{V_i}{I_i'} = \frac{V_i}{\dfrac{V_i}{\beta_1 r_e + \beta_1\beta_2 R_C}}$$

so that
$$\boxed{Z_i' = \beta_1 r_{e_1} + \beta_1\beta_2 R_C} \qquad \textbf{(5.124)}$$

In general,
$$\beta_1\beta_2 R_C \gg \beta_1 r_{e_1}$$

and
$$\boxed{Z_i' \cong \beta_1\beta_2 R_C} \qquad \textbf{(5.125)}$$

with $$\boxed{Z_i = R_B \| Z_i'} \tag{5.126}$$

For the network of Fig. 5.89: $$r_{e_1} = \frac{26\text{ mV}}{I_{E_1}} = \frac{26\text{ mV}}{0.623\text{ mA}} = 41.73\ \Omega$$

and
$$\begin{aligned} Z_i' &= \beta_1 r_{e_1} + \beta_1\beta_2 R_C \\ &= (140)(41.73\ \Omega) + (140)(180)(75\ \Omega) \\ &= 5842.2\ \Omega + 1.89\ \text{M}\Omega \\ &= \mathbf{1.895\ M\Omega} \end{aligned}$$

where Eq. (5.125) results in $Z_i' \cong \beta_1\beta_2 R_C = (140)(180)(75\ \Omega) = \mathbf{1.89\ M\Omega}$, validating the above approximations.

## Current Gain

Defining $I_{b_1} = I_i'$ as shown in Fig. 5.90 will permit finding the current gain $A_i' = I_o/I_i'$.

Looking back on the derivation of $Z_i$ we found $I_o = -\beta_1\beta_2 I_{b_1} = -\beta_1\beta_2 I_i'$

resulting in $$\boxed{A_i' = \frac{I_o}{I_i'} = -\beta_1\beta_2} \tag{5.127}$$

The current gain $A_i = I_o/I_i$ can be determined using the fact that

$$A_i = \frac{I_o}{I_i} = \frac{I_o}{I_i'} \cdot \frac{I_i'}{I_i}$$

For the input side: $$I_i' = \frac{R_B I_i}{R_B + Z_i'} = \frac{R_B I_i}{R_B + \beta_1\beta_2 R_C}$$

Substituting: $$A_i = \frac{I_o}{I_i'} \cdot \frac{I_i'}{I_i} = (-\beta_1\beta_2)\left(\frac{R_B}{R_B + \beta_1\beta_2 R_C}\right)$$

So that $$\boxed{A_i = \frac{I_o}{I_i} = \frac{-\beta_1\beta_2 R_B}{R_B + \beta_1\beta_2 R_C}} \tag{5.128}$$

The negative sign appears because both $I_i$ and $I_o$ are defined as entering the network.

For the network of Fig. 5.89:
$$\begin{aligned} A_i' &= \frac{I_o}{I_i'} = -\beta_1\beta_2 \\ &= -(140)(180) \\ &= \mathbf{-25.2 \times 10^3} \end{aligned}$$

$$\begin{aligned} A_i &= \frac{-\beta_1\beta_2 R_B}{R_B + \beta_1\beta_2 R_c} = -\frac{(140)(180)(2\ \text{M}\Omega)}{2\ \text{M}\Omega + 1.89\ \text{M}\Omega} \\ &= -\frac{50{,}400\ \text{M}\Omega}{3.89\ \text{M}\Omega} \\ &= \mathbf{-12.96 \times 10^3}\ (\cong \text{ half of } A_i') \end{aligned}$$

## Voltage Gain

The voltage gain can quickly be determined using the results obtained above.

That is, $$A_v = \frac{V_o}{V_i} = \frac{-I_o R_C}{I_i' Z_i'}$$

$$= -\frac{(-\beta_1\beta_2 I_i')R_C}{I_i'(\beta_1 r_{e_1} + \beta_1\beta_2 R_C)}$$

$$\boxed{A_v = \frac{\beta_2 R_C}{r_{e_1} + \beta_2 R_C}} \tag{5.129}$$

which is simply the following if we apply the approximation: $\beta_2 R_C \gg r_{e_1}$

$$A_v \cong \frac{\beta_2 R_C}{\beta_2 R_C} = 1$$

For the network of Fig. 5.89:

$$A_v = \frac{\beta_2 R_C}{r_{e_1} + \beta_2 R_C} = \frac{(180)(75\ \Omega)}{41.73\ \Omega + (180)(75\ \Omega)}$$

$$= \frac{13.5 \times 10^3\ \Omega}{41.73\ \Omega + 13.5 \times 10^3\ \Omega}$$

$$= \mathbf{0.997} \cong 1 \text{ (as indicated above)}$$

## Output Impedance

The output impedance $Z_o'$ is defined in Fig. 5.91 when $V_i$ is set to zero volts.

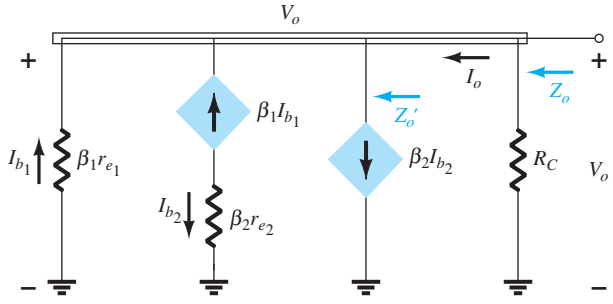



**FIG. 5.91**
*Determining $Z_o'$ and $Z_o$.*

Using the fact that $I_o = -\beta_1\beta_2 I_{b_1}$ from calculations above, we find that

$$Z_o' = \frac{V_o}{I_o} = \frac{V_o}{-\beta_1\beta_2 I_{b_1}}$$

but

$$I_{b_1} = -\frac{V_o}{\beta_1 r_{e_1}}$$

and

$$Z_o' = \frac{V_o}{-\beta_1\beta_2\left(-\dfrac{V_o}{\beta_1 r_{e_1}}\right)} = \frac{\beta_1 r_{e_1}}{\beta_1\beta_2}$$

so that

$$\boxed{Z_o' = \frac{r_{e_1}}{\beta_2}} \tag{5.130}$$

with

$$\boxed{Z_o = R_C \| \frac{r_{e_1}}{\beta_2}} \tag{5.131}$$

However,

$$R_C \gg \frac{r_{e_1}}{\beta_2}$$

leaving

$$\boxed{Z_o \cong \frac{r_{e_1}}{\beta_2}} \tag{5.132}$$

which will be a very low value.
For the network of Fig. 5.89:

$$Z_o \cong \frac{41.73\ \Omega}{180} = \mathbf{0.23\ \Omega}$$

The preceding analysis shows that the feedback pair connection of Fig. 5.89 provides operation with voltage gain very near 1 (just as with a Darlington emitter-follower), a very high current gain, a very low output impedance, and a high input impedance.

## 5.19 THE HYBRID EQUIVALENT MODEL

The hybrid equivalent model was mentioned in the earlier sections of this chapter as one that was used in the early years before the popularity of the $r_e$ model developed. Today there is a mix of usage depending on the level and direction of the investigation.

***The $r_e$ model has the advantage that the parameters are defined by the actual operating conditions,***

whereas

***the parameters of the hybrid equivalent circuit are defined in general terms for any operating conditions.***

In other words, the hybrid parameters may not reflect the actual operating conditions but simply provide an indication of the level of each parameter to expect for general use. The $r_e$ model suffers from the fact that parameters such as the output impedance and the feedback elements are not available, whereas the hybrid parameters provide the entire set on the specification sheet. In most cases, if the $r_e$ model is employed, the investigator will simply examine the specification sheet to have some idea of what the additional elements might be. This section will show how one can go from one model to the other and how the parameters are related. Because all specification sheets provide the hybrid parameters and the model is still extensively used, it is important to be aware of both models. The hybrid parameters as shown in Fig. 5.92 are derived from the specification sheet for the 2N4400 transistor described in Chapter 3. The values are provided at a dc collector current of 1 mA and a collector-to-emitter voltage of 10 V. In addition, a range of values is provided for each parameter for guidance in the initial design or analysis of a system. One obvious advantage of the specification sheet listing is the immediate knowledge of typical levels for the parameters of the device as compared to other transistors.

| | | Min. | Max. | |
|---|---|---|---|---|
| Input impedance ($I_C$ = 1 mA dc, $V_{CE}$ = 10 V dc, $f$ = 1 kHz) | $h_{ie}$ | 0.5 | 7.5 | kΩ |
| Voltage feedback ratio ($I_C$ = 1 mA dc, $V_{CE}$ = 10 V dc, $f$ = 1 kHz) | $h_{re}$ | 0.1 | 8.0 | $\times 10^{-4}$ |
| Small-signal current gain ($I_C$ = 1 mA dc, $V_{CE}$ = 10 V dc, $f$ = 1 kHz) | $h_{fe}$ | 20 | 250 | — |
| Output admittance ($I_C$ = 1 mA dc, $V_{CE}$ = 10 V dc, $f$ = 1 kHz) | $h_{oe}$ | 1.0 | 30 | 1 μS |

**FIG. 5.92**
*Hybrid parameters for the 2N4400 transistor.*

The description of the hybrid equivalent model will begin with the general two-port system of Fig. 5.93. The following set of equations (5.131) and (5.132) is only one of a number of ways in which the four variables of Fig. 5.93 can be related. It is the most frequently employed in transistor circuit analysis, however, and therefore is discussed in detail in this chapter.

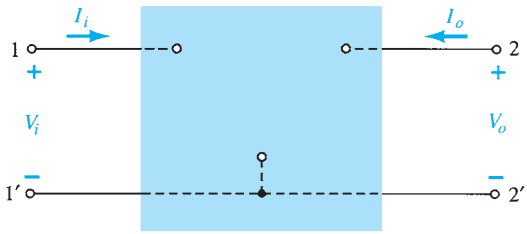



**FIG. 5.93**
*Two-port system.*

$$V_i = h_{11}I_i + h_{12}V_o \tag{5.133}$$

$$I_o = h_{21}I_i + h_{22}V_o \tag{5.134}$$

The parameters relating the four variables are called *h-parameters*, from the word "hybrid." The term *hybrid* was chosen because the mixture of variables ($V$ and $I$) in each equation results in a "hybrid" set of units of measurement for the $h$-parameters. A clearer understanding of what the various $h$-parameters represent and how we can determine their magnitude can be developed by isolating each and examining the resulting relationship.

**$h_{11}$** If we arbitrarily set $V_o = 0$ (short circuit the output terminals) and solve for $h_{11}$ in Eq. (5.133), we find

$$h_{11} = \left.\frac{V_i}{I_i}\right|_{V_o=0} \quad \text{ohms} \tag{5.135}$$

The ratio indicates that the parameter $h_{11}$ is an impedance parameter with the units of ohms. Because it is the ratio of the *input* voltage to the *input* current with the output terminals *shorted*, it is called the *short-circuit input-impedance parameter.* The subscript 11 of $h_{11}$ refers to the fact that the parameter is determined by a ratio of quantities measured at the input terminals.

**$h_{12}$** If $I_i$ is set equal to zero by opening the input leads, the following results for $h_{12}$:

$$h_{12} = \left.\frac{V_i}{V_o}\right|_{I_i=0} \quad \text{unitless} \tag{5.136}$$

The parameter $h_{12}$, therefore, is the ratio of the input voltage to the output voltage with the input current equal to zero. It has no units because it is a ratio of voltage levels and is called the *open-circuit reverse transfer voltage ratio parameter.* The subscript 12 of $h_{12}$ indicates that the parameter is a transfer quantity determined by a ratio of input (1) to output (2) measurements. The first integer of the subscript defines the measured quantity to appear in the numerator; the second integer defines the source of the quantity to appear in the denominator. The term *reverse* is included because the ratio is an input voltage over an output voltage rather than the reverse ratio typically of interest.

**$h_{21}$** If in Eq. (5.134) $V_o$ is set equal to zero by again shorting the output terminals, the following results for $h_{21}$:

$$h_{21} = \left.\frac{I_o}{I_i}\right|_{V_o=0} \quad \text{unitless} \tag{5.137}$$

Note that we now have the ratio of an output quantity to an input quantity. The term *forward* will now be used rather than *reverse* as indicated for $h_{12}$. The parameter $h_{21}$ is the ratio of the output current to the input current with the output terminals shorted. This parameter, like $h_{12}$, has no units because it is the ratio of current levels. It is formally called the *short-circuit forward transfer current ratio parameter.* The subscript 21 again indicates that it is a transfer parameter with the output quantity (2) in the numerator and the input quantity (1) in the denominator.

**$h_{22}$** The last parameter, $h_{22}$, can be found by again opening the input leads to set $I_1 = 0$ and solving for $h_{22}$ in Eq. (5.134):

$$h_{22} = \left.\frac{I_o}{V_o}\right|_{I_i=0} \quad \text{siemens} \tag{5.138}$$

Because it is the ratio of the output current to the output voltage, it is the output conductance parameter, and it is measured in siemens (S). It is called the *open-circuit output admittance parameter.* The subscript 22 indicates that it is determined by a ratio of output quantities.

Because each term of Eq. (5.133) has the unit volt, let us apply Kirchhoff's voltage law "in reverse" to find a circuit that "fits" the equation. Performing this operation results in the circuit of Fig. 5.94. Because the parameter $h_{11}$ has the unit ohm, it is represented by a resistor in Fig. 5.94. The quantity $h_{12}$ is dimensionless and therefore simply appears as a multiplying factor of the "feedback" term in the input circuit.

Because each term of Eq. (5.134) has the units of current, let us now apply Kirchhoff's current law "in reverse" to obtain the circuit of Fig. 5.95. Because $h_{22}$ has the units of admittance, which for the transistor model is conductance, it is represented by the resistor symbol. Keep in mind, however, that the resistance in ohms of this resistor is equal to the reciprocal of conductance ($1/h_{22}$).

The complete "ac" equivalent circuit for the basic three-terminal linear device is indicated in Fig. 5.96 with a new set of subscripts for the $h$-parameters. The notation of Fig. 5.96 is of a more practical nature because it relates the $h$-parameters to the resulting ratio obtained in the last few paragraphs. The choice of letters is obvious from the following listing:

$$h_{11} \longrightarrow \textit{i}\text{nput resistance} \longrightarrow h_i$$
$$h_{12} \longrightarrow \textit{r}\text{everse transfer voltage ratio} \longrightarrow h_r$$
$$h_{21} \longrightarrow \textit{f}\text{orward transfer current ratio} \longrightarrow h_f$$
$$h_{22} \longrightarrow \textit{o}\text{utput conductance} \longrightarrow h_o$$

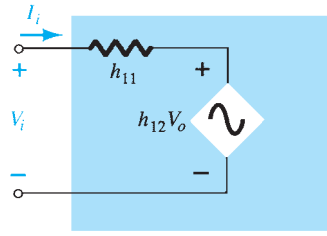



**FIG. 5.94**
*Hybrid input equivalent circuit.*

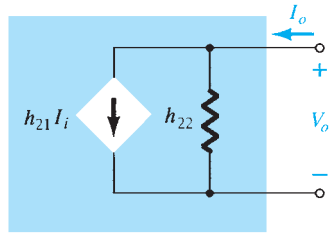



**FIG. 5.95**
*Hybrid output equivalent circuit.*

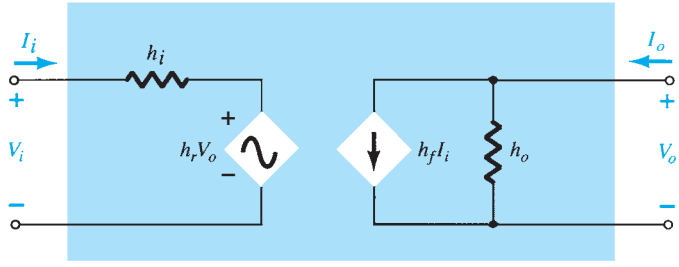



**FIG. 5.96**
*Complete hybrid equivalent circuit.*

The circuit of Fig. 5.96 is applicable to any linear three-terminal electronic device or system with no internal independent sources. For the transistor, therefore, even though it has three basic configurations, *they are all three-terminal configurations*, so that the resulting equivalent circuit will have the same format as shown in Fig. 5.96. In each case, the bottom of the input and output sections of the network of Fig. 5.96 can be connected as shown in Fig. 5.97 because the potential level is the same. Essentially, therefore, the transistor model is a three-terminal two-port system. The $h$-parameters, however, will change with each configuration. To distinguish which parameter has been used or which is available, a second

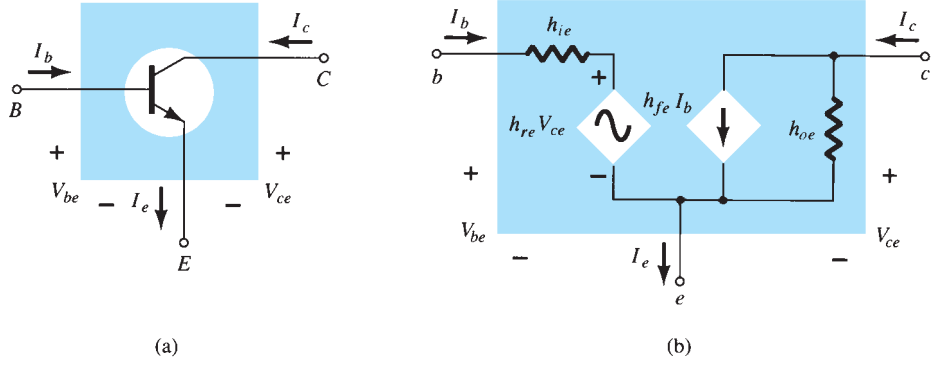



**FIG. 5.97**
*Common-emitter configuration: (a) graphical symbol; (b) hybrid equivalent circuit.*

subscript has been added to the $h$-parameter notation. For the common-base configuration, the lowercase letter $b$ was added, whereas for the common-emitter and common-collector configurations, the letters $e$ and $c$ were added, respectively. The hybrid equivalent network for the common-emitter configuration appears with the standard notation in Fig. 5.97. Note that $I_i = I_b$, $I_o = I_c$, and, through an application of Kirchhoff's current law, $I_e = I_b + I_c$. The input voltage is now $V_{be}$, with the output voltage $V_{ce}$. For the common-base configuration of Fig. 5.98, $I_i = I_e$, $I_o = I_c$ with $V_{eb} = V_i$ and $V_{cb} = V_o$. The networks of Figs. 5.97 and 5.98 are applicable for *pnp* or *npn* transistors.

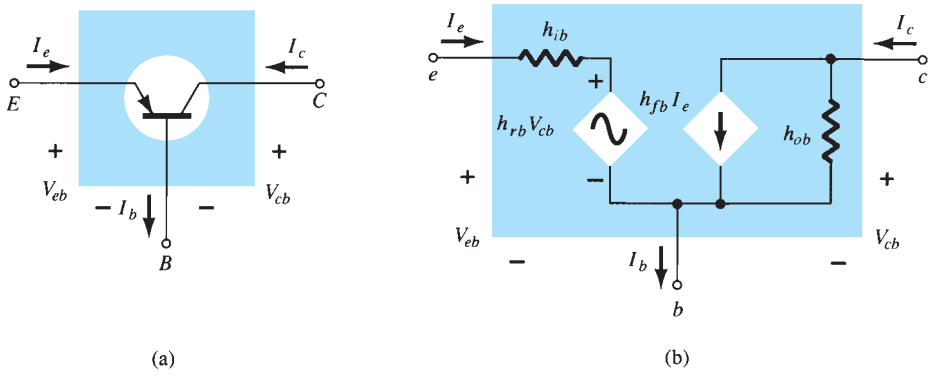



**FIG. 5.98**
*Common-base configuration: (a) graphical symbol; (b) hybrid equivalent circuit.*

The fact that both a Thévenin and a Norton circuit appear in the circuit of Fig. 5.96 was further impetus for calling the resultant circuit a *hybrid* equivalent circuit. Two additional transistor equivalent circuits, not to be discussed in this text, called the **z**-parameter and **y**-parameter equivalent circuits, use either the voltage source or the current source, but not both, in the same equivalent circuit. In Appendix A the magnitudes of the various parameters will be found from the transistor characteristics in the region of operation resulting in the desired *small-signal equivalent network* for the transistor.

For the common-emitter and common-base configurations, the magnitude of $h_r$ and $h_o$ is often such that the results obtained for the important parameters such as $Z_i$, $Z_o$, $A_v$, and $A_i$ are only slightly affected if $h_r$ and $h_o$ are not included in the model.

Because $h_r$ is normally a relatively small quantity, its removal is approximated by $h_r \cong 0$ and $h_r V_o = 0$, resulting in a short-circuit equivalent for the feedback element as shown in Fig. 5.99. The resistance determined by $1/h_o$ is often large enough to be ignored in comparison to a parallel load, permitting its replacement by an open-circuit equivalent for the CE and CB models, as shown in Fig. 5.99.

The resulting equivalent of Fig. 5.100 is quite similar to the general structure of the common-base and common-emitter equivalent circuits obtained with the $r_e$ model. In fact,

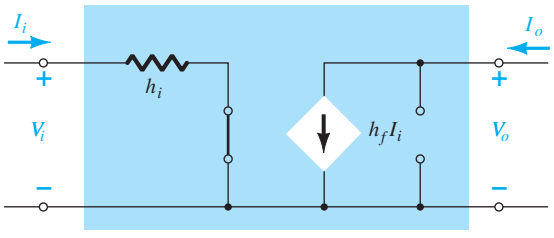



**FIG. 5.99**
*Effect of removing $h_{re}$ and $h_{oe}$ from the hybird equivalent circuit.*

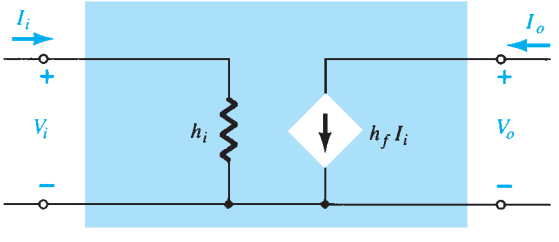



**FIG. 5.100**
*Approximate hybrid equivalent model.*

the hybrid equivalent and the $r_e$ models for each configuration are repeated in Fig. 5.101 for comparison. It should be reasonably clear from Fig. 5.101a that

$$h_{ie} = \beta r_e \tag{5.139}$$

and

$$h_{fe} = \beta_{ac} \tag{5.140}$$

From Fig. 5.101b,

$$h_{ib} = r_e \tag{5.141}$$

and

$$h_{fb} = -\alpha \cong -1 \tag{5.142}$$

In particular, note that the minus sign in Eq. (5.142) accounts for the fact that the current source of the standard hybrid equivalent circuit is pointing down rather than in the actual direction as shown in the $r_e$ model of Fig. 5.101b.

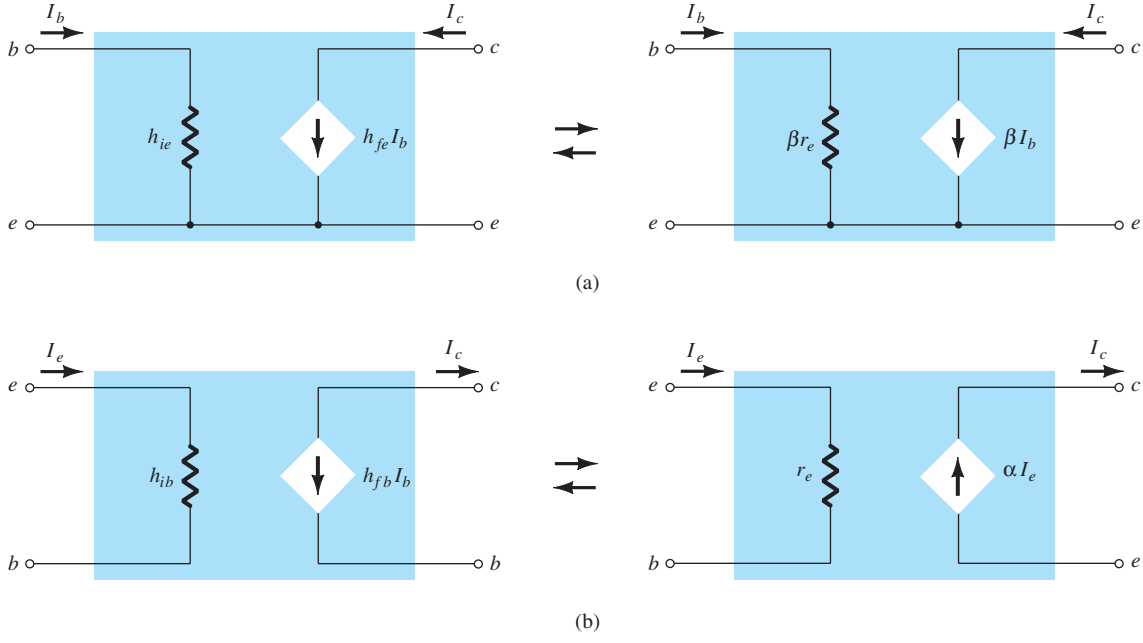



**FIG. 5.101**

*Hybrid versus $r_e$ model: (a) common-emitter configuration; (b) common-base configuration.*

**EXAMPLE 5.19** Given $I_E = 2.5$ mA, $h_{fe} = 140$, $h_{oe} = 20\ \mu$S ($\mu$mho), and $h_{ob} = 0.5\ \mu$S, determine:

a. The common-emitter hybrid equivalent circuit.
b. The common-base $r_e$ model.

***Solution:***

a. $$r_e = \frac{26\text{ mV}}{I_E} = \frac{26\text{ mV}}{2.5\text{ mA}} = \mathbf{10.4\ \Omega}$$

$$h_{ie} = \beta r_e = (140)(10.4\ \Omega) = \mathbf{1.456\ k\Omega}$$

$$r_o = \frac{1}{h_{oe}} = \frac{1}{20\ \mu\text{S}} = \mathbf{50\ k\Omega}$$

Note Fig. 5.102.

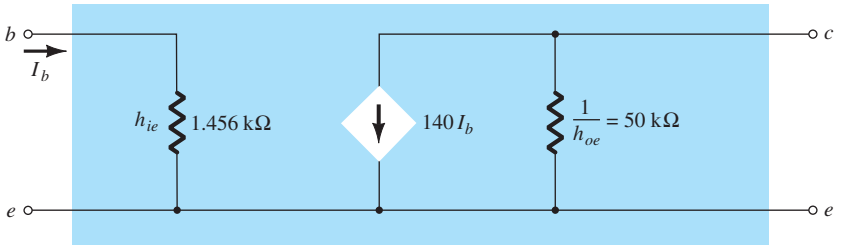



**FIG. 5.102**
*Common-emitter hybrid equivalent circuit for the parameters of Example 5.19.*

b. $r_e = \mathbf{10.4\ \Omega}$

$$\alpha \cong 1, \qquad r_o = \frac{1}{h_{ob}} = \frac{1}{0.5\ \mu\text{S}} = \mathbf{2\ M\Omega}$$

Note Fig. 5.103.

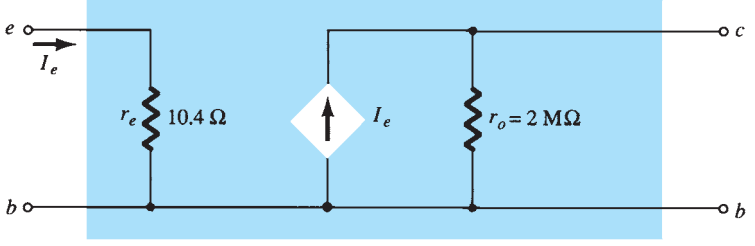



**FIG. 5.103**
*Common-base $r_e$ model for the parameters of Example 5.19.*

A series of equations relating the parameters of each configuration for the hybrid equivalent circuit is provided in Appendix B. In Section 5.23 it is demonstrated that the hybrid parameter $h_{fe}$ ($\beta_{ac}$) is the least sensitive of the hybrid parameters to a change in collector current. Assuming, therefore, that $h_{fe} = \beta$ is a constant for the range of interest, is a fairly good approximation. It is $h_{ie} = \beta r_e$ that will vary significantly with $I_C$ and should be determined at operating levels because it can have a real effect on the gain levels of a transistor amplifier.

## 5.20 APPROXIMATE HYBRID EQUIVALENT CIRCUIT

The analysis using the approximate hybrid equivalent circuit of Fig. 5.104 for the common-emitter configuration and of Fig. 5.105 for the common-base configuration is very similar to that just performed using the $r_e$ model. A brief overview of some of the most important configurations will be included in this section to demonstrate the similarities in approach and the resulting equations.

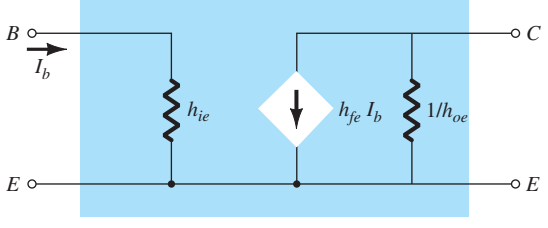



**FIG. 5.104**
*Approximate common-emitter hybrid equivalent circuit.*

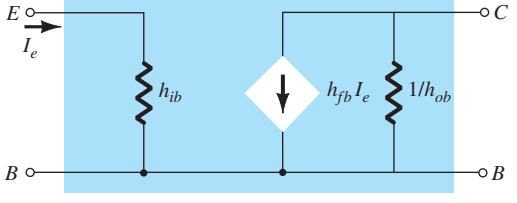



**FIG. 5.105**
*Approximate common-base hybrid equivalent circuit.*

Because the various parameters of the hybrid model are specified by a data sheet or experimental analysis, the dc analysis associated with use of the $r_e$ model is not an integral part of the use of the hybrid parameters. In other words, when the problem is presented, the parameters such as $h_{ie}$, $h_{fe}$, $h_{ib}$, and so on, are specified. Keep in mind, however, that the hybrid parameters and components of the $r_e$ model are related by the following equations, as discussed earlier in this chapter: $h_{ie} = \beta r_e$, $h_{fe} = \beta$, $h_{oe} = 1/r_o$, $h_{fb} = -\alpha$, and $h_{ib} = r_e$.

## Fixed-Bias Configuration

For the fixed-bias configuration of Fig. 5.106, the small-signal ac equivalent network will appear as shown in Fig. 5.107 using the approximate common-emitter hybrid equivalent model. Compare the similarities in appearance with Fig. 5.22 and the $r_e$ model analysis. The similarities suggest that the analyses will be quite similar, and the results of one can be directly related to the other.

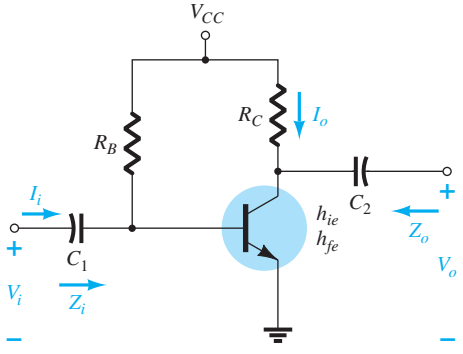



**FIG. 5.106**
*Fixed-bias configuration.*

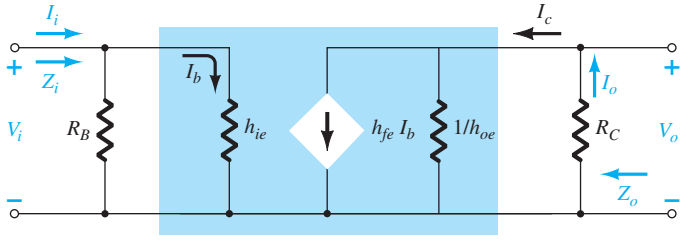



**FIG. 5.107**
*Substituting the approximate hybrid equivalent circuit into the ac equivalent network of Fig. 5.106.*

**$Z_i$** From Fig. 5.107,

$$Z_i = R_B \| h_{ie} \tag{5.143}$$

**$Z_o$** From Fig. 5.107,

$$Z_o = R_C \| 1/h_{oe} \tag{5.144}$$

**$A_v$** Using $R' = 1/h_{oe} \| R_C$, we obtain

$$V_o = -I_o R' = -I_C R'$$
$$= -h_{fe} I_b R'$$

and

$$I_b = \frac{V_i}{h_{ie}}$$

with

$$V_o = -h_{fe} \frac{V_i}{h_{ie}} R'$$

so that

$$A_v = \frac{V_o}{V_i} = -\frac{h_{ie}(R_C \| 1/h_{oe})}{h_{ie}} \tag{5.145}$$

**$A_i$** Assuming that $R_B \gg h_{ie}$ and $1/h_{oe} \geq 10R_C$, we find $I_b \cong I_i$ and $I_o = I_c = h_{fe} I_b = h_{fe} I_i$, and so

$$A_i = \frac{I_o}{I_i} \cong h_{fe} \tag{5.146}$$

**EXAMPLE 5.20** For the network of Fig. 5.108, determine:

a. $Z_i$.
b. $Z_o$.
c. $A_v$.
d. $A_i$.

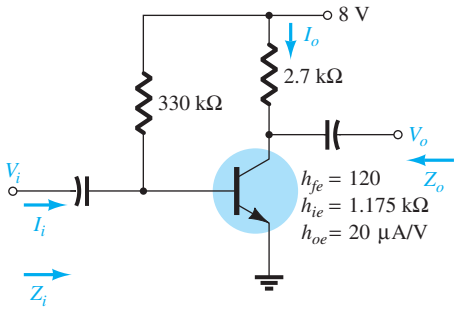



**FIG. 5.108**
*Example 5.20.*

***Solution:***

a. $Z_i = R_B \| h_{ie} = 330\,\text{k}\Omega \| 1.175\,\text{k}\Omega$

$\cong h_{ie} = \mathbf{1.171\,k\Omega}$

b. $r_o = \dfrac{1}{h_{oe}} = \dfrac{1}{20\,\mu\text{A/V}} = 50\,\text{k}\Omega$

$Z_o = \dfrac{1}{h_{oe}} \| R_C = 50\,\text{k}\Omega \| 2.7\,\text{k}\Omega = \mathbf{2.56\,k\Omega} \cong R_C$

c. $A_v = -\dfrac{h_{fe}(R_C \| 1/h_{oe})}{h_{ie}} = -\dfrac{(120)(2.7\,\text{k}\Omega \| 50\,\text{k}\Omega)}{1.171\,\text{k}\Omega} = \mathbf{-262.34}$

d. $A_i \cong h_{fe} = \mathbf{120}$

## Voltage-Divider Configuration

For the voltage-divider bias configuration of Fig. 5.109, the resulting small-signal ac equivalent network will have the same appearance as Fig. 5.107, with $R_B$ replaced by $R' = R_1 \| R_2$.

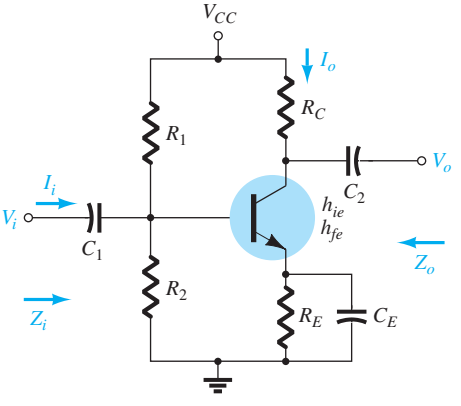



**FIG. 5.109**
*Voltage-divider bias configuration.*

**$Z_i$** From Fig. 5.107 with $R_B = R'$,

$$Z_i = R_1 \| R_2 \| h_{ie} \tag{5.147}$$

**$Z_o$** From Fig. 5.107,

$$Z_o \cong R_C \tag{5.148}$$

**$A_v$**

$$A_v = -\frac{h_{fe}(R_C \| 1/h_{oe})}{h_{ie}} \tag{5.149}$$

**$A_i$**

$$A_i = \frac{h_{fe}(R_1 \| R_2)}{R_1 \| R_2 + h_{ie}} \tag{5.150}$$

## Unbypassed Emitter-Bias Configuration

For the CE unbypassed emitter-bias configuration of Fig. 5.110, the small-signal ac model will be the same as Fig. 5.30, with $\beta r_e$ replaced by $h_{ie}$ and $\beta I_b$ by $h_{fe} I_b$. The analysis will proceed in the same manner.

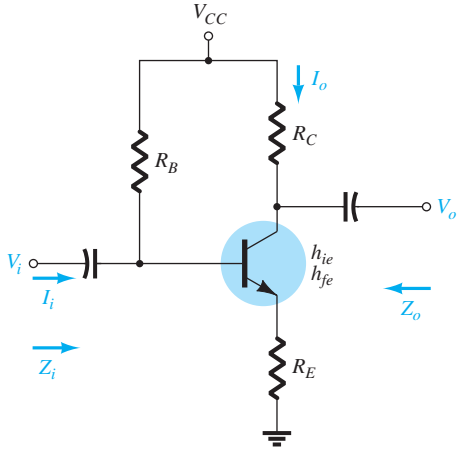



**FIG. 5.110**
*CE unbypassed emitter-bias configuration.*

**$Z_i$**

$$Z_b \cong h_{fe} R_E \tag{5.151}$$

and

$$Z_i = R_B \| Z_b \tag{5.152}$$

**$Z_o$**

$$Z_o = R_C \tag{5.153}$$

**$A_v$**

$$A_v = -\frac{h_{fe} R_C}{Z_b} \cong -\frac{h_{fe} R_C}{h_{fe} R_E}$$

and

$$A_v \cong -\frac{R_C}{R_E} \tag{5.154}$$

**$A_i$**

$$A_i = -\frac{h_{fe}R_B}{R_B + Z_b} \tag{5.155}$$

or

$$A_i = -A_v\frac{Z_i}{R_C} \tag{5.156}$$

## Emitter-Follower Configuration

For the emitter-follower of Fig. 5.38, the small-signal ac model will match that of Fig. 5.111, with $\beta r_e = h_{ie}$ and $\beta = h_{fe}$. The resulting equations will therefore be quite similar.

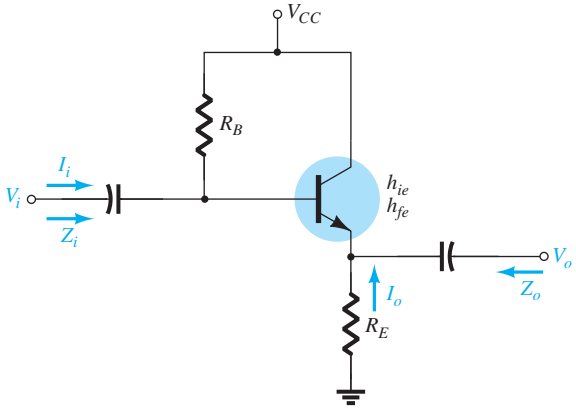



**FIG. 5.111**
*Emitter-follower configuration.*

**$Z_i$**

$$Z_b \cong h_{fe}R_E \tag{5.157}$$

$$Z_i = R_B \| Z_b \tag{5.158}$$

**$Z_o$** For $Z_o$, the output network defined by the resulting equations will appear as shown in Fig. 5.112. Review the development of the equations in Section 5.8 and

$$Z_o = R_E \| \frac{h_{ie}}{1 + h_{fe}}$$

or, because $1 + h_{fe} \cong h_{fe}$,

$$Z_o \cong R_E \| \frac{h_{ie}}{h_{fe}} \tag{5.159}$$

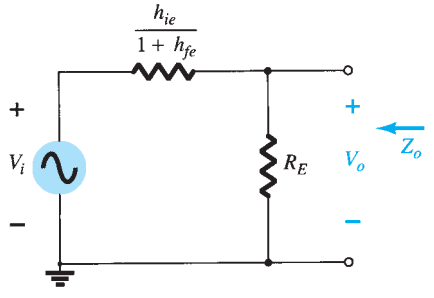



**FIG. 5.112**
*Defining $Z_o$ for the emitter-follower configuration.*

**$A_v$** For the voltage gain, the voltage-divider rule can be applied to Fig. 5.112 as follows:

$$V_o = \frac{R_E(V_i)}{R_E + h_{ie}/(1 + h_{fe})}$$

but, since $1 + h_{fe} \cong h_{fe}$,

$$\boxed{A_v = \frac{V_o}{V_i} \cong \frac{R_E}{R_E + h_{ie}/h_{fe}}} \qquad \textbf{(5.160)}$$

**$A_i$**

$$\boxed{A_i = \frac{h_{fe} R_B}{R_B + Z_b}} \qquad \textbf{(5.161)}$$

or

$$\boxed{A_i = -A_v \frac{Z_i}{R_E}} \qquad \textbf{(5.162)}$$

## Common-Base Configuration

The last configuration to be examined with the approximate hybrid equivalent circuit will be the common-base amplifier of Fig. 5.113. Substituting the approximate common-base hybrid equivalent model results in the network of Fig. 5.114, which is very similar to Fig. 5.44.

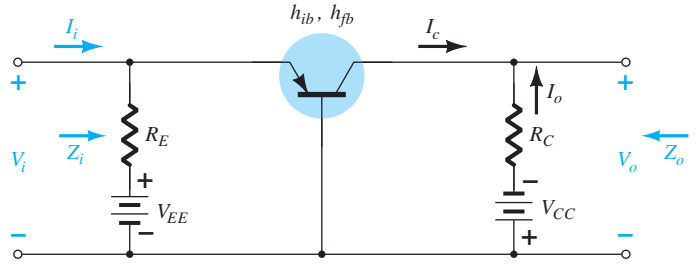



**FIG. 5.113**
*Common-base configuration.*

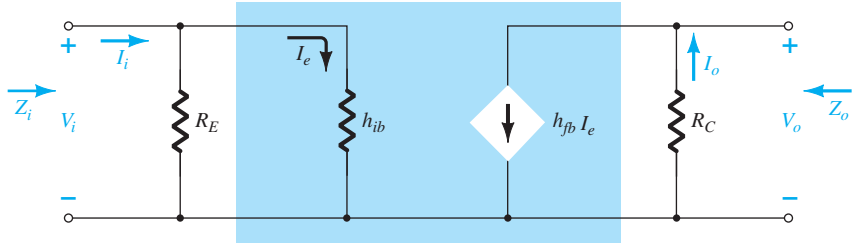



**FIG. 5.114**
*Substituting the approximate hybrid equivalent circuit into the ac equivalent network of Fig. 5.113.*

We have the following results from Fig. 5.114.

**$Z_i$**

$$\boxed{Z_i = R_E \| h_{ib}} \qquad \textbf{(5.163)}$$

**$Z_o$**

$$\boxed{Z_o = R_C} \qquad \textbf{(5.164)}$$

### $A_v$

$$V_o = -I_o R_C = -(h_{fb} I_e) R_C$$

with $$I_e = \frac{V_i}{h_{ib}} \quad \text{and} \quad V_o = -h_{fb}\frac{V_i}{h_{ib}} R_C$$

so that

$$\boxed{A_v = \frac{V_o}{V_i} = -\frac{h_{fb} R_C}{h_{ib}}} \tag{5.165}$$

### $A_i$

$$\boxed{A_i = \frac{I_o}{I_i} = h_{fb} \cong -1} \tag{5.166}$$

**EXAMPLE 5.21** For the network of Fig. 5.115, determine:

a. $Z_i$.
b. $Z_o$.
c. $A_v$.
d. $A_i$.

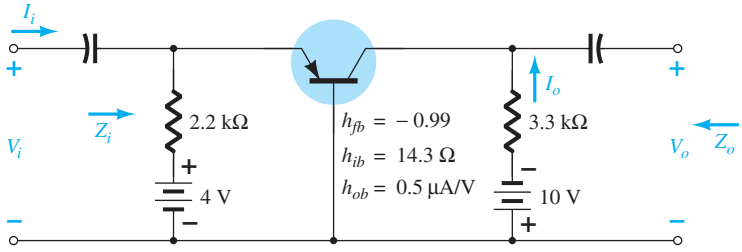



**FIG. 5.115**
*Example 5.21.*

**Solution:**

a. $Z_i = R_E \| h_{ib} = 2.2\,\text{k}\Omega \| 14.3\,\Omega = \mathbf{14.21\,\Omega} \cong h_{ib}$

b. $r_o = \dfrac{1}{h_{ob}} = \dfrac{1}{0.5\,\mu\text{A/V}} = \mathbf{2\,M\Omega}$

$$Z_o = \frac{1}{h_{ob}} \| R_C \cong R_C = \mathbf{3.3\,k\Omega}$$

c. $A_v = -\dfrac{h_{fb} R_C}{h_{ib}} = -\dfrac{(-0.99)(3.3\,\text{k}\Omega)}{14.21} = \mathbf{229.91}$

d. $A_i \cong h_{fb} = \mathbf{-1}$

The remaining configurations that were not analyzed in this section are left as an exercise in the problem section of this chapter. It is assumed that the analysis above clearly reveals the similarities in approach using the $r_e$ or approximate hybrid equivalent models, thereby removing any real difficulty with analyzing the remaining networks of the earlier sections.

## 5.21 COMPLETE HYBRID EQUIVALENT MODEL

The analysis of Section 5.20 was limited to the approximate hybrid equivalent circuit with some discussion about the output impedance. In this section, we employ the complete equivalent circuit to show the effect of $h_r$ and define in more specific terms the effect of $h_o$. It is important to realize that because the hybrid equivalent model has the same appearance for the common-base, common-emitter, and common-collector configurations, the equations developed in this section can be applied to each configuration. It is only necessary to

insert the parameters defined for each configuration. That is, for a common-base configuration, $h_{fb}$, $h_{ib}$, and so on, are employed, whereas for a common-emitter configuration, $h_{fe}$, $h_{ie}$, and so on, are used. Recall that Appendix A permits a conversion from one set to the other if one set is provided and the other is required.

Consider the general configuration of Fig. 5.116 with the two-port parameters of particular interest. The complete hybrid equivalent model is then substituted in Fig. 5.117 using parameters that do not specify the type of configuration. In other words, the solutions will be in terms of $h_i$, $h_r$, $h_f$, and $h_o$. Unlike the analysis of previous sections of this chapter, here the current gain $A_i$ will be determined first because the equations developed will prove useful in the determination of the other parameters.

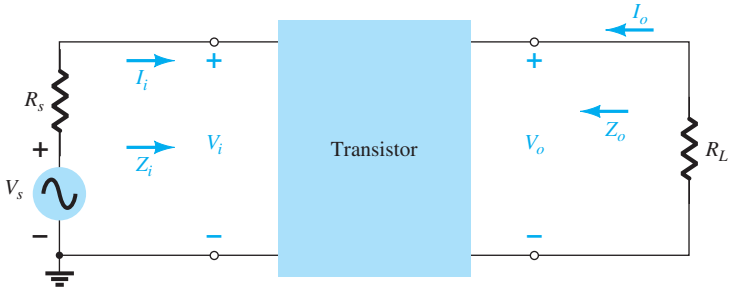



**FIG. 5.116**
*Two-port system.*

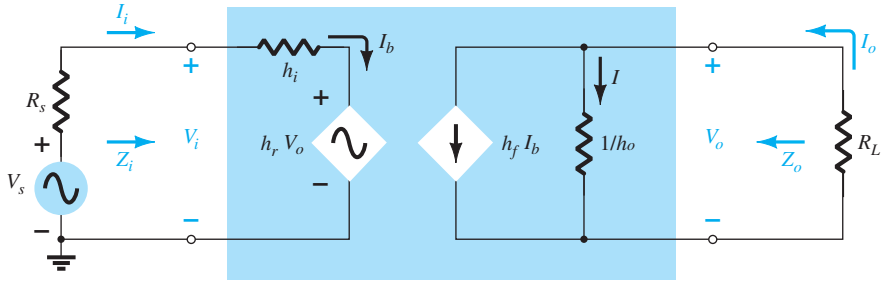



**FIG. 5.117**
*Substituting the complete hybrid equivalent circuit into the two-port system of Fig. 5.116.*

## Current Gain, $A_i = I_o/I_i$

Applying Kirchhoff's current law to the output circuit yields

$$I_o = h_f I_b + I = h_f I_i + \frac{V_o}{1/h_o} = h_f I_i + h_o V_o$$

Substituting $V_o = -I_o R_L$ gives

$$I_o = h_f I_i - h_o R_L I_o$$

Rewriting the equation above, we have

$$I_o + h_o R_L I_o = h_f I_i$$

and

$$I_o(1 + h_o R_L) = h_f I_i$$

so that

$$\boxed{A_i = \frac{I_o}{I_i} = \frac{h_f}{1 + h_o R_L}} \qquad \textbf{(5.167)}$$

Note that the current gain reduces to the familiar result of $A_i = h_f$ if the factor $h_o R_L$ is sufficiently small compared to 1.

## Voltage Gain, $A_v = V_o/V_i$

Applying Kirchhoff's voltage law to the input circuit results in

$$V_i = I_i h_i + h_r V_o$$

Substituting $I_i = (1 + h_oR_L)I_o/h_f$ from Eq. (5.167) and $I_o = -V_o/R_L$ from above results in

$$V_i = \frac{-(1 + h_oR_L)h_i}{h_fR_L}V_o + h_rV_o$$

Solving for the ratio $V_o/V_i$ yields

$$\boxed{A_v = \frac{V_o}{V_i} = \frac{-h_fR_L}{h_i + (h_ih_o - h_fh_r)R_L}} \qquad \textbf{(5.168)}$$

In this case, the familiar form of $A_v = -h_fR_L/h_i$ returns if the factor $(h_ih_o - h_fh_r)R_L$ is sufficiently small compared to $h_i$.

## Input Impedance, $Z_i = V_i/I_i$

For the input circuit,

$$V_i = h_iI_i + h_rV_o$$

Substituting $V_o = -I_oR_L$

we have $$V_i = h_iI_i - h_rR_LI_o$$

Because $$A_i = \frac{I_o}{I_i}$$

$$I_o = A_iI_i$$

so that the equation above becomes

$$V_i = h_iI_i - h_rR_LA_iI_i$$

Solving for the ratio $V_i/I_i$, we obtain

$$Z_i = \frac{V_i}{I_i} = h_i - h_rR_LA_i$$

and substituting

$$A_i = \frac{h_f}{1 + h_oR_L}$$

yields

$$\boxed{Z_i = \frac{V_i}{I_i} = h_i - \frac{h_fh_rR_L}{1 + h_oR_L}} \qquad \textbf{(5.169)}$$

The familiar form of $Z_i = h_i$ is obtained if the second factor in the denominator $(h_oR_L)$ is sufficiently smaller than one.

## Output Impedance, $Z_o = V_o/I_o$

The output impedance of an amplifier is defined to be the ratio of the output voltage to the output current with the signal $V_s$ set to zero. For the input circuit with $V_s = 0$,

$$I_i = -\frac{h_rV_o}{R_s + h_i}$$

Substituting this relationship into the equation from the output circuit yields

$$I_o = h_fI_i + h_oV_o$$

$$= -\frac{h_fh_rV_o}{R_s + h_i} + h_oV_o$$

and

$$\boxed{Z_o = \frac{V_o}{I_o} = \frac{1}{h_o - [h_fh_r/(h_i + R_s)]}} \qquad \textbf{(5.170)}$$

In this case, the output impedance is reduced to the familiar form $Z_o = 1/h_o$ for the transistor when the second factor in the denominator is sufficiently smaller than the first.

**EXAMPLE 5.22** For the network of Fig. 5.118, determine the following parameters using the complete hybrid equivalent model and compare to the results obtained using the approximate model.

a. $Z_i$ and $Z_i'$.
b. $A_v$.
c. $A_i = I_o/I_i$.
d. $Z_o'$ (within $R_C$) and $Z_o$ (including $R_C$).

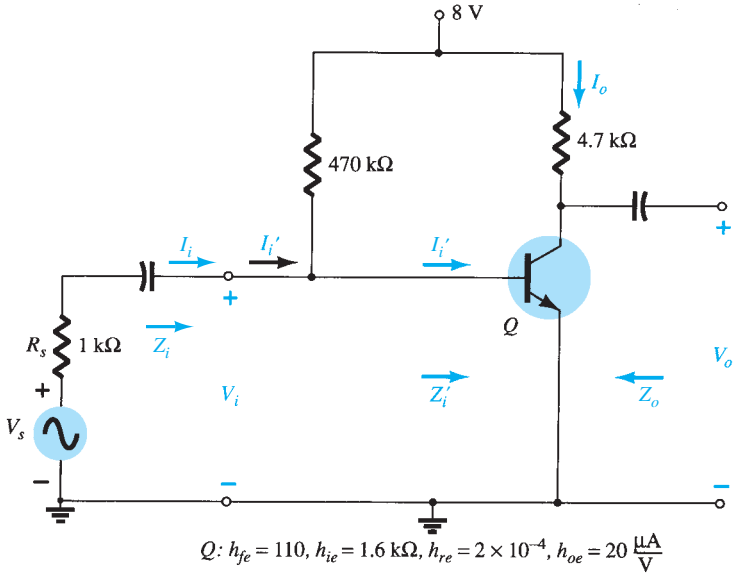



**FIG. 5.118**
*Example 5.22.*

***Solution:*** Now that the basic equations for each quantity have been derived, the order in which they are calculated is arbitrary. However, the input impedance is often a useful quantity to know, and therefore will be calculated first. The complete common-emitter hybrid equivalent circuit has been substituted and the network redrawn as shown in Fig. 5.119. A Thévenin equivalent circuit for the input section of Fig. 5.119 results in the input equivalent of Fig. 5.120 because $E_{\text{Th}} \cong V_s$ and $R_{\text{Th}} \cong R_s = 1\ \text{k}\Omega$ (a result of $R_B = 470\ \text{k}\Omega$ being much greater than $R_s = 1\ \text{k}\Omega$). In this example, $R_L = R_C$, and $I_o$ is defined as the current through $R_C$ as in previous examples of this chapter. The output impedance $Z_o$ as defined by Eq. (5.170) is for the output transistor terminals only. It does not include the effects of $R_C$. $Z_o$ is simply the parallel combination of $Z_o$ and $R_L$. The resulting configuration of

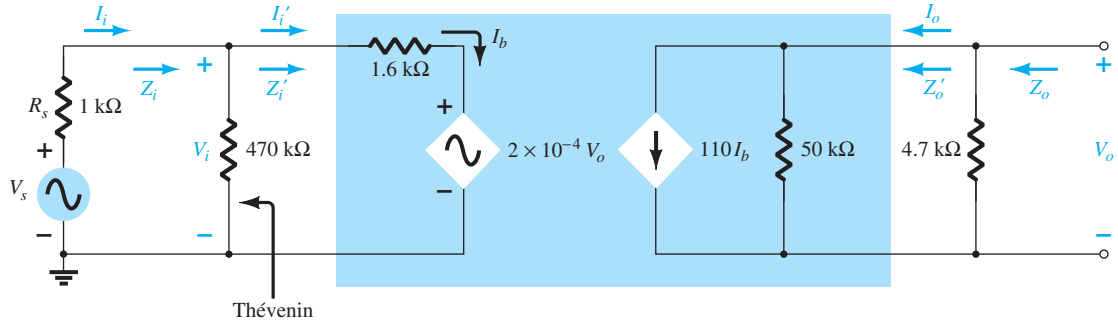



**FIG. 5.119**
*Substituting the complete hybrid equivalent circuit into the ac equivalent network of Fig. 5.118.*

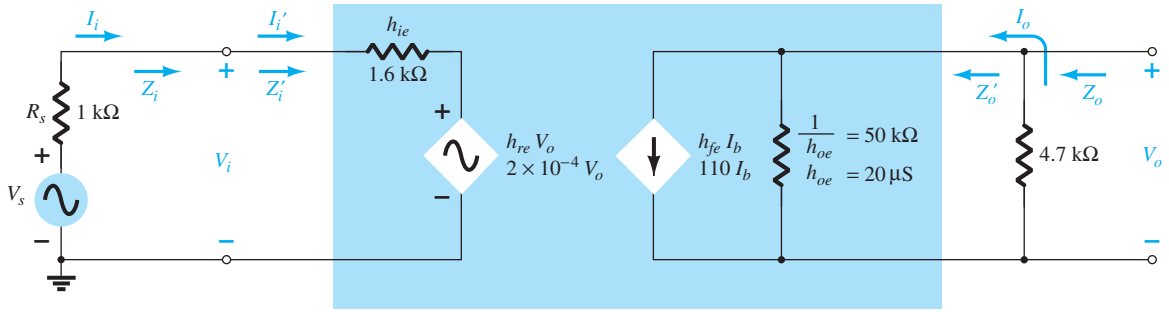



**FIG. 5.120**

*Replacing the input section of Fig. 5.119 with a Thévenin equivalent circuit.*

Fig. 5.120 is then an exact duplicate of the defining network of Fig. 5.117, and the equations derived above can be applied.

a. Eq. (5.169):

$$Z_i = \frac{V_i}{I_i} = h_{ie} - \frac{h_{fe}h_{re}R_L}{1 + h_{oe}R_L}$$

$$= 1.6\,\text{k}\Omega - \frac{(110)(2 \times 10^{-4})(4.7\,\text{k}\Omega)}{1 + (20\,\mu\text{S})(4.7\,\text{k}\Omega)}$$

$$= 1.6\,\text{k}\Omega - 94.52\,\Omega$$

$$= \mathbf{1.51\,k\Omega}$$

versus 1.6 kΩ using simply $h_{ie}$; and

$$Z_i' = 470\,\text{k}\Omega \| Z_i \cong Z_i = \mathbf{1.51\,k\Omega}$$

b. Eq. (5.168):

$$A_v = \frac{V_o}{V_i} = \frac{-h_{fe}R_L}{h_{ie} + (h_{ie}h_{oe} - h_{fe}h_{re})R_L}$$

$$= \frac{-(110)(4.7\,\text{k}\Omega)}{1.6\,\text{k}\Omega + [(1.6\,\text{k}\Omega)(20\,\mu\text{S}) - (110)(2 \times 10^{-4})]4.7\,\text{k}\Omega}$$

$$= \frac{-517 \times 10^3\,\Omega}{1.6\,\text{k}\Omega + (0.032 - 0.022)4.7\,\text{k}\Omega}$$

$$= \frac{-517 \times 10^3\,\Omega}{1.6\,\text{k}\Omega + 47\,\Omega}$$

$$= \mathbf{-313.9}$$

versus −323.125 using $A_v \cong -h_{fe}R_L/h_{ie}$.

c. Eq. (5.167):

$$A_i' = \frac{I_o}{I_i'} = \frac{h_{fe}}{1 + h_{oe}R_L} = \frac{110}{1 + (20\,\mu\text{S})(4.7\,\text{k}\Omega)}$$

$$= \frac{110}{1 + 0.094} = \mathbf{100.55}$$

versus 110 using simply $h_{fe}$. Because $470\,\text{k}\Omega \gg Z_i'$, $I_i \cong I_i'$ and $A_i \cong$ **100.55** also.

d. Eq. (5.170):

$$Z_o' = \frac{V_o}{I_o} = \frac{1}{h_{oe} - [h_{fe}h_{re}/(h_{ie} + R_s)]}$$

$$= \frac{1}{20\,\mu\text{S} - [(110)(2 \times 10^{-4})/(1.6\,\text{k}\Omega + 1\,\text{k}\Omega)]}$$

$$= \frac{1}{20\,\mu\text{S} - 8.46\,\mu\text{S}}$$

$$= \frac{1}{11.54\,\mu\text{S}}$$

$$= \mathbf{86.66\,k\Omega}$$

which is greater than the value determined from $1/h_{oe}$, 50 kΩ; and

$$Z_o = R_C \| Z_o' = 4.7\,\text{k}\Omega \| 86.66\,\text{k}\Omega = \mathbf{4.46\,k\Omega}$$

versus 4.7 kΩ using only $R_C$.

Note from the results above that the approximate solutions for $A_v$ and $Z_i$ were very close to those calculated with the complete equivalent model. In fact, even $A_i$ was off by less than 10%. The higher value of $Z_o'$ only contributed to our earlier conclusion that $Z_o'$ is often so high that it can be ignored compared to the applied load. However, keep in mind that when there is a need to determine the effect of $h_{re}$ and $h_{oe}$, the complete hybrid equivalent model must be used, as described earlier.

The specification sheet for a particular transistor typically provides the common-emitter parameters as noted in Fig. 5.92. The next example will employ the same transistor parameters appearing in Fig. 5.118 in a *pnp* common-base configuration to introduce the parameter conversion procedure and emphasize the fact that the hybrid equivalent model maintains the same layout.

**EXAMPLE 5.23** For the common-base amplifier of Fig. 5.121, determine the following parameters using the complete hybrid equivalent model and compare the results to those obtained using the approximate model.

a. $Z_i$
b. $A_i$
c. $A_v$.
d. $Z_o$

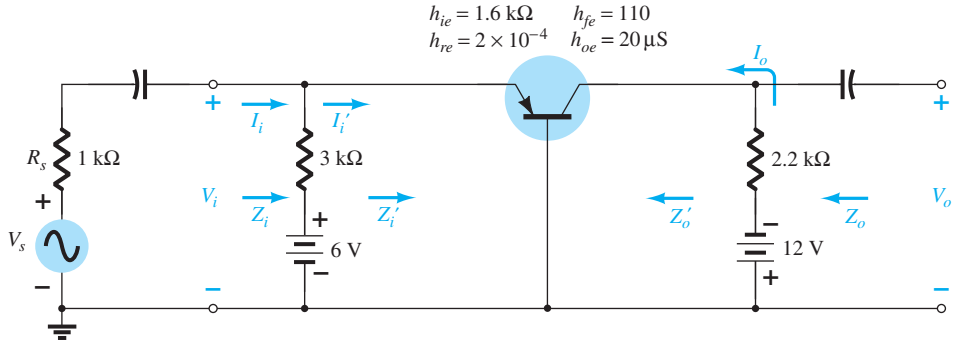



**FIG. 5.121**
*Example 5.23.*

***Solution:*** The common-base hybrid parameters are derived from the common-emitter parameters using the approximate equations of Appendix B:

$$h_{ib} \cong \frac{h_{ie}}{1 + h_{fe}} = \frac{1.6\,\text{k}\Omega}{1 + 110} = \mathbf{14.41\ \Omega}$$

Note how closely the magnitude compares with the value determined from

$$h_{ib} = r_e = \frac{h_{ie}}{\beta} = \frac{1.6\,\text{k}\Omega}{110} = 14.55\ \Omega$$

Also,

$$h_{rb} \cong \frac{h_{ie}h_{oe}}{1 + h_{fe}} - h_{re} = \frac{(1.6\,\text{k}\Omega)(20\,\mu\text{S})}{1 + 110} - 2 \times 10^{-4}$$

$$= \mathbf{0.883 \times 10^{-4}}$$

$$h_{fb} \cong \frac{-h_{fe}}{1 + h_{fe}} = \frac{-110}{1 + 110} = \mathbf{-0.991}$$

$$h_{ob} \cong \frac{h_{oe}}{1 + h_{fe}} = \frac{20\,\mu\text{S}}{1 + 110} = \mathbf{0.18\ \mu S}$$

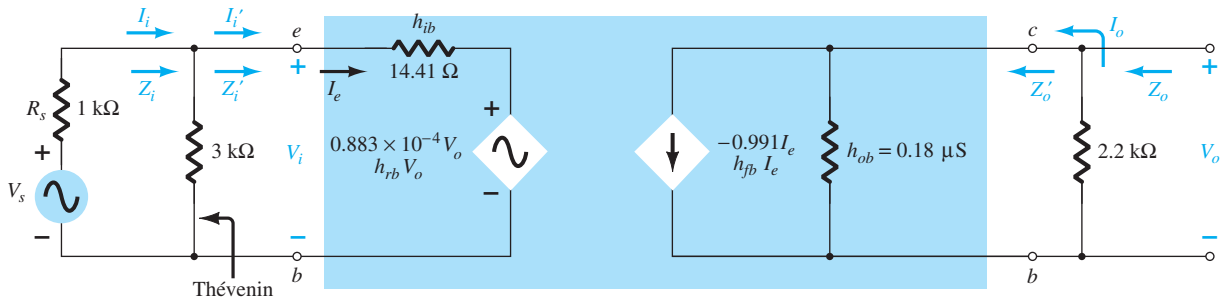



**FIG. 5.122**
*Small-signal equivalent for the network of Fig. 5.121.*

Substituting the common-base hybrid equivalent circuit into the network of Fig. 5.121 results in the small-signal equivalent network of Fig. 5.122. The Thévenin network for the input circuit results in $R_{\text{Th}} = 3\,\text{k}\Omega \| 1\,\text{k}\Omega = 0.75\,\text{k}\Omega$ for $R_s$ in the equation for $Z_o$.

a. Eq. (5.169):

$$Z_i' = \frac{V_i}{I_i'} = h_{ib} - \frac{h_{fb}h_{rb}R_L}{1 + h_{ob}R_L}$$

$$= 14.41\ \Omega - \frac{(-1.991)(0.883 \times 10^{-4})(2.2\,\text{k}\Omega)}{1 + (0.18\,\mu\text{S})(2.2\,\text{k}\Omega)}$$

$$= 14.41\ \Omega + 0.19\ \Omega$$

$$= 14.60\ \Omega$$

versus 14.41 Ω using $Z_i \cong h_{ib}$; and

$$Z_i = 3\,\text{k}\Omega \| Z_i' \cong Z_i' = \mathbf{14.60\ \Omega}$$

b. Eq. (5.167):

$$A_i' = \frac{I_o}{I_i'} = \frac{h_{fb}}{1 + h_{ob}R_L}$$

$$= \frac{-0.991}{1 + (0.18\,\mu\text{S})(2.2\,\text{k}\Omega)}$$

$$= -0.991$$

Because $3\,\text{k}\Omega \gg Z_i'$, $I_i \cong I_i'$ and $A_i = I_o/I_i \cong \mathbf{-1}$.

c. Eq. (5.168):

$$A_v = \frac{V_o}{V_i} = \frac{-h_{fb}R_L}{h_{ib} + (h_{ib}h_{ob} - h_{fb}h_{rb})R_L}$$

$$= \frac{-(-0.991)(2.2\,\text{k}\Omega)}{14.41\ \Omega + [(14.41\,\Omega)(0.18\,\mu\text{S}) - (-0.991)(0.883 \times 10^{-4})]2.2\,\text{k}\Omega}$$

$$= \mathbf{149.25}$$

versus 151.3 using $A_v \cong -h_{fb}R_L/h_{ib}$.

d. Eq. (5.170):

$$Z_o' = \frac{1}{h_{ob} - [h_{fb}h_{rb}/(h_{ib} + R_s)]}$$

$$= \frac{1}{0.18\,\mu\text{S} - [(-0.991)(0.883 \times 10^{-4})/(14.41\ \Omega + 0.75\,\text{k}\Omega)]}$$

$$= \frac{1}{0.295\,\mu\text{S}}$$

$$= \mathbf{3.39\ \text{M}\Omega}$$

versus 5.56 MΩ using $Z_o' \cong 1/h_{ob}$. For $Z_o$ as defined by Fig. 5.122,

$$Z_o = R_C \| Z_o' = 2.2\,\text{k}\Omega \| 3.39\,\text{M}\Omega = \mathbf{2.199\ \text{k}\Omega}$$

versus 2.2 kΩ using $Z_o \cong R_C$.

## 5.22 HYBRID $\pi$ MODEL

The last transistor model to be introduced is the hybrid $\pi$ model of Fig. 5.123 which includes parameters that do not appear in the other two models primarily to provide a more accurate model for high-frequency effects.

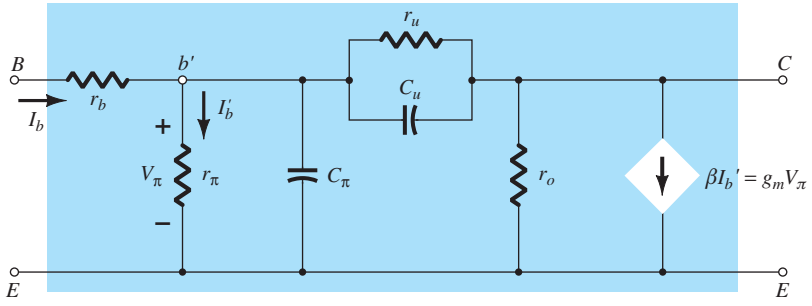



**FIG. 5.123**

*Giacoletto (or hybrid $\pi$) high-frequency transistor small-signal ac equivalent circuit.*

### $r_\pi$, $r_o$, $r_b$, and $r_u$

The resistors $r_\pi$, $r_o$, $r_b$, and $r_u$ are the resistances between the indicated terminals of the device when the device is in the active region. The resistance $r_\pi$ (using the symbol $\pi$ to agree with the hybrid $\pi$ terminology) is simply $\beta r_e$ as introduced for the common-emitter $r_e$ model.

That is,

$$r_\pi = \beta r_e \tag{5.171}$$

The output resistance $r_o$ is the output resistance normally appearing across an applied load. Its value, which typically lies between 5 kΩ and 40 kΩ, is determined from the hybrid parameter $h_{oe}$, the Early voltage, or the output characteristics.

The resistance $r_b$ includes the base contact, base bulk, and base spreading resistance levels. The first is due to the actual connection to the base. The second includes the resistance from the external terminal to the active region of the transistor, and the last is the actual resistance within the active base region. It is typically a few ohms to tens of ohms.

The resistance $r_u$ (the subscript $u$ refers to the *union* it provides between collector and base terminals) is a very large resistance and provides a feedback path from output to input circuits in the equivalent model. It is typically larger than $\beta r_o$, which places it in the megohm range.

### $C_\pi$ and $C_u$

All the capacitors that appear in Fig. 5.123 are stray parasitic capacitors between the various junctions of the device. They are all capacitive effects that really only come into play at high frequencies. For low to mid-frequencies their reactance is very large, and they can be considered open circuits. The capacitor $C_\pi$ across the input terminals can range from a few *pF* to tens of *pF*. The capacitor $C_u$ from base to collector is usually limited to a few *pF* but is magnified at the input and output by an effect called the Miller effect, to be introduced in Chapter 9.

### $\beta I_b'$ or $g_m V_\pi$

It is important to note in Fig. 5.123 that the controlled source can be a voltage-controlled current source (VCCS) or a current-controlled current source (CCCS), depending on the parameters employed.

Note the following parameter equivalence in Fig. 5.123:

$$g_m = \frac{1}{r_e} \tag{5.172}$$

and
$$r_o = \frac{1}{h_{oe}} \tag{5.173}$$

with
$$\frac{r_\pi}{r_\pi + r_u} \cong \frac{r_\pi}{r_u} \cong h_{re} \tag{5.174}$$

Take particular note of the fact that the equivalent sources $\beta I_b'$ and $g_m V_\pi$ are both controlled current sources. One is controlled by a current at another place in the network and the other by a voltage at the input side of the network. The equivalence between the two is defined by

$$\beta I_b' = \frac{1}{r_e} \cdot r_e \beta I_b' = g_m I_b' \beta r_e = g_m (I_b' r_\pi) = g_m V_\pi$$

For the broad range of low- to mid-frequency analysis, the effect of the stray capacitive effects can be ignored due to the very high reactance levels associated with each. The resistance $r_b$ is usually small enough with other series elements to be ignored while the resistance $r_u$ is usually large enough compared to parallel elements to be ignored. The result is an equivalent network similar to the $r_e$ model introduced and applied in this chapter.

In Chapter 9, when high-frequency effects are considered, the hybrid $\pi$ model will be the model of choice.

## 5.23 VARIATIONS OF TRANSISTOR PARAMETERS

A variety of curves can be drawn to show the variations of the transistor parameters with temperature, frequency, voltage, and current. The most interesting and useful at this stage of the development include the variations with junction temperature and collector voltage and current.

The effect of the collector current on the $r_e$ model and hybrid equivalent model is shown in Fig. 5.124. Take careful note of the logarithmic scale on the vertical and horizontal axes. Logarithmic scales will be examined in detail in Chapter 9. The parameters have all been normalized (a process described in detail in Section 9.5) to unity so that the relative change in magnitude with collector current can easily be determined. On each set of curves, such as in Figs. 5.124 to 5.126, the operating point at which the parameters were determined is always indicated. For this particular situation, the quiescent point is at the fairly typical values of $V_{CE} = 5.0$ V and $I_C = 1.0$ mA. Because the frequency and temperature of operation

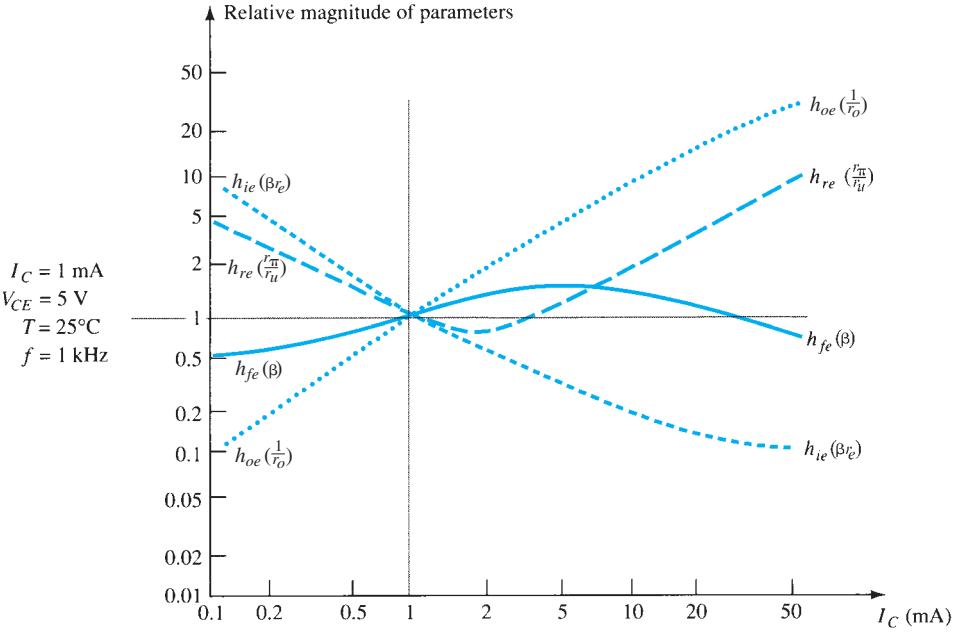



**FIG. 5.124**
*Hybrid parameter variations with collector current.*

also affect the parameters, these quantities are also indicated on the curves. Figure 5.124 shows the variation of the parameters with collector current. Note that at $I_C = 1$ mA the value of all the parameters has been normalized to 1 on the vertical axis. The result is that the magnitude of each parameter is compared to the values at the defined operating point. Because manufacturers typically use the hybrid parameters for plots of this type, they are the curves of choice in Fig. 5.124. However, to broaden the use of the curves the $r_e$ and hybrid $\pi$ equivalent parameters have also been added.

At first glance it is particularly interesting to note that:

***The parameter $h_{fe}(\beta)$ varies the least of all the parameters of a transistor equivalent circuit when plotted against variations in collector current.***

Figure 5.124 clearly reveals that for the full range of collector current the parameter $h_{fe}(\beta)$ varies from 0.5 of its $Q$-point value to a peak of about 1.5 times that value at a current of about 6 mA. For a transistor with a $\beta$ of 100, it therefore varies from about 50 to 150. This seems like quite a bit, but look at $h_{oe}$, which jumps to almost 40 times its $Q$-point value at a collector current of 50 mA.

Figure 5.124 also shows that $h_{oe}(1/r_o)$ and $h_{ie}(\beta r_e)$ vary the most for the chosen current range. The parameter $h_{ie}$ varies from about 10 times its $Q$-point value down to about one tenth the $Q$ point value at 50 mA. This variation, however, should be expected because we know that the value of $r_e$ is directly related to the emitter current by $r_e = 26\,\text{mV}/I_E$. As $I_E(\cong I_C)$ increases, the value of $r_e$ and therefore $\beta r_e$ will decrease, as shown in Fig. 5.124.

Keep in mind as you review the curve of $h_{oe}$ versus current that the actual output resistance $r_o$ is $1/h_{oe}$. Therefore, as the curve increases with current, the value of $r_o$ becomes less and less. Because $r_o$ is a parameter that normally appears in parallel with the applied load, decreasing values of $r_o$ can become a critical problem. The fact that $r_o$ has dropped to almost 1/40 of its value at the $Q$-point could spell a real reduction in gain at 50 mA.

The parameter $h_{re}$ varies quite a bit, but because its $Q$-point value is usually small enough to permit ignoring its effect, it is a parameter that is only of concern for collector currents that are much less, or quite a bit more, than the $Q$-point level.

This may seem like an extensive description of a set of characteristic curves. However, experience has revealed that graphs of this nature are too often reviewed without taking the time to fully appreciate the broad impact of what they are providing. These plots reveal a lot of information that could be extremely useful in the design process.

Figure 5.125 shows the variation in magnitude of the parameters due to changes in collector-to-emitter voltage. This set of curves is normalized at the same operating point as the curves of Fig. 5.124 to permit comparisons between the two. In this case, however, the vertical scale is in percent rather than whole numbers. The 200% level defines a set of parameters twice that at the 100% level. A level of 1000% would reflect a 10:1 change. Note that $h_{fe}$ and $h_{ie}$ are relatively steady in magnitude with variations in collector-to-emitter voltage, whereas for changes in collector current the variation is a great deal more

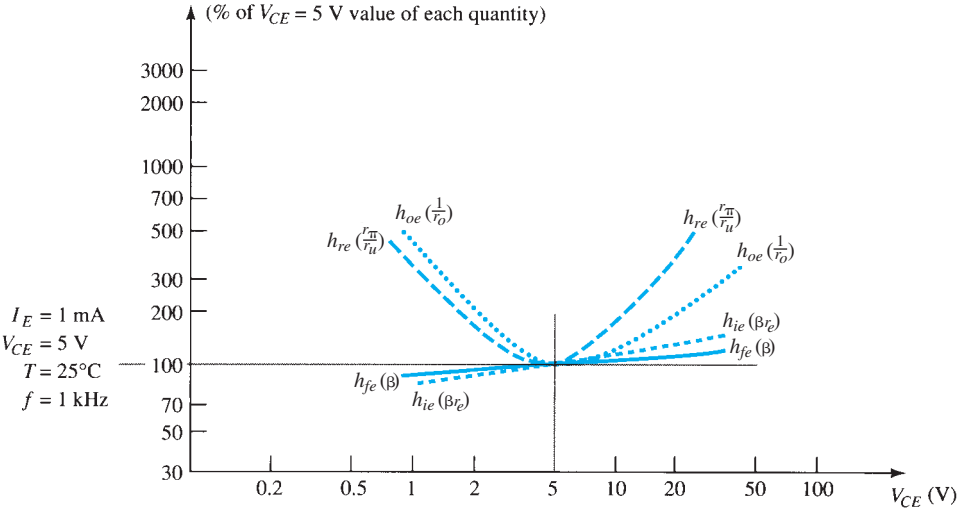



**FIG. 5.125**

*Hybrid parameter variations with collector–emitter potential.*

significant. In other words, if you want a parameter such as $h_{ie}(\beta r_e)$ to remain fairly steady, keep the variation of $I_C$ to a minimum while worrying less about variations in the collector-to-emitter voltage. The variation of $h_{oe}$ and $h_{ie}$ remains significant for the indicated range of collector-to-emitter voltage.

In Fig. 5.126, the variation in parameters is plotted for changes in junction temperature. The normalization value is taken to be room temperature, $T = 25°C$. The horizontal scale is now a linear scale rather than the logarithmic scale employed in the two previous figures. In general:

***All the parameters of a hybrid transistor equivalent circuit increase with temperature.***

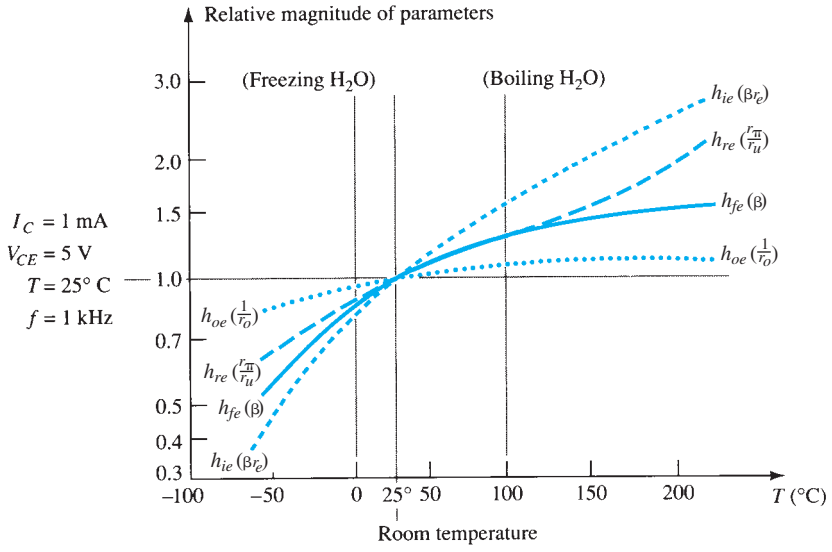



**FIG. 5.126**
*Hybrid parameter variations with temperature.*

However, again keep in mind that the actual output resistance $r_o$ is inversely related to $h_{oe}$, so its value drops with an increase in $h_{oe}$. The greatest change is in $h_{ie}$, although note that the range of the vertical scale is considerably less than in the other plots. At a temperature of 200°C the value of $h_{ie}$ is almost 3 times its $Q$-point value, but in Fig. 5.124 parameters jumped to almost 40 times the $Q$-point value.

Of the three parameters, therefore, the variation in collector current has by far the greatest effect on the parameters of a transistor equivalent circuit. Temperature is always a factor, but the effect of the collector current can be significant.

## 5.24 TROUBLESHOOTING

Although the terminology *troubleshooting* suggests that the procedures to be described are designed simply to isolate a malfunction, it is important to realize that the same techniques can be applied to ensure that a system is operating properly. In any case, the testing, checking, and isolating procedures require an understanding of what to expect at various points in the network in both the dc and ac domains. In most cases, a network operating correctly in the dc mode will also behave properly in the ac domain.

***In general, therefore, if a system is not working properly, first disconnect the ac source and check the dc biasing levels.***

In Fig. 5.127 we have four transistor configurations with specific voltage levels provided as measured by a DMM in the dc mode. The first test of any transistor network is to simply measure the base-to-emitter voltage of the transistor. The fact that it is only 0.3 V in this case suggests that the transistor is not "on" and perhaps sitting in its saturation mode. If this is a switching design then the result is expected, but if in the amplifier mode there is an open connection preventing the base voltage from reaching an operating level.

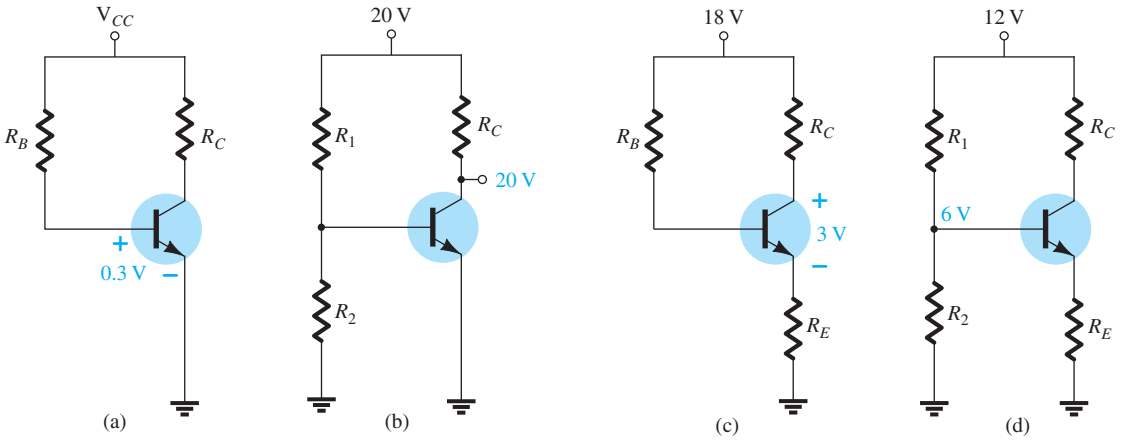



**FIG. 5.127**

*Checking the dc levels to determine if a network is properly biased.*

In Fig. 5.127b the fact that the voltage at the collector equals the supply voltage reveals that there is no drop across the resistor $R_C$ and the collector current is zero. The resistor $R_C$ is connected properly because it made the connection from the dc source to the collector. However, any one of the other elements may not have been connected properly, resulting in the absence of a base or collector current. In Fig. 5.127c the voltage drop across the collector-to-emitter voltage is too small compared with the applied dc voltage. Normally the voltage $V_{CE}$ is in the mid-range of perhaps 6 V to 14 V. A reading of 18 V would cause the same concern as the reading of 3 V. The fact that the voltage levels exist at all suggests that all the elements are connected but the value of one or more of the resistive elements may be wrong. In Fig. 5.127d we find that the voltage at the base is exactly half the supply voltage. We know from this chapter that the resistance $R_E$ will reflect back to the base by a factor of beta and appear in parallel with $R_2$. The result would be a base voltage less than half the supply voltage. The measurement suggests that the base lead is not connected to the voltage divider, causing an even split of the 20-V source.

In a typical laboratory setting, the ac response at various points in the network is checked with an oscilloscope as shown in Fig. 5.128. Note that the black (gnd) lead of the oscilloscope is connected directly to ground and the red lead is moved from point to point in the

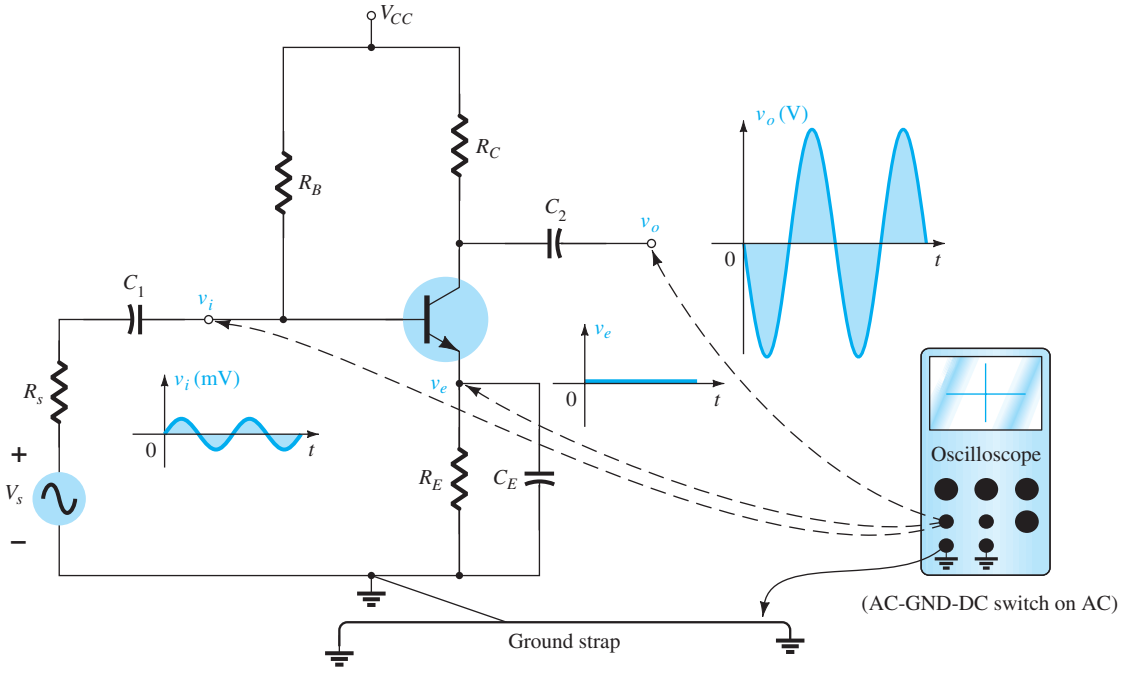



**FIG. 5.128**

*Using the oscilloscope to measure and display various voltages of a BJT amplifier.*

network, providing the patterns appearing in Fig. 5.128. The vertical channels are set in the ac mode to remove any dc component associated with the voltage at a particular point. The small ac signal applied to the base is amplified to the level appearing from collector to ground. Note the difference in vertical scales for the two voltages. There is no ac response at the emitter terminal due to the short-circuit characteristics of the capacitor at the applied frequency. The fact that $v_o$ is measured in volts and $v_i$ in millivolts suggests a sizable gain for the amplifier. In general, the network appears to be operating properly. If desired, the dc mode of the multimeter could be used to check $V_{BE}$ and the levels of $V_B$, $V_{CE}$, and $V_E$ to review whether they lie in the expected range. Of course, the oscilloscope can also be used to compare dc levels simply by switching to the dc mode for each channel.

A poor ac response can be due to a variety of reasons. In fact, there may be more than one problem area in the same system. Fortunately, however, with time and experience, the probability of malfunctions in some areas can be predicted, and an experienced person can isolate problem areas fairly quickly.

In general, there is nothing mysterious about the general troubleshooting process. If you decide to follow the ac response, it is good procedure to start with the applied signal and progress through the system toward the load, checking critical points along the way. An unexpected response at some point suggests that the network is fine up to that area, thereby defining the region that must be investigated further. The waveform obtained on the oscilloscope will certainly help in defining the possible problems with the system.

If the response for the network of Fig. 5.128 is as appears in Fig. 5.129, the network has a malfunction that is probably in the emitter area. An ac response across the emitter is unexpected, and the gain of the system as revealed by $v_o$ is much lower. Recall for this configuration that the gain is much greater if $R_E$ is bypassed. The response obtained suggests that $R_E$ is not bypassed by the capacitor, and the terminal connections of the capacitor and the capacitor itself should be checked. In this case, a checking of the dc levels will probably not isolate the problem area because the capacitor has an "open-circuit" equivalent for dc. In general, prior knowledge of what to expect, familiarity with the instrumentation, and, most important, experience are all factors that contribute to the development of an effective approach to the art of troubleshooting.

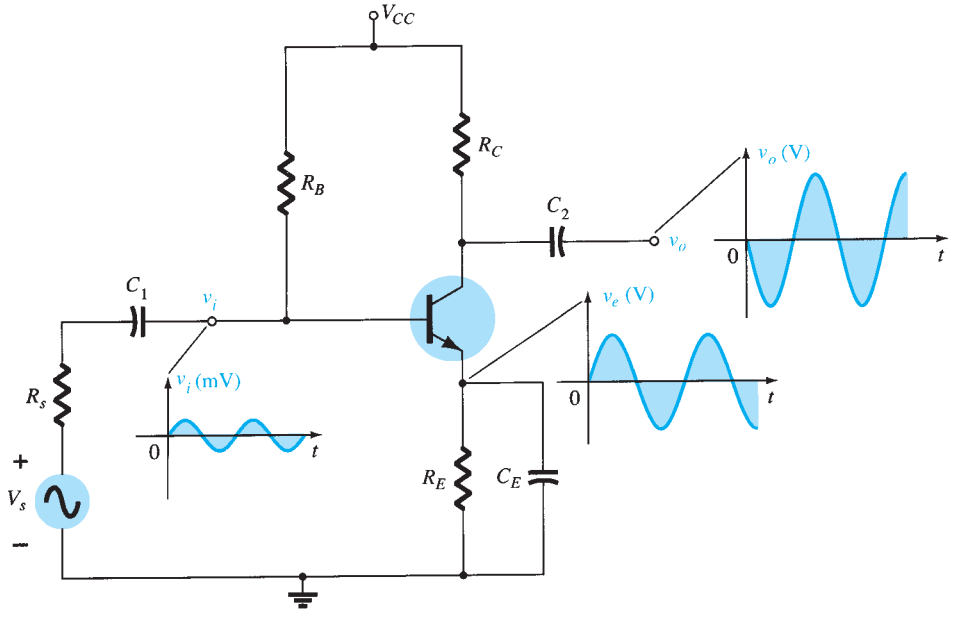



**FIG. 5.129**

*The waveforms resulting from a malfunction in the emitter area.*

## 5.25 PRACTICAL APPLICATIONS

### Audio Mixer

When two or more signals are to be combined into a single audio output, mixers such as shown in Fig. 5.130 are employed. The potentiometers at the input are the volume controls for each channel, with potentiometer $R_3$ included to provide additional balance between

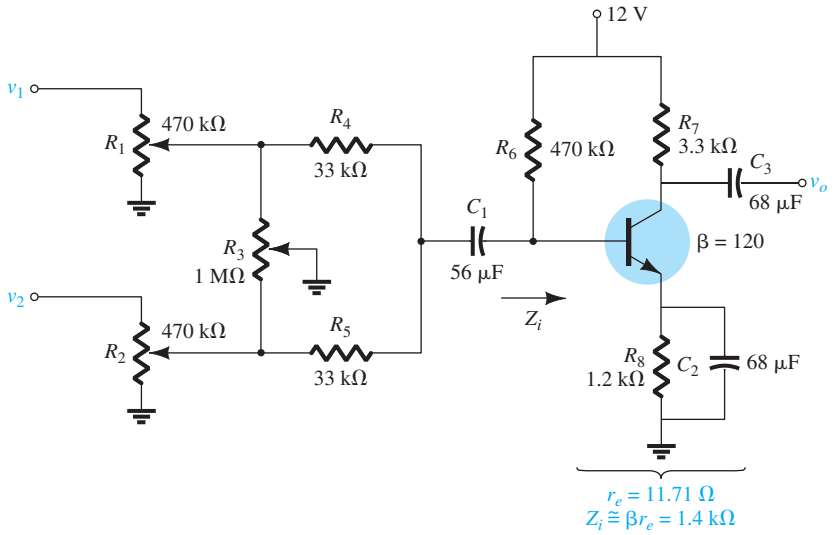



**FIG. 5.130**
*Audio mixer.*

the two signals. Resistors $R_4$ and $R_5$ are there to ensure that one channel does not load down the other, that is, to ensure that one signal does not appear as a load to the other, draw power, and affect the desired balance on the mixed signal.

The effect of resistors $R_4$ and $R_5$ is an important one that should be discussed in some detail. A dc analysis of the transistor configuration results in $r_e = 11.71\ \Omega$, which will establish an input impedance to the transistor of about 1.4 kΩ. The parallel combination of $R_6 \| Z_i$ is also approximately 1.4 kΩ. Setting both volume controls to their maximum value and the balance control $R_3$ to its midpoint result in the equivalent network of Fig. 5.131a. The signal at $v_1$ is assumed to be a low-impedance microphone with an internal resistance of 1 kΩ. The signal at $v_2$ is assumed to be a guitar amplifier with a higher internal impedance of 10 kΩ. Because the 470-kΩ and 500-kΩ resistors are in parallel for the above conditions, they can be combined and replaced with a single resistor of about 242 kΩ. Each source will then have an equivalent such as shown in Fig. 5.131b for the microphone. Applying Thévenin's theorem shows that it is an excellent approximation to simply drop the 242 kΩ and assume that the equivalent network is as shown for each channel. The result is the equivalent network of Fig. 5.131c for the input section of the mixer. Applying the superposition theorem results in the following equation for the ac voltage at the base of the transistor:

$$v_b = \frac{(1.4\ \text{k}\Omega \| 43\ \text{k}\Omega)v_{s_1}}{34\ \text{k}\Omega + (1.4\ \text{k}\Omega \| 43\ \text{k}\Omega)} + \frac{(1.4\ \text{k}\Omega \| 34\ \text{k}\Omega)v_{s_2}}{43\ \text{k}\Omega + (1.4\ \text{k}\Omega \| 34\ \text{k}\Omega)}$$
$$= 38 \times 10^{-3} v_{s_1} + 30 \times 10^{-3} v_{s_2}$$

With $r_e = 11.71\ \Omega$, the gain of the amplifier is $-R_C/r_e = 3.3\ \text{k}\Omega/11.71\ \Omega = -281.8$, and the output voltage is

$$v_o = -10.7 v_{s_1} - 8.45 v_{s_2}$$

which provides a pretty good balance between the two signals, even though they have a 10:1 ratio in internal impedance. In general, the system will respond quite well. However, if we now remove the 33-kΩ resistors from the diagram of Fig. 5.131c, the equivalent network of Fig. 5.132 results, and the following equation for $v_b$ is obtained using the superposition theorem:

$$v_b = \frac{(1.4\ \text{k}\Omega \| 10\ \text{k}\Omega)v_{s_1}}{1\ \text{k}\Omega + 1.4\ \text{k}\Omega \| 10\ \text{k}\Omega} + \frac{(1.4\ \text{k}\Omega \| 1\ \text{k}\Omega)v_{s_2}}{10\ \text{k}\Omega + (1.4\ \text{k}\Omega \| 1\ \text{k}\Omega)}$$
$$= 0.55 v_{s_1} + 0.055 v_{s_2}$$

Using the same gain as before, we obtain the output voltage as

$$v_o = 155 v_{s_1} + 15.5 v_{s_2} \cong 155 v_{s_1}$$

which indicates that the microphone will be quite loud and clear and the guitar input essentially lost.

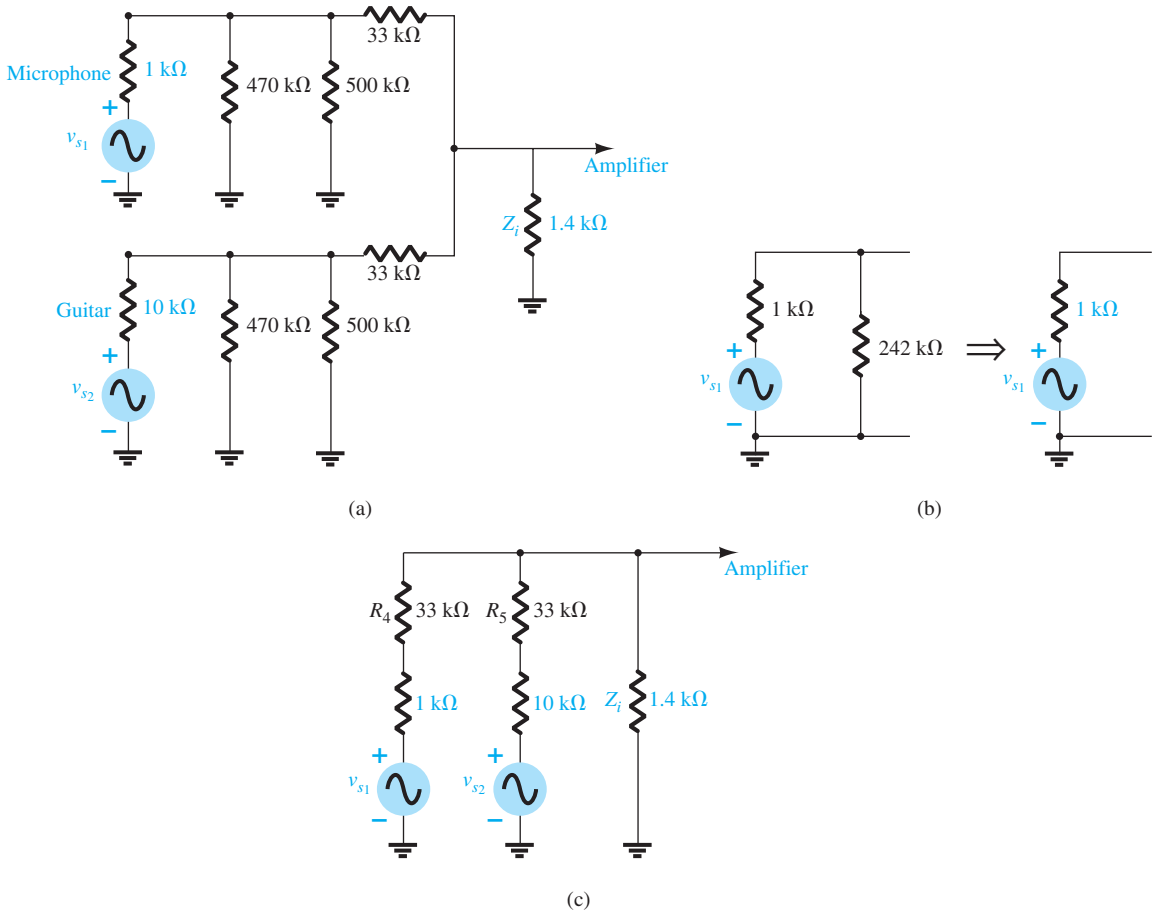



**FIG. 5.131**

*(a) Equivalent network with $R_3$ set at the midpoint and the volume controls on their maximum settings; (b) finding the Thévenin equivalent for channel 1; (c) substituting the Thévenin equivalent networks into Fig. 5.131a.*

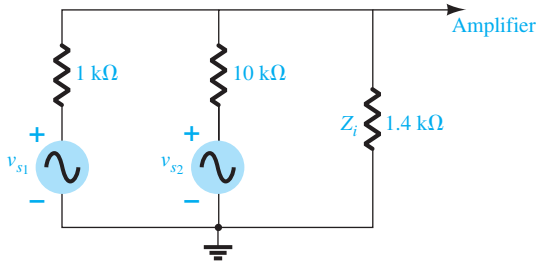



**FIG. 5.132**

*Redrawing the network of Fig. 5.131c with the 33-kΩ resistors removed.*

The importance of the 33-kΩ resistors is therefore defined. It makes each applied signal appear to have a similar impedance level so that there is good balance at the output. One might suggest that the larger resistor improves the balance. However, even though the balance at the base of the transistor may be better, the strength of the signal at the base of the transistor will be less, and the output level reduced accordingly. In other words, the choice of resistors $R_4$ and $R_5$ is a give-and-take situation between the input level at the base of the transistor and the balance of the output signal.

To demonstrate that the capacitors are truly short-circuit equivalents in the audio range, substitute a very low audio frequency of 100 Hz into the reactance equation of a 56-$\mu$F capacitor:

$$X_C = \frac{1}{2\pi fC} = \frac{1}{2\pi(100\text{ Hz})(56\ \mu\text{F})} = 28.42\ \Omega$$

A level of 28.42 Ω compared to any of the neighboring impedances is certainly small enough to be ignored. Higher frequencies will have even less effect.

A similar mixer will be discussed in connection with the junction field effect transistor (JFET) in the following chapter. The major difference will be the fact that the input impedance of the JFET can be approximated by an open circuit rather than the rather low-level input impedance of the BJT configuration. The result will be a higher signal level at the input to the JFET amplifier. However, the gain of the FET is much less than that of the BJT transistor, resulting in output levels that are actually quite similar.

## Preamplifier

The primary function of a **preamplifier** is as its name implies: **an amplifier used to pick up the signal from its primary source and then operate on it in preparation for its passage into the amplifier section.** Typically, a preamplifier will amplify the signal, control its volume, perhaps change its input impedance characteristics, and if necessary determine its route through the stages to follow—in total, a stage of any system with a multitude of functions.

A preamplifier such as shown in Fig. 5.133 is often used with dynamic microphones to bring the signal level up to levels that are suitable for further amplification or power amplifiers. Typically, dynamic microphones are low-impedance microphones because their internal resistance is determined primarily by the winding of the voice coil. The basic construction consists of a voice coil attached to a small diaphragm that is free to move within a permanent magnet. When one speaks into the microphone, the diaphragm moves accordingly and causes the voice coil to move in the same manner within the magnetic field. In accord with Faraday's law, a voltage will be induced across the coil that will carry the audio signal.

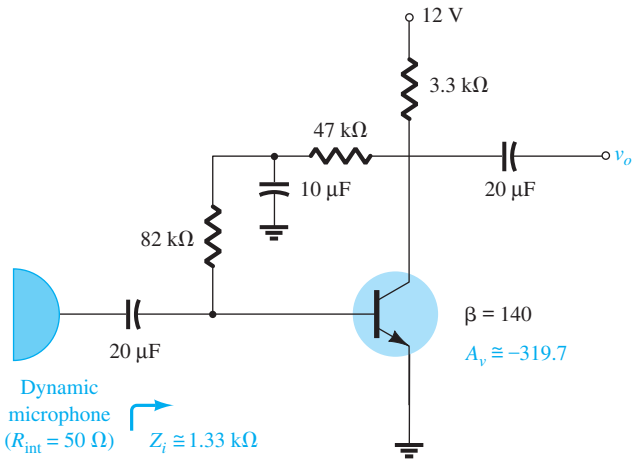



**FIG. 5.133**
*Preamplifier for a dynamic microphone.*

Because it is a low-impedance microphone, the input impedance of the transistor amplifier does not have to be that high to pick up most of the signal. Because the internal impedance of a dynamic microphone may be as low as 20 Ω to 100 Ω, most of the signal would be picked up with an amplifier having an input impedance as low as 1 to 2 kΩ. This, in fact, is the case for the preamplifier of Fig. 5.133. For dc biasing conditions, the collector dc feedback configuration was chosen because of its high stablity characteristics.

In the ac domain, the 10-$\mu$F capacitor will assume a short-circuit state (on an approximate basis), placing the 82-kΩ resistor across the input impedance of the transistor and the 47 kΩ across the output of the transistor. A dc analysis of the transistor configuration results in $r_e = 9.64\ \Omega$, giving an ac gain determined by

$$A_v = -\frac{(47\ \text{k}\Omega \,\|\, 3.3\ \text{k}\Omega)}{9.64\ \Omega} = \mathbf{-319.7}$$

which is excellent for this application. Of course, the gain will drop when this pickup stage of the design is connected to the input of the amplifier section. That is, the input resistance

of the next stage will appear in parallel with the 47-kΩ and 3.3-kΩ resistors and will drop the gain below the unloaded level of 319.7.

The input impedance of the preamplifier is determined by

$$Z_i = 82\,\text{k}\Omega \| \beta r_e = 82\,\text{k}\Omega \| (140)(9.64\ \Omega) = 82\,\text{k}\Omega \| 1.34\,\text{k}\Omega = \mathbf{1.33\,k\Omega}$$

which is also fine for most low-impedance dynamic microphones. In fact, for a microphone with an internal impedance of 50 Ω, the signal at the base would be over 98% of that available. This discussion is important because if the impedance of the microphone is a great deal more, say, 1 kΩ, the preamplifier would have to be designed differently to ensure that the input impedance was at least 10 kΩ or more.

## Random-Noise Generator

There is often a need for a random-noise generator to test the response of a speaker, microphone, filter, and, in fact, any system designed to work over a wide range of frequencies. A **random-noise generator** is just as its name implies: **a generator that generates signals of random amplitude and frequency.** The fact that these signals are usually totally unintelligible and unpredictable is the reason that they are simply referred to as *noise*. **Thermal noise** is noise generated due to thermal effects resulting from the interaction between free electrons and the vibrating ions of a material in conduction. The result is an uneven flow of electrons through the medium, which will result in a varying potential across the medium. In most cases, these randomly generated signals are in the microvolt range, but with sufficient amplification they can wreak havoc on a system's response. This thermal noise is also called **Johnson noise** (named after the original researcher in the area) or **white noise** (because in optics, white light contains all frequencies). This type of noise has a fairly flat frequency response such as shown in Fig. 5.134a, that is, a plot of its power versus frequency from the very low to the very high end is fairly uniform. A second type of noise is called **shot noise**, a name derived from the fact that its noise sounds like a shower of lead shot hitting a solid surface or like heavy rain on a window. Its source is pockets of carriers passing through a medium at uneven rates. A third is **pink**, **flicker**, or **1/*f* noise**, which is due to the variation in transit times for carriers crossing various junctions of semiconductor devices. It is called $1/f$ noise because its magnitude drops off with increase in frequency. **Its effect is usually the most dramatic for frequencies below 1 kHz**, as shown in Fig. 5.134b.

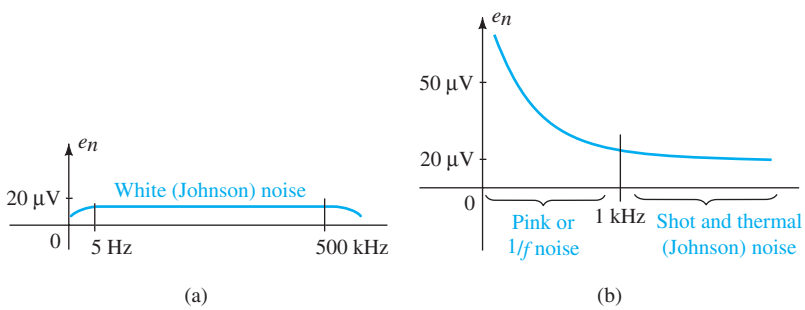



**FIG. 5.134**

*Typical noise frequency spectra: (a) white or Johnson; (b) pink, thermal, and shot.*

The network of Fig. 5.135 is designed to generate both a white noise and a pink noise. Rather than a separate source for each, first white noise is developed (level across the entire frequency spectrum), and then a filter is applied to remove the mid- and high-frequency components, leaving only the low-frequency noise response. The filter is further designed to modify the flat response of the white noise in the low-frequency region (to create a $1/f$ drop-off) by having sections of the filter "drop in" as the frequency increases. The white noise is created by leaving the collector terminal of transistor $Q_1$ open and reverse-biasing the base-to-emitter junction. In essence, the transistor is being used as a diode biased in the Zener avalanche region. Biasing a transistor in this region creates a very unstable situation that is conducive to the generation of random white noise. The combination of the avalanche region with its rapidly changing charge levels, sensitivity of the current level to

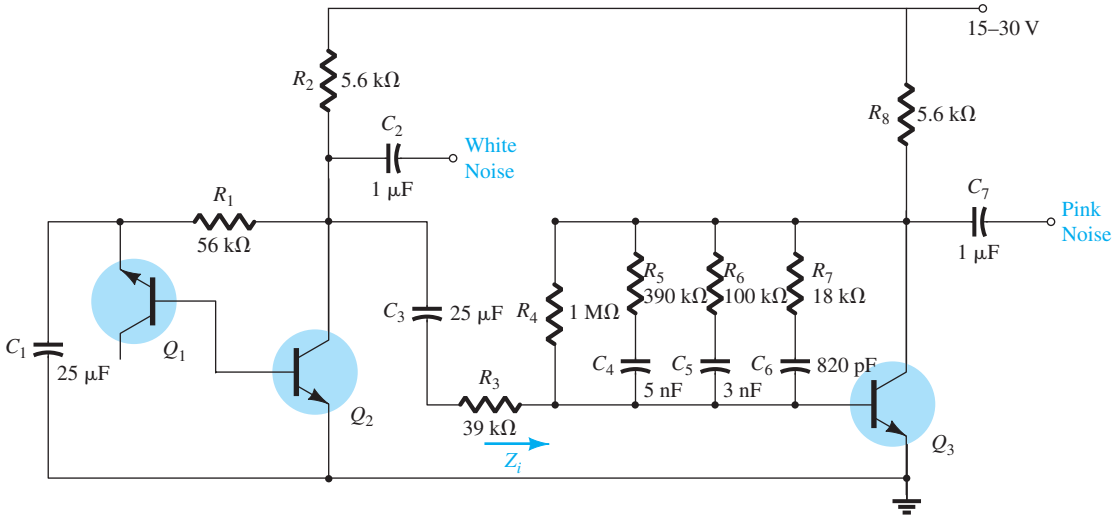



**FIG. 5.135**
*White- and pink-noise generator.*

temperature, and quickly changing impedance levels contributes to the level of noise voltage and current generated by the transistor. Germanium transistors are often used because the avalanche region is less defined and less stable than in silicon transistors. In addition, there are diodes and transistors designed specifically for random-noise generation.

The source of the noise is not some specially designed generator. It is simply due to the fact that current flow is not an ideal phenomenon but actually varies with time at a level that generates unwanted variations in the terminal voltage across elements. In fact, that variation in flow is so broad that it can generate frequencies that extend across a wide spectrum—a very interesting phenomenon.

The generated noise current of $Q_1$ will then be the base current for $Q_2$, which will be amplified to generate a white noise of perhaps 100 mV, which for this design would suggest an input noise voltage of about 170 $\mu$V. Capacitor $C_1$ will have a low impedance throughout the frequency range of interest to provide a "shorting effect" on any spurious signals in the air from contributing to the signal at the base of $Q_1$. The capacitor $C_2$ is there to isolate the dc biasing of the white-noise generator from the dc levels of the filter network to follow. The 39 kΩ and the input impedance of the next stage create the simple voltage-divider network of Fig. 5.136. If the 39 kΩ were not present, the parallel combination of $R_2$ and $Z_i$ would load down the first stage and reduce the gain of $Q_1$ considerably. In the gain equation, $R_2$ and $Z_i$ would appear in parallel (discussed in Chapter 9).

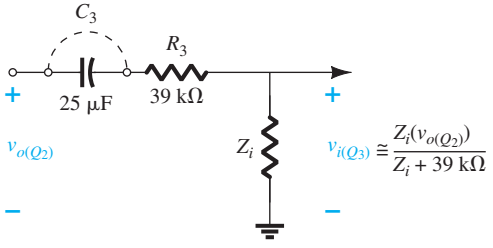



**FIG. 5.136**
*Input circuit for the second stage.*

The filter network is actually part of the feedback loop from collector to base appearing in the collector feedback network of Section 5.10. To describe its behavior, let us first consider the extremes of the frequency spectrum. For very low frequencies all the capacitors can be approximated by an open circuit, and the only resistance from collector to base is the 1-MΩ resistor. Using a beta of 100, we find that the gain of the section is about 280 and the input impedance about 1.28 kΩ. At a sufficiently high frequency all the capacitors

could be replaced by short circuits, and the total resistance combination between collector and base would be reduced to about 14.5 kΩ, which would result in a very high unloaded gain of about 731, more than twice that just obtained with $R_F = 1\ \text{M}\Omega$. Because the $1/f$ filter is supposed to reduce the gain at high frequencies, it initially appears as though there is an error in design. However, the input impedance has dropped to about 19.33 Ω, which is a 66-fold drop from the level obtained with $R_F = 1\ \text{M}\Omega$. This would have a significant impact on the input voltage appearing at the second stage when we consider the voltage-divider action of Fig. 5.136. In fact, when compared to the series 39-kΩ resistor, the signal at the second stage can be assumed to be negligible or at a level where even a gain in excess of 700 cannot raise it to a level of any consequence. In total, therefore, the effect of doubling the gain is totally lost due to the tremendous drop in $Z_i$, and the output at very high frequencies can be ignored entirely.

For the range of frequencies between the very low and the very high, the three capacitors of the filter will cause the gain to drop off with increase in frequency. First, capacitor $C_4$ will be dropped in and cause a reduction in gain (around 100 Hz). Then capacitor $C_5$ will be included and will place the three branches in parallel (around 500 Hz). Finally, capacitor $C_6$ will result in four parallel branches and the minimum feedback resistance (around 6 kHz).

The result is a network with an excellent random-noise signal for the full frequency spectrum (white) and the low-frequency spectrum (pink).

## Sound-Modulated Light Source

The light from the 12-V bulb of Fig. 5.137 will vary at a frequency and an intensity that are sensitive to the applied signal. The applied signal may be the output of an acoustical amplifier, a musical instrument, or even a microphone. Of particular interest is the fact that the applied voltage is 12 V ac rather than the typical dc biasing supply. The immediate question, in the absence of a dc supply, is how the dc biasing levels for the transistor will be established. In actuality, the dc level is obtained through the use of diode $D_1$, which rectifies the ac signal, and capacitor $C_2$, which acts as a power supply filter to generate a dc level across the output branch of the transistor. The peak value of a 12-V rms supply is about 17 V, resulting in a dc level after the capacitive filtering in the neighborhood of 16 V. If the potentiometer is set so that $R_1$ is about 320 Ω, the voltage from base to emitter of the transistor will be about 0.5 V, and the transistor will be in the "off" state. In this state the collector and emitter currents are essentially 0 mA, and the voltage across resistor $R_3$ is approximately 0 V. The voltage at the junction of the collector terminal and the diode is therefore 0 V, resulting in $D_2$ being in the "off" state and 0 V at the gate terminal of the silicon-controlled rectifier (SCR). The SCR (see Section 17.3) is fundamentally a diode whose state is controlled by an applied voltage at the gate terminal. The absence of a voltage at the gate means that the SCR and bulb are off.

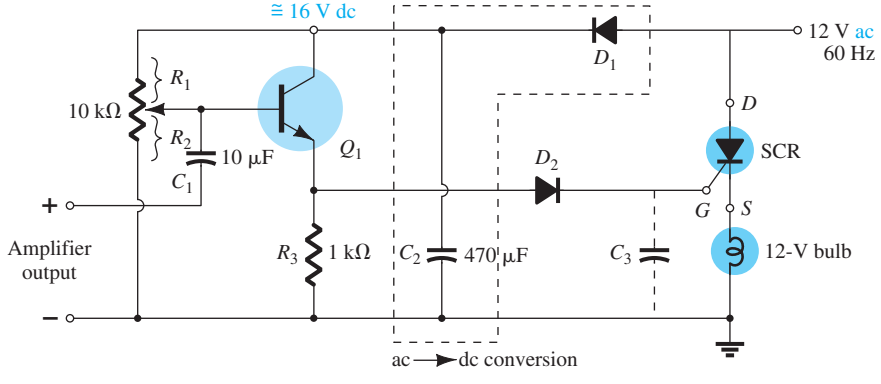



**FIG. 5.137**
*Sound-modulated light source. SCR, Silicon-controlled rectifier.*

If a signal is now applied to the gate terminal, the combination of the established biasing level and the applied signal can establish the required 0.7-V turn-on voltage, and the transistor will be turned on for periods of time dependent on the applied signal. When the

transistor turns on, it will establish a collector current through resistor $R_3$ that will establish a voltage from collector to ground. If the voltage is more than the required 0.7 V for diode $D_2$, a voltage will appear at the gate of the SCR that may be sufficient to turn it on and establish conduction from the drain to the source of the SCR. However, we must now examine one of the most interesting aspects of this design. Because the applied voltage across the SCR is ac, which will vary in magnitude with time as shown in Fig. 5.138, the conduction strength of the SCR will vary with time also. As shown in the figure, if the SCR is turned on when the sinusoidal voltage is a maximum, the resulting current through the SCR will be a maximum also, and the bulb will be its brightest. If the SCR should turn on when the sinusoidal voltage is near its minimum, the bulb may turn on, but the lower current will result in considerably less illumination. The result is that the lightbulb turns on in sync with when the input signal is peaking, but the strength of turn-on will be determined by where one is on the applied 12-V signal. One can imagine the interesting and varied responses of such a system. Each time one applies the same audio signal, the response will have a different character.

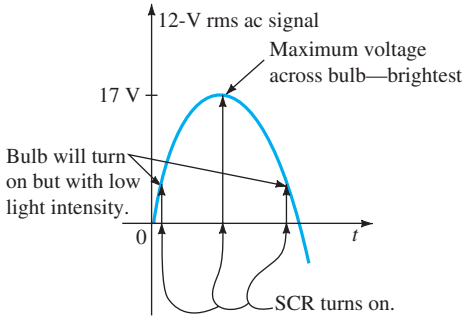



**FIG. 5.138**
*Demonstrating the effect of an ac voltage on the operation of the SCR of Fig. 5.137.*

In the above action, the potentiometer was set below the turn-on voltage of the transistor. The potentiometer can also be adjusted so that the transistor is "just on," resulting in a low-level base current. The result is a low-level collector current and insufficient voltage to forward-bias diode $D_2$ and turn on the SCR at the gate. However, when the system is set up in this manner, the resultant light output will be more sensitive to lower amplitude components of the applied signal. In the first case, the system acts more like a peak detector, whereas in the latter case it is sensitive to more components of the signal.

Diode $D_2$ was included to be sure that there is sufficient voltage to turn on both the diode and the SCR, in other words, to eliminate the possibility of noise or some other low-level unexpected voltage on the line turning the SCR on. Capacitor $C_3$ can be inserted to slow down the response by ensuring the voltage charge across the capacitor before the gate will reach sufficient voltage to turn on the SCR.

## 5.26 SUMMARY

### Important Conclusions and Concepts

1. Amplification in the ac domain cannot be obtained **without the application of dc biasing level**.
2. For most applications the BJT amplifier can be considered linear, permitting the use of the **superposition theorem** to separate the dc and ac analyses and designs.
3. When introducing the **ac model** for a BJT:
   a. All **dc sources are set to zero** and replaced by a short-circuit connection to ground.
   b. All **capacitors** are replaced by a **short-circuit equivalent**.
   c. All elements **in parallel with** an introduced short-circuit equivalent should be removed from the network.
   d. The network should be **redrawn** as often as possible.
4. The **input impedance** of an ac network **cannot be measured** with an ohmmeter.

5. The **output impedance** of an amplifier is measured with the **applied signal set to zero**. It cannot be measured with an ohmmeter.
6. The **output impedance** for the $r_e$ model **can be included** only if obtained from a data sheet or from a graphical measurement from the characteristic curves.
7. Elements that were isolated by capacitors for the dc analysis **will appear in the ac analysis** due to the short-circuit equivalent for the capacitive elements.
8. The **amplification factor** (beta, $\beta$, or $h_{fe}$) is the least sensitive to changes **in collector current**, whereas the **output impedance** parameter is the most sensitive. The output impedance is also quite sensitive to changes in $\boldsymbol{V_{CE}}$, whereas the **amplification** factor is the **least sensitive**. However, the **output impedance** is the **least sensitive** to changes in **temperature**, whereas the amplification factor is somewhat sensitive.
9. The $r_e$ **model** for a BJT in the ac domain is sensitive to the **actual dc operating conditions of the network**. This parameter is normally not provided on a specification sheet, although $h_{ie}$ of the normally provided hybrid parameters is equal to $\beta r_e$, but only under specific operating conditions.
10. Most **specification sheets** for BJTs include a **list of hybrid parameters** to establish an ac model for the transistor. One must be aware, however, that they are provided for a particular set of dc operating conditions.
11. The **CE fixed-bias configuration** can have a **significant voltage gain** characteristic, although its **input impedance can be relatively low**. The approximate **current gain** is given by simply **beta**, and the **output impedance** is normally assumed to be $\boldsymbol{R_C}$.
12. The **voltage-divider bias configuration** has a **higher stability** than the fixed-bias configuration, but it has about the **same voltage gain, current gain, and output impedance**. Due to the biasing resistors, its input impedance may be lower than that of the fixed-bias configuration.
13. The **CE emitter-bias configuration** with an unbypassed emitter resistor has a **larger input resistance** than the bypassed configuration, but it will have a **much smaller voltage gain** than the bypassed configuration. For the unbypassed or bypassed situation, the **output impedance** is normally assumed to be simply $\boldsymbol{R_C}$.
14. The **emitter-follower configuration** will always have an **output voltage slightly less than the input signal**. However, the **input impedance** can be **very large**, making it very useful for situations where a high-input first stage is needed to "pick up" as much of the applied signal as possible. Its **output impedance** is **extremely low**, making it an excellent signal source for the second stage of a multistage amplifier.
15. The **common-base configuration** has a **very low input impedance**, but it can have a **significant voltage gain**. The **current gain** is just **less than 1**, and the **output impedance** is simply $\boldsymbol{R_C}$.
16. The **collector feedback configuration** has an **input impedance** that is **sensitive to beta** and that can be quite low depending on the parameters of the configuration. However, the **voltage gain** can be **significant** and the **current gain** of **some magnitude** if the parameters are chosen properly. The **output impedance** is most often simply the collector resistance $\boldsymbol{R_C}$.
17. The **collector dc feedback configuration** uses the dc feedback to **increase its stability** and the changing state of a capacitor from dc to ac to establish a **higher voltage gain** than obtained with a straight feedback connection. The **output impedance** is usually close to $\boldsymbol{R_C}$ and the **input impedance** relatively close to that obtained with the **basic common-emitter configuration**.
18. The **approximate hybrid equivalent network** is very **similar** in composition to that used with the $\boldsymbol{r_e}$ **model**. In fact, the **same methods** of analysis can be applied to both models. For the hybrid model the results will be in terms of the network parameters and the hybrid parameters, whereas for the $r_e$ model they will be in terms of the network parameters and $\beta$, $r_e$, and $r_o$.
19. The **hybrid model** for common-emitter, common-base, and common-collector configurations **is the same**. The only difference will be the magnitude of the parameters of the equivalent network.
20. The total gain of a cascaded system is determined by the **product of the gains of each stage**. The gain of each stage, however, must be determined **under loaded conditions**.
21. Because the total gain is the product of the individual gains of a cascaded system, the **weakest link** can have a major effect on the total gain.

## Equations

$$r_e = \frac{26\text{ mV}}{I_E}$$

Hybrid parameters:

$$h_{ie} = \beta r_e, \qquad h_{fe} = \beta_{ac}, \qquad h_{ib} = r_e, \qquad h_{fb} = -\alpha \cong -1$$

CE fixed bias:

$$Z_i \cong \beta r_e, \qquad Z_o \cong R_C$$

$$A_v = -\frac{R_C}{r_e}, \qquad A_i = -A_v\frac{Z_i}{R_C} \cong \beta$$

Voltage-divider bias:

$$Z_i = R_1 \| R_2 \| \beta r_e, \qquad Z_o \cong R_C$$

$$A_v = -\frac{R_C}{r_e}, \qquad A_i = -A_v\frac{Z_i}{R_C} \cong \beta$$

CE emitter-bias:

$$Z_i \cong R_B \| \beta R_E, \qquad Z_o \cong R_C$$

$$A_v \cong -\frac{R_C}{R_E}, \qquad A_i \cong \frac{\beta R_B}{R_B + \beta R_E}$$

Emitter-follower:

$$Z_i \cong R_B \| \beta R_E, \qquad Z_o \cong r_e$$

$$A_v \cong 1, \qquad A_i = -A_v\frac{Z_i}{R_E}$$

Common-base:

$$Z_i \cong R_E \| r_e, \qquad Z_o \cong R_C$$

$$A_v \cong \frac{R_C}{r_e}, \qquad A_i \cong -1$$

Collector feedback:

$$Z_i \cong \frac{r_e}{\frac{1}{\beta} + \frac{R_C}{R_F}}, \qquad Z_o \cong R_C \| R_F$$

$$A_v = -\frac{R_C}{r_e}, \qquad A_i \cong \frac{R_F}{R_C}$$

Collector dc feedback:

$$Z_i \cong R_{F_1} \| \beta r_e, \qquad Z_o \cong R_C \| R_{F_2}$$

$$A_v = -\frac{R_{F_2} \| R_C}{r_e}, \qquad A_i = -A_v\frac{Z_i}{R_C}$$

Effect of load impedance:

$$A_{v_L} = \frac{V_o}{V_i} = \frac{R_L}{R_L + R_o}A_{v_{NL}}, \qquad A_{i_L} = \frac{I_o}{I_i} = -A_{v_L}\frac{Z_i}{R_L}$$

Effect of source impedance:

$$V_i = \frac{R_i V_s}{R_i + R_s}, \qquad A_{v_s} = \frac{V_o}{V_s} = \frac{R_i}{R_i + R_s}A_{v_{NL}}$$

$$I_s = \frac{V_s}{R_s + R_i}$$

Combined effect of load and source impedance:

$$A_{v_L} = \frac{V_o}{V_i} = \frac{R_L}{R_L + R_o}A_{v_{NL}}, \qquad A_{v_s} = \frac{V_o}{V_s} = \frac{R_i}{R_i + R_s} \cdot \frac{R_L}{R_L + R_o}A_{v_{NL}}$$

$$A_{i_L} = \frac{I_o}{I_i} = -A_{v_L}\frac{R_i}{R_L}, \qquad A_{i_s} = \frac{I_o}{I_s} = -A_{v_s}\frac{R_s + R_i}{R_L}$$

Cascode connection:

$$A_v = A_{v_1}A_{v_2}$$

Darlington connection (with $R_E$):

$$\beta_D = \beta_1\beta_2,$$

$$Z_i = R_B \| (\beta_1\beta_2 R_E), \qquad A_i = \frac{\beta_1\beta_2 R_B}{(R_B + \beta_1\beta_2 R_E)}$$

$$Z_o = \frac{r_{e_1}}{\beta_2} + r_{e_2} \qquad A_v = \frac{V_o}{V_i} \approx 1$$

Darlington connection (without $R_E$):

$$Z_i = R_1 \| R_2 \| \beta_1(r_{e_1} + \beta_1\beta_2 r_{e_2}) \qquad A_i = \frac{\beta_1\beta_2(R_1 \| R_2)}{R_1 \| R_2 + Z_i'}$$

where $Z_i' = \beta_1(r_{e_1} + \beta_2 r_{e_2})$

$$Z_o \cong R_C \| r_{o_2} \qquad A_v = \frac{V_o}{V_i} = \frac{\beta_1\beta_2 R_C}{Z_i'}$$

Feedback pair:

$$Z_i = R_B \| \beta_1\beta_2 R_C \qquad A_i = \frac{-\beta_1\beta_2 R_B}{R_B + \beta_1\beta_2 R_C}$$

$$Z_o \approx \frac{r_{e_1}}{\beta_2} \qquad A_v \cong 1$$

## 5.27 COMPUTER ANALYSIS

### PSpice Windows

**BJT Voltage-Divider Configuration** The last few chapters have been limited to the dc analysis of electronic networks using PSpice and Multisim. This section will consider the application of an ac source to a BJT network and describe how the results are obtained and interpreted.

Most of the construction of the network of Fig. 5.139 can be accomplished using the procedures introduced in earlier chapters. The ac source can be found in the **SOURCE** library as **VSIN**. You can scroll down the list of options or simply type in **VSIN** at the head of the listing. Once this is selected and placed, a number of labels will appear that define

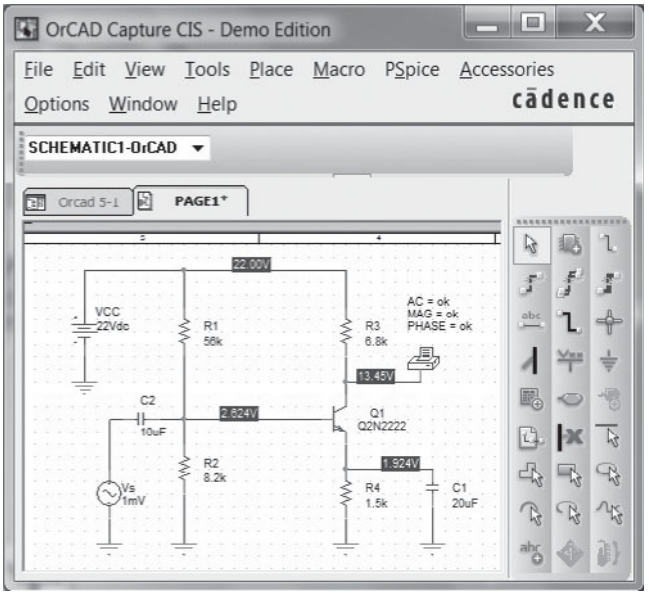



**FIG. 5.139**

*Using PSpice Windows to analyze the network of Fig. 5.28 (Example 5.2).*

the parameters of the source. Double-clicking the source symbol or using the sequence **Edit-Properties** will result in the **Property Editor** dialog box, which lists all the parameters appearing on the screen and more. By scrolling all the way to the left, you will find a listing for **AC**. Select the blank rectangle under the heading and enter the **1 mV** value. Be aware that the entries can use prefixes such as m (milli) and k (kilo). Moving to the right, the heading **FREQ** will appear, in which you can enter **10 kHz**. Moving again to **PHASE**, you will find the default value is **0**, so it can be left alone. It represents the initial phase angle for the sinusoidal signal. Next you will find **VAMPL**, which is set at 1 mV, also followed by **VOFF** at **0** V. Now that each of the properties has been set, we have to decide what to display on the screen to define the source. In Fig. 5.139 the only labels are Vs and 1 mV, so a number of items have to be deleted and the name of the source has to be modified. For each quantity simply return to the heading and select it for modification. If you choose **AC**, select **Display** to obtain the **Display Properties** dialog box. Select **Value Only** because we prefer not to have the label **AC** appear. Leave all the other choices blank. An **OK**, and you can move to the other parameters within the **Property Editor** dialog box. We do not want the **FREQ**, **PHASE**, **VAMPL** and **VOFF** labels to appear with their values, so in each case select **Do Not Display**. To change **V1** to **Vs**, simply go to the **Part Reference**, and after selecting it, type in **Vs**. Then go to **Display** and select **Value Only**. Finally, to apply all the changes, select **Apply** and exit the dialog box; the source will appear as shown in Fig. 5.139.

The ac response for the voltage at a point in the network is obtained using the **VPRINT1** option found in the **SPECIAL** library. If the library does not appear, simply select **Add Library** followed by **special.olb**. When **VPRINT1** is chosen, it will appear on the screen as a printer with three labels: **AC**, **MAG**, and **PHASE**. Each has to be set to an OK status to reflect the fact that you desire this type of information about the voltage level. This is accomplished by simply clicking on the printer symbol to obtain the dialog box and setting each to **OK**. For each entry select **Display** and choose **Name and Label**. Finally, select **Apply** and exit the dialog box. The result appears in Fig. 5.139.

The transistor **Q2N2222** can be found under the **EVAL** library by typing it under the **Part** heading or simply scrolling through the possibilities. The levels of $I_s$ and $\beta$ can be set by first selecting the Q2N2222 transistor to make it red and then applying the sequence **Edit-PSpice Model** to obtain the **PSpice Model Editor Lite** dialog box and changing **Is** to **2E-15A** and **Bf** to 90. The level of **Is** is the result of numerous runs of the network to find the value that would result in $V_{BE}$ being closest to 0.7 V.

Now that all the components of the network have been set, it is time to ask the computer to analyze the network and provide some results. If improper entries were made, the computer will quickly respond with an error listing. First select the **New Simulation Profile** key to obtain the **New Simulation** dialog box. Then, after entering **Name** as **OrCAD 5-1**, select **Create** and the **Simulation Settings** dialog box will appear. Under **Analysis type**, select **AC Sweep/Noise** and then under **AC Sweep Type** choose **Linear**. The **Start Frequency** is **10 kHz**, the **End Frequency** is **10 kHz**, and the **Total Points** is **1**. An **OK**, and the simulation can be initiated by selecting the **Run PSpice** key (white arrow). A schematic will result with a graph that extends from 5 kHz to 15 kHz with no vertical scale. Through the sequence **View-Output File** the listing of Fig. 5.140 can be obtained. It starts with a list of all the elements of the network and their settings followed by all the parameters of the transistor. In particular, note the level of **IS** and **BF**. Next the dc levels are provided under the **SMALL SIGNAL BIAS SOLUTION**, which match those appearing on the schematic of Fig. 5.139. The dc levels appear on Fig. 5.139 due to the selection of the **V** option. Also note that $V_{BE} = 2.624\text{ V} - 1.924\text{ V} = 0.7\text{ V}$, as stated above, due to the choice of **Is**.

The next listing, **OPERATING POINT INFORMATION**, reveals that even though beta of the **BJT MODEL PARAMETERS** listing was set at 90, the operating conditions of the network resulted in a dc beta of 48.3 and an ac beta of 55. Fortunately, however, the voltage-divider configuration is less sensitive to changes in beta in the dc mode, and the dc results are excellent. However, the drop in ac beta had an effect on the resulting level of $V_o$: 296.1 mV versus the handwritten solution (with $r_o = 50\,\text{k}\Omega$) of 324.3 mV—a 9% difference. The results are certainly close, but probably not as close as one would like. A closer result (within 7%) could be obtained by setting all the parameters of the device except $I_s$ and beta to zero. However, for the moment, the impact of the remaining parameters has been demonstrated, and the results will be accepted as sufficiently close to the handwritten levels. Later in this chapter, an ac model for the transistor will be introduced with results

```
****          CIRCUIT DESCRIPTION

******************************************************************************************************************

*Analysis directives:
.AC LIN 1 10kHz 10kHz
.OP
.PROBE V(alias(*)) I(alias(*)) W(alias(*)) D(alias(*)) NOISE(alias(*))
.INC "..\SCHEMATIC1.net"
* source ORCAD 5-1
Q_Q1        N00286 N00282 N00319 Q2N2222
R_R1        N00282 N00254  56k TC=0,0
R_R2        0 N00282  8.2k TC=0,0
R_R3        N00286 N00254  6.8k TC=0,0
R_R4        0 N00319  1.5k TC=0,0
V_VCC       N00254 0 22Vdc
C_C1        0 N00319  20uF  TC=0,0
V_Vs        N00342 0  AC  1mV
+SIN 0V 1mV 10kHz 0 0 0
. PRINT       AC
+  VM ([N00286])
+  VP ([N00286])
C_C2        N00342 N00282  10uF  TC=0,0
.END

****    BJT MODEL PARAMETERS

******************************************************************************************************************

                    Q2N2222
                    NPN
          LEVEL     1
                IS    2.000000E-15
                BF    90
                NF    1
               VAF    74.03
               IKF    .2847
               ISE    14.340000E-15
                NE    1.307
                BR    6.092
                NR    1
               ISS    0
                RB    10
                RE    0
                RC    1
               CJE    22.010000E-12
               VJE    .75
               MJE    .377
               CJC    7.306000E-12
               VJC    .75
               MJC    .3416

             XCJC    1
               CJS    0
               VJS    .75
                TF 411.100000E-12
               XTF    3
               VTF    1.7
               ITF    .6
                TR    46.910000E-09
               XTB    1.5
                KF    0
                AF    1
                CN    2.42
                 D    .87

****    SMALL SIGNAL BIAS SOLUTION                      TEMPERATURE =  27.000  DEG  C

******************************************************************************************************************

NODE         VOLTAGE     NODE         VOLTAGE     NODE         VOLTAGE     NODE         VOLTAGE
(N00254)     22.0000     (N00282)     2.6239      (N00286)     13.4530     (N00319)     1.9244
(N00342)      0.0000

   VOLTAGE SOURCE CURRENTS
   NAME         CURRENT
   V_VCC       -1.603E-03
   V_Vs         0.000E+00

   TOTAL POWER DISSIPATION   3.53E-02  WATTS

****    OPERATING POINT INFORMATION                     TEMPERATURE =  27.000  DEG  C

******************************************************************************************************************

**** BIPOLAR JUNCTION TRANSISTORS

NAME                Q_Q1
MODEL               Q2N2222
IB                  2.60E-05
IC                  1.26E-03
VBE                 6.99E-01
VBC                -1.08E+01
VCE                 1.15E+01
BETADC              4.83E+01
GM                  4.84E-02
RPI                 1.14E+03
RX                  1.00E+01
RO                  6.75E+04
CBE                 5.78E-11
CBC                 2.87E-12
CJS                 0.00E+00
BETAAC              5.50E+01
CBX/CBX2            0.00E+00
FT/FT2              1.27E+08

****    AC ANALYSIS                                     TEMPERATURE =  27.000  DEG  C

******************************************************************************************************************

  FREQ       VM(N00286)    VP(N00286)
1.000E+04     2.961E-01    -1.780E+02
```

**FIG. 5.140**

*Output file for the network of Fig. 5.139.*

that will be an exact match with the handwritten solution. The phase angle is $-178°$ versus the ideal of $-180°$, a very close match.

A plot of the voltage at the collector of the transistor can be obtained by setting up a new simulation process to calculate the value of the desired voltage at a number of data points. The more points, the more accurate is the plot. The process is initiated by returning to the

**Simulation Settings** dialog box and under **Analysis type** selecting **Time Domain(Transient)**. Time domain is chosen because the horizontal axis will be a time axis, requiring that the collector voltage be determined at a specified time interval to permit the plot. Because the period of the waveform is $1/10\,\text{kHz} = 0.1\,\text{ms} = 100\,\mu\text{s}$, and it would be convenient to display five cycles of the waveform, the **Run to time(TSTOP)** is set at 500 $\mu$s. The **Start saving data after** point is left at 0 s and under **Transient option**, the **Maximum step size** is set at 1 $\mu$s to ensure 100 data points for each cycle of the waveform. An **OK**, and a **SCHEMATIC** window will appear with a horizontal axis broken down in units of time but with no vertical axis defined. The desired waveform can then be added by first selecting **Trace** followed by **Add Trace** to obtain the **Add Trace** dialog box. In the provided listing **V(Q1:c)** is selected as the voltage at the collector of the transistor. The instant it is selected it will appear as the **Trace Expression** at the bottom of the dialog box. Referring to Fig. 5.139, we find that because the capacitor $C_E$ will essentially be in the short-circuit state at 10 kHz, the voltage from collector to ground is the same as that across the output terminals of the transistor. An **OK**, and the simulation can be initiated by selecting the **Run PSpice** key.

The result will be the waveform of Fig. 5.141 having an average value of about 13.45 V, which corresponds exactly with the bias level of the collector voltage in Fig. 5.139. The range of the vertical axis was chosen automatically by the computer. Five full cycles of the output voltage are displayed with 100 data points for each cycle. The data points appear in Fig. 5.139 because the sequence **Tools-Options-Mark Data Points** was applied. The data points appear as small dark circles on the plot curve. Using the scale of the graph, we see that the peak-to-peak value of the curve is approximately $13.76\,\text{V} - 13.16\,\text{V} = 0.6\,\text{V} = 600\,\text{mV}$, resulting in a peak value of 300 mV. Because a 1-mV signal was applied, the gain is 300, or very close to the calculator solution of 296.1.

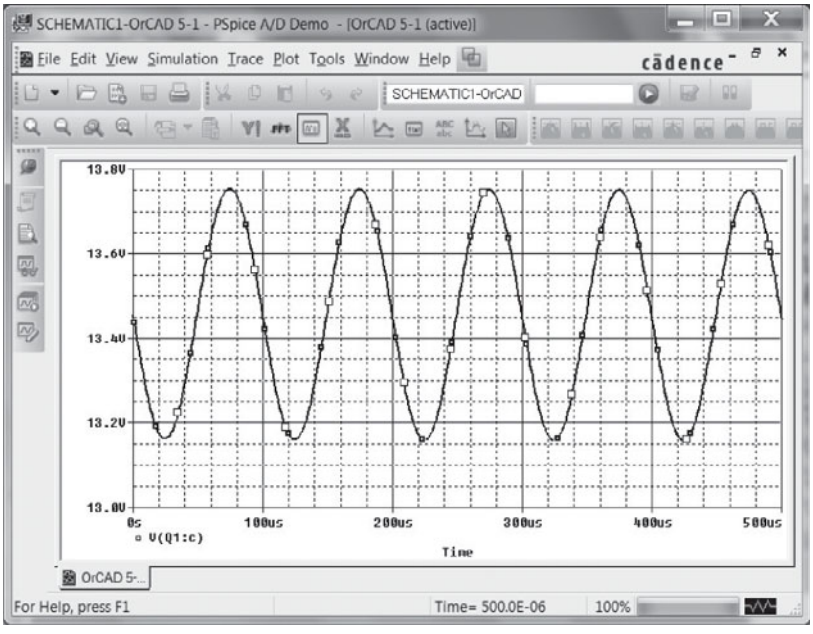



**FIG. 5.141**

*Voltage $v_C$ for the network Fig. 5.139.*

If a comparison is to be made between the input and output voltages on the same screen, the **Add Y-Axis** option under **Plot** can be used. After you select it, choose the **Add Trace** icon and select **V(Vs:+)** from the provided list. The result is that both waveforms will appear on the same screen as shown in Fig. 5.142, each with its own vertical scale.

If two separate graphs are preferred, we can start by selecting **Plot** followed by **Add Plot to Window** after the graph of Fig. 5.141 is in place. The result will be a second set of axes waiting for a decision about which curve to plot. Using **Trace-Add Trace-V(Vs:+)** will result in the graphs of Fig. 5.143. The **SEL >>** (from **SELECT**) appearing next to one of the plots defines the "active" plot.

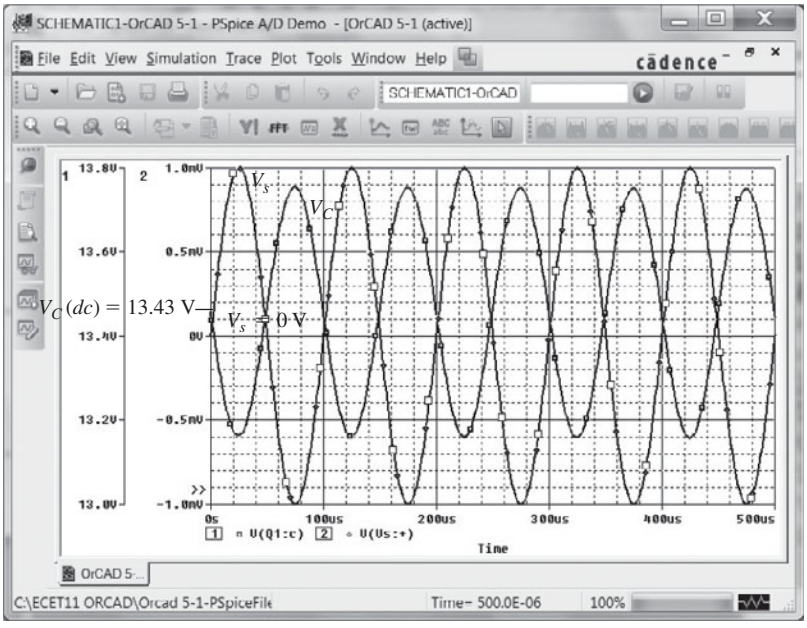



**FIG. 5.142**

*The voltages $v_C$ and $v_s$ for the network of Fig. 5.139.*

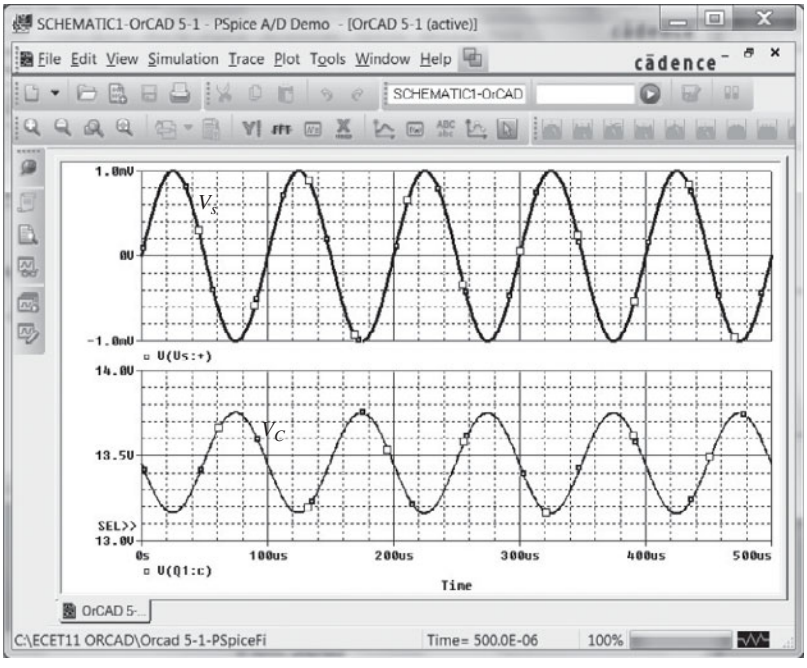



**FIG. 5.143**

*Two separate plots of $v_C$ and $v_s$ in Fig. 5.139.*

The last operation to be introduced in this coverage of graph displays is the use of the cursor option. The result of the sequence **Trace-Cursor-Display** is a line at the dc level of the graph of Fig. 5.144 intersecting with a vertical line. The level and time both appear in the small dialog box in the bottom right corner of the screen. The first number for **Cursor 1** is the time intersection and the second is the voltage level at that instant. A left-click of the mouse will provide control of the intersecting vertical and horizontal lines at this level. Clicking on the vertical line and holding down on the clicker will allow you to move the intersection horizontally along the curve, simultaneously displaying the time and

voltage level in the data box at the bottom right of the screen. If it is moved to the first peak of the waveform, the time appears as 75.194 $\mu$s with a voltage level of 13.753 V, as shown in Fig. 5.144. On right-clicking of the mouse, a second intersection, defined by **Cursor 2**, will appear, which can be moved in the same way with its time and voltage appearing in the same dialog box. Note that if **Cursor 2** is placed close to the negative peak, the difference in time is 49.61 $\mu$s (as displayed in the same box), which is very close to one-half the period of the waveform. The difference in magnitude is 591 mV, which is very close to the 600 mV obtained earlier.

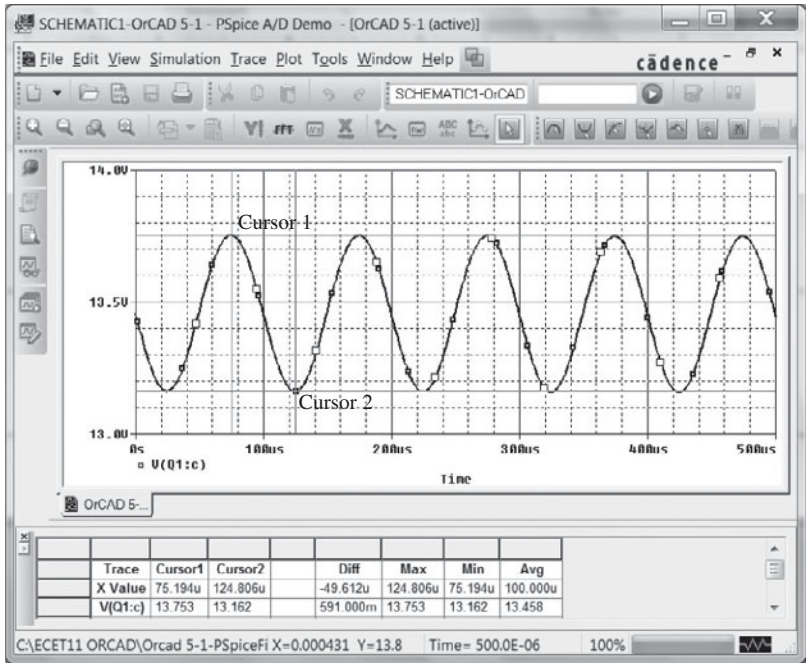



**FIG. 5.144**

*Demonstrating the use of cursors to read specific points on a plot.*

**Voltage-Divider Configuration—Controlled Source Substitution** The results obtained for any analysis using the transistors provided in the PSpice listing will always be somewhat different from those obtained with an equivalent model that only includes the effect of beta and $r_e$. This was clearly demonstrated for the network of Fig. 5.139. If a solution is desired that is limited to the approximate model used in the hand calculations, then the transistor must be represented by a model such as appearing in Fig. 5.145.

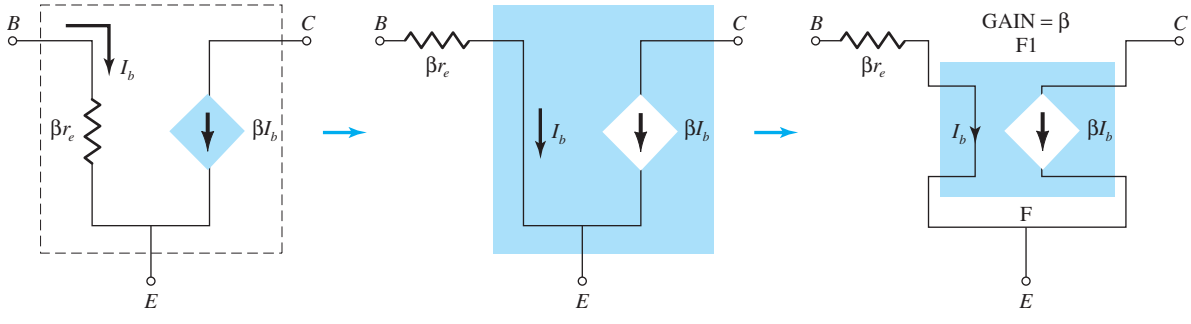



**FIG. 5.145**

*Using a controlled source to represent the transistor of Fig. 5.139.*

For Example 5.2, $\beta$ is 90, with $\beta r_e = 1.66\,\text{k}\Omega$. The current-controlled current source (CCCS) is found in the **ANALOG** library as part **F**. After selection, an **OK**, and the graphical symbol for the CCCS will appear on the screen as shown in Fig. 5.146. Because it does not appear within the basic structure of the CCCS, it must be added in series with the controlling current that appears as an arrow in the symbol. Note the added 1.66-k$\Omega$ resistor, labeled **beta-re** in Fig. 5.146. Double-clicking on the CCCS symbol will result in the **Property Editor** dialog box, in which the **GAIN** can be set to 90. It is the only change to be made in the listing. Then select **Display** followed by **Name and Value** and exit **(x)** the dialog box. The result is the **GAIN = 90** label appearing in Fig. 5.146.

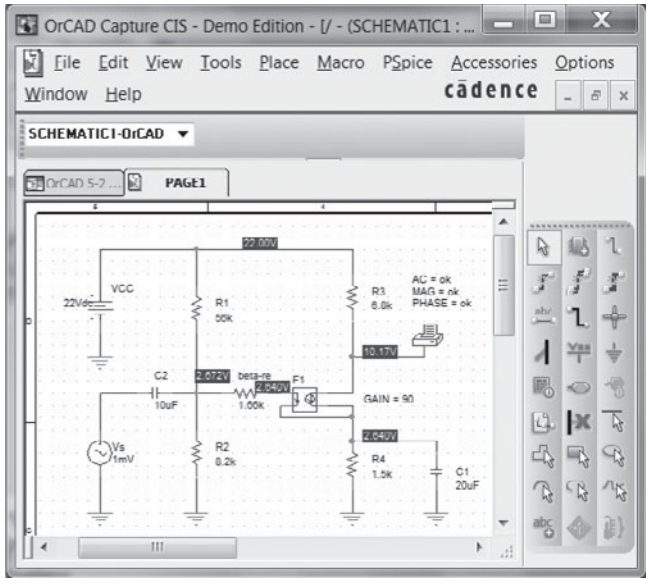
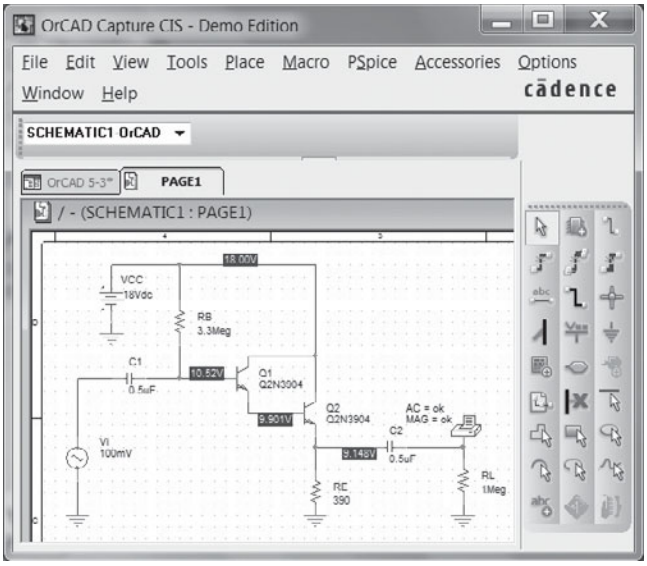



**FIG. 5.146**
*Substituting the controlled source of Fig. 5.145 for the transistor of Fig. 5.139.*

A simulation and the dc levels of Fig. 5.146 will appear. The dc levels do not match the earlier results because the network is a mix of dc and ac parameters. The equivalent model substituted in Fig. 5.146 is a representation of the transistor under ac conditions, not dc biasing conditions. When the software package analyzes the network from an ac viewpoint it will work with an ac equivalent of Fig. 5.146, which will not include the dc parameters. The **Output File** will reveal that the output collector voltage is 368.3 mV, or a gain of 368.3, essentially an exact match with the handwritten solution of 368.76. The effects of $r_o$ could be included by simply placing a resistor in parallel with the controlled source.

**Darlington Configuration** Although PSpice does have two Darlington pairs in the library, individual transistors are employed in Fig. 5.147 to test the solution to Example 5.17. The details of setting up the network have been covered in the preceding sections and chapters. For each transistor $I_s$ is set to 100E-18 and $\beta$ to 89.4. The applied frequency is 10 kHz. A simulation of the network results in the dc levels appearing in Fig. 5.147a and the **Output File** in Fig. 5.147b. In particular, note that the voltage drop between base and emitter for both transistors is $10.52\,\text{V} - 9.148\,\text{V} = 1.37\,\text{V}$ compared to the 1.6 V assumed in the example. Recall that the drop across Darlington pairs is typically about 1.6 V and not simply twice that of a single transistor, or $2(0.7\,\text{V}) = 1.4\,\text{V}$. The output voltage of 99.36 mV is very close to the 99.80 mV obtained in Section 5.17.




(a)

```
****     BJT MODEL PARAMETERS

**********************************************************************************************

                 Q2N3904
                 NPN
           LEVEL     1
              IS     100.000000E-18
              BF     89.4
              NF     1
              BR     1
              NR     1
              CN     2.42
               D     .87

****     SMALL SIGNAL BIAS SOLUTION          TEMPERATURE =    27.000 DEG C

**********************************************************************************************

NODE    VOLTAGE     NODE    VOLTAGE     NODE    VOLTAGE     NODE    VOLTAGE
N00218) 0.0000      (N00225) 18.0000    (N00243) 8.9155     (N00250) 9.6513
(N00291) 0.0000     (N02131) 8.0632

****  AC ANALYSIS           TEMPERATURE =  27.000 DEG C

**********************************************************************************************

  FREQ            VM(N00291)

 1.000E+04        9.936E-02
```

(b)

**FIG. 5.147**

*(a) Design Center schematic of Darlington network; (b) output listing for circuit of part (a) (edited).*

## Multisim

**Collector Feedback Configuration** Because the collector feedback configuration generated the most complex equations for the various parameters of a BJT network, it seems appropriate that Multisim be used to verify the conclusions of Example 5.9. The network appears as shown in Fig. 5.148 using the "virtual" transistor from the **Transistor family** toolbar. Recall from the previous chapter that transistors are obtained by first selecting the **Transistor** keypad appearing as the fourth option over on the **component**

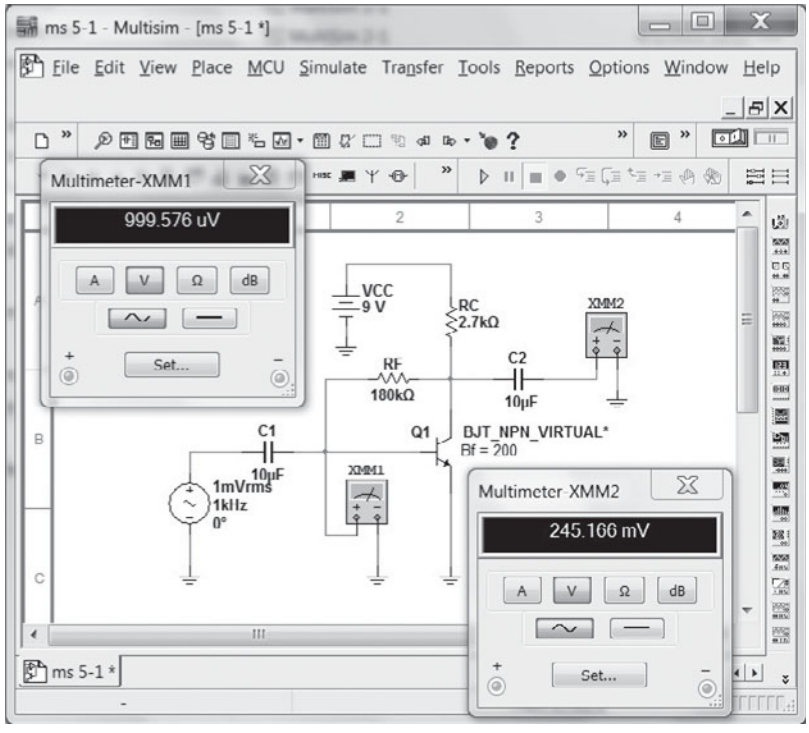



**FIG. 5.148**

*Network of Example 5.9 redrawn using Multisim.*

toolbar. Once chosen, the **Select a Component** dialog box will appear; under the **Family** heading, select **TRANSISTORS_VIRTUAL** followed by **BJT_NPN_VIRTUAL**. Following an **OK** the symbols and labels will appear as shown in Fig. 5.148. We must now check that the beta value is 200 to match the example under investigation. This can be accomplished using one of two paths. In Chapter 4 we used the **EDIT-PROPERTIES** sequence, but here we will simply double-click on the symbol to obtain the **TRANSISTORS_VIRTUAL** dialog box. Under **Value**, select **Edit Model** to obtain the **Edit Model** dialog box (the dialog box has a different appearance from that obtained with the other route and requires a different sequence to change its parameters). The value of **BF** appears as **100**, which must be changed to 200. First select the **BF** line to make it blue all the way across. Then place the cursor directly over the 100 value and select it to isolate it as the quantity to be changed. After deleting the 100, type in the desired 200 value. Then click the **BF** line directly under the **Name** heading and the entire line will be blue again, but now with the 200 value. Then choose **Change Part Model** at the bottom left of the dialog box and the **TRANSISTORS-VIRTUAL** dialog box will appear again. Select **OK** and $\beta = 200$ will be set for the virtual transistor. Note the asterisk next to the BJT label to indicate the parameters of the device have been changed from the default values. The label **Bf = 100** was set using **Place-Text** as described in the previous chapter.

This will be the first opportunity to set up an ac source. First, it is important to realize that there are two types of ac sources available, one whose value is in rms units, the other with its peak value displayed. The option under **Power Sources** uses **rms** values, whereas the ac source under **Signal Sources** uses **peak** values. Because meters display rms values, the **Power Sources** option will be used here. Once **Source** is selected, the **Select a Component** dialog box will appear. Under the **Family** listing select **POWER_SOURCES** and then select **AC_POWER** under the **Component** listing. An **OK**, and the source will appear on the screen with four pieces of information. The label **V1** can be deleted by first double-clicking on the source symbol to obtain the **AC_POWER** dialog box. Select **Display** and disengage **Use Schematic Global Settings**. To remove the label **V1**, disengage the **Show RefDes** option. An **OK**, and the **V1** will disappear from the screen. Next the value has to be set at 1 mV, a process initiated by selecting **Value** in the **AC_POWER** dialog box and then changing the **Voltage (RMS)** to 1 mV. The units of mV can be set using the scroll keys to the right of the magnitude of the source. After you change the **Voltage** to **1 mV**, an **OK** will place this new value on the screen. The frequency of **1000 Hz** can be set in the same way. The **0**-degree phase shift happens to be the default value.

The label **Bf = 200** is set in the same way as described in Chapter 4. The two multimeters are obtained using the first option at the top of the right vertical toolbar. The meter faces appearing in Fig. 5.148 were obtained by simply double-clicking on the multimeter symbols on the schematic. Both were set to read voltages, the magnitudes of which will be in rms units.

After simulation the results of Fig. 5.148 appear. Note that the meter **XMM1** is not reading the 1 mV expected. This is due to the small drop in voltage across the input capacitor at 1 kHz. Certainly, however, it is very close to 1 mV. The output of 245.166 mV quickly reveals that the gain of the transistor configuration is about 245.2, which is a very close match with the 240 obtained in Example 5.9.

**Darlington Configuration** Applying Multisim to the network of Fig. 5.147 with a packaged Darlington amplifier results in the printout of Fig. 5.149. For each transistor the parameters were changed to **Is = 100E-18 A** and **Bf = 89.4** using the technique described earlier. For practice purposes the ac signal source was employed rather than the power source. The peak value of the applied signal is set at 100 mV, but note that the multimeter reads the effective or rms value of 99.991 mV. The indicators reveal that the base voltage of $Q_1$ is 7.736 V, and the emitter voltage of $Q_2$ is 6.193 V. The rms value of the output voltage is 99.163 mV, resulting in a gain of 0.99 as expected for the emitter follower configuration. The collector current is 16 mA with a base current of 1.952 mA, resulting in a $\beta_D$ of about 8200.

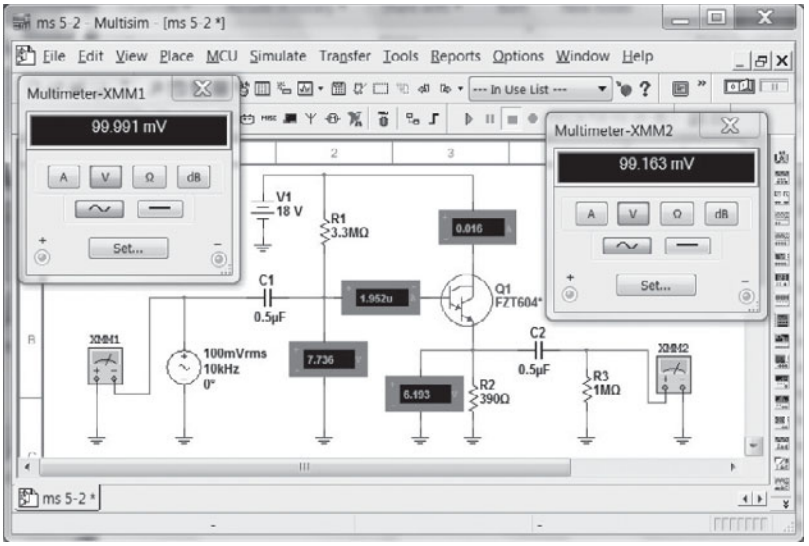



**FIG. 5.149**
*Network of Example 5.9 redrawn using Multisim.*

## PROBLEMS

**Note:* Asterisks indicate more difficult problems.

### 5.2 Amplification in the AC Domain

1. **a.** What is the expected amplification of a BJT transistor amplifier if the dc supply is set to zero volts?
   **b.** What will happen to the output ac signal if the dc level is insufficient? Sketch the effect on the waveform.
   **c.** What is the conversion efficiency of an amplifier in which the effective value of the current through a 2.2-kΩ load is 5 mA and the drain on the 18-V dc supply is 3.8 mA?
2. Can you think of an analogy that would explain the importance of the dc level on the resulting ac gain?
3. If a transistor amplifier has more than one dc source, can the superposition theorem be applied to obtain the response of each dc source and algebraically add the results?

### 5.3 BJT Transistor Modeling

4. What is the reactance of a 10-$\mu$F capacitor at a frequency of 1 kHz? For networks in which the resistor levels are typically in the kilohm range, is it a good assumption to use the short-circuit equivalence for the conditions just described? How about at 100 kHz?
5. Given the common-base configuration of Fig. 5.150, sketch the ac equivalent using the notation for the transistor model appearing in Fig. 5.7.

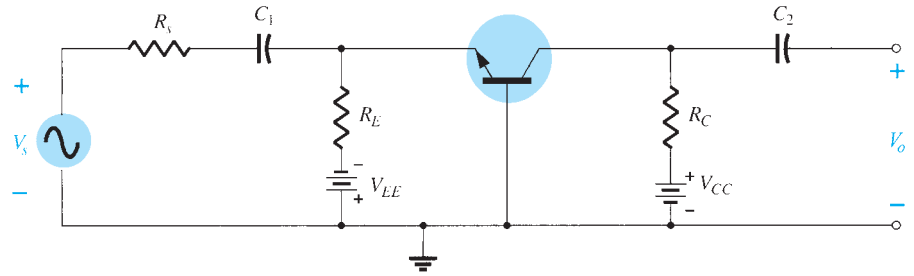



**FIG. 5.150**
*Problem 5.*

### 5.4 The $r_e$ Transistor Model

6. **a.** Given an Early voltage of $V_A = 100$ V, determine $r_o$ if $V_{CE_Q} = 8$ V and $I_{C_Q} = 4$ mA.
   **b.** Using the results of part (a), find the change in $I_C$ for a change in $V_{CE}$ of 6 V at the same $Q$-point as part (a).

7. For the common-base configuration of Fig. 5.18, an ac signal of 10 mV is applied, resulting in an ac emitter current of 0.5 mA. If $\alpha = 0.980$, determine:
   **a.** $Z_i$.
   **b.** $V_o$ if $R_L = 1.2\,\text{k}\Omega$.
   **c.** $A_v = V_o/V_i$.
   **d.** $Z_o$ with $r_o = \infty\,\Omega$.
   **e.** $A_i = I_o/I_i$.
   **f.** $I_b$.
8. Using the model of Fig. 5.16, determine the following for a common-emitter amplifier if $\beta = 80$, $I_E(\text{dc}) = 2\,\text{mA}$, and $r_o = 40\,\text{k}\Omega$.
   **a.** $Z_i$.
   **b.** $I_b$.
   **c.** $A_i = I_o/I_i = I_L/I_b$ if $R_L = 1.2\,\text{k}\Omega$.
   **d.** $A_v$ if $R_L = 1.2\,\text{k}\Omega$.
9. The input impedance to a common-emitter transistor amplifier is 1.2 kΩ with $\beta = 140$, $r_o = 50\,\text{k}\Omega$, and $R_L = 2.7\,\text{k}\Omega$. Determine:
   **a.** $r_e$.
   **b.** $I_b$ if $V_i = 30\,\text{mV}$.
   **c.** $I_c$.
   **d.** $A_i = I_o/I_i = I_L/I_b$.
   **e.** $A_v = V_o/V_i$.
10. For the common-base configuration of Fig. 5.18, the dc emitter current is 3.2 mA and $\alpha$ is 0.99. Determine the following if the applied voltage is 48 mV and the load is 2.2 kΩ.
    **a.** $r_e$.
    **b.** $Z_i$.
    **c.** $I_c$.
    **d.** $V_o$.
    **e.** $A_v$.
    **f.** $I_b$.

## 5.5 Common-Emitter Fixed-Bias Configuration

11. For the network of Fig. 5.151:
    **a.** Determine $Z_i$ and $Z_o$.
    **b.** Find $A_v$.
    **c.** Repeat parts (a) and (b) with $r_o = 20\,\text{k}\Omega$.
12. For the network of Fig. 5.152, determine $V_{CC}$ for a voltage gain of $A_v = -160$.

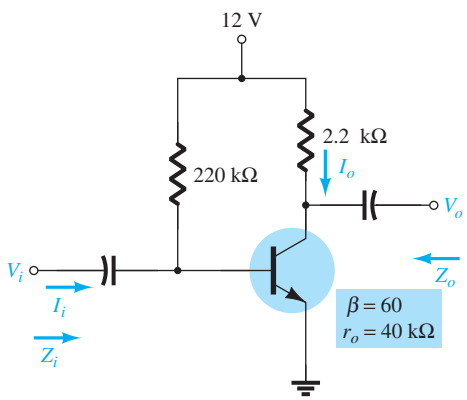



**FIG. 5.151**
*Problem 11.*

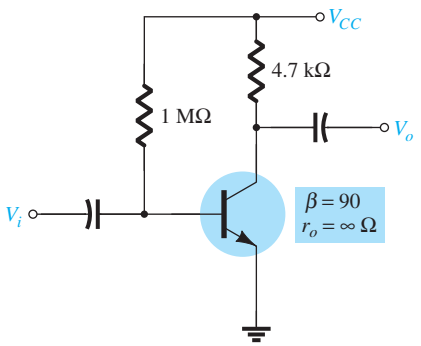



**FIG. 5.152**
*Problem 12.*

*13. For the network of Fig. 5.153:
    **a.** Calculate $I_B$, $I_C$, and $r_e$.
    **b.** Determine $Z_i$ and $Z_o$.
    **c.** Calculate $A_v$.
    **d.** Determine the effect of $r_o = 30\,\text{k}\Omega$ on $A_v$.
14. For the network of Fig. 5.153, what value of $R_C$ will cut the voltage gain to half the value obtained in problem 13?

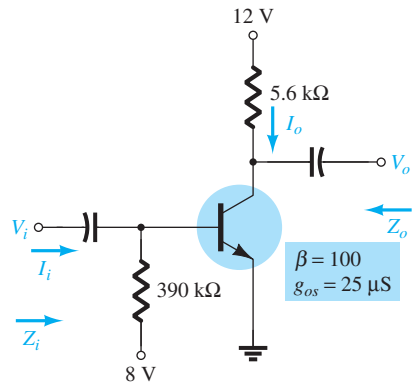



**FIG. 5.153**
*Problem 13.*

## 5.6 Voltage-Divider Bias

**15.** For the network of Fig. 5.154:
- **a.** Determine $r_e$.
- **b.** Calculate $Z_i$ and $Z_o$.
- **c.** Find $A_v$.
- **d.** Repeat parts (b) and (c) with $r_o = 25\ \text{k}\Omega$.

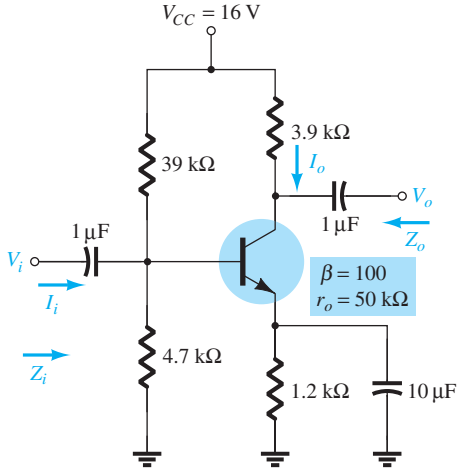



**FIG. 5.154**
*Problem 15.*

**16.** Determine $V_{CC}$ for the network of Fig. 5.155 if $A_v = -160$ and $r_o = 100\ \text{k}\Omega$.

**17.** For the network of Fig. 5.156:
- **a.** Determine $r_e$.
- **b.** Calculate $V_B$ and $V_C$.
- **c.** Determine $Z_i$ and $A_v = V_o/V_i$.

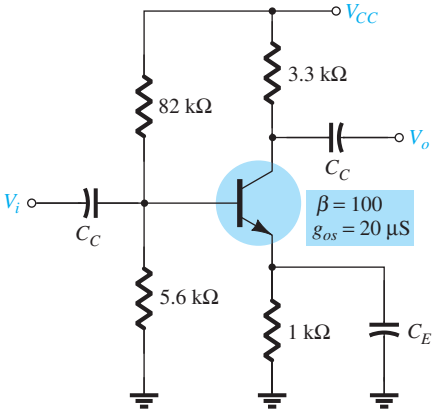



**FIG. 5.155**
*Problem 16.*

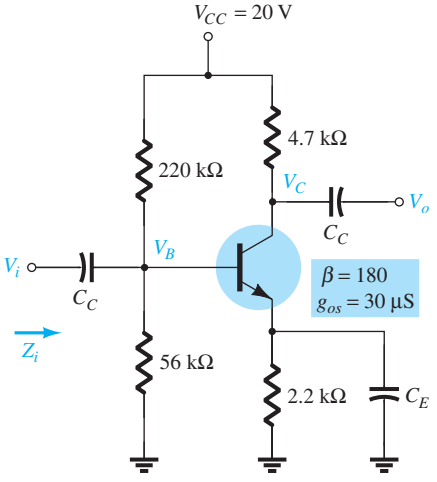



**FIG. 5.156**
*Problem 17.*

**18.** For the network of Fig. 5.157:
- **a.** Determine $r_e$.
- **b.** Find the dc voltages $V_B$, $V_{CB}$, and $V_{CE}$.
- **c.** Determine $Z_i$ and $Z_o$.
- **d.** Calculate $A_v = V_o/V_i$.

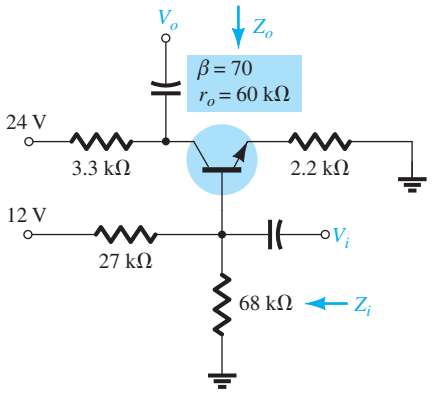



**FIG. 5.157**
*Problem 18.*

## 5.7 CE Emitter-Bias Configuration

**19.** For the network of Fig. 5.158:
- **a.** Determine $r_e$.
- **b.** Find $Z_i$ and $Z_o$.
- **c.** Calculate $A_v$.
- **d.** Repeat parts (b) and (c) with $r_o = 20\ \text{k}\Omega$.

**20.** Repeat Problem 19 with $R_E$ bypassed. Compare results.

**21.** For the network of Fig. 5.159, determine $R_E$ and $R_B$ if $A_v = -10$ and $r_e = 3.8\ \Omega$. Assume that $Z_b = \beta R_E$.

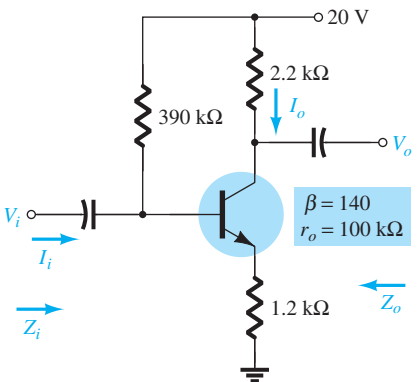



**FIG. 5.158**
*Problems 19 and 20.*

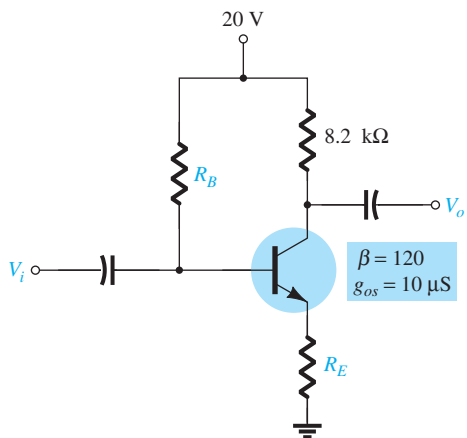



**FIG. 5.159**
*Problem 21.*

***22.** For the network of Fig. 5.160:
- **a.** Determine $r_e$.
- **b.** Find $Z_i$ and $A_v$.

**23.** For the network of Fig. 5.161:
- **a.** Determine $r_e$.
- **b.** Calculate $V_B$, $V_{CE}$, and $V_{CB}$.
- **c.** Determine $Z_i$ and $Z_o$.
- **d.** Calculate $A_v = V_o/V_i$.
- **e.** Determine $A_i = I_o/I_i$.

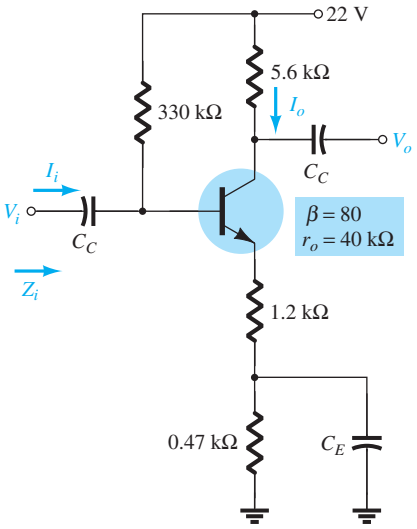



**FIG. 5.160**
*Problem 22.*

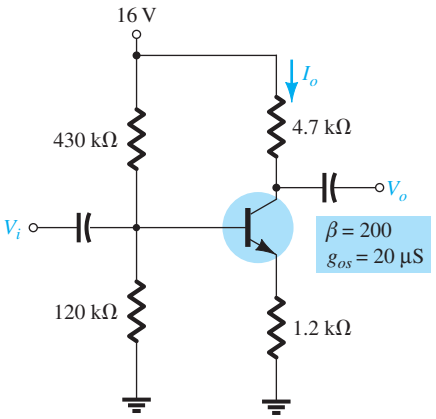



**FIG. 5.161**
*Problem 23.*

## 5.8 Emitter-Follower Configuration

**24.** For the network of Fig. 5.162:
- **a.** Determine $r_e$ and $\beta r_e$.
- **b.** Find $Z_i$ and $Z_o$.
- **c.** Calculate $A_v$.

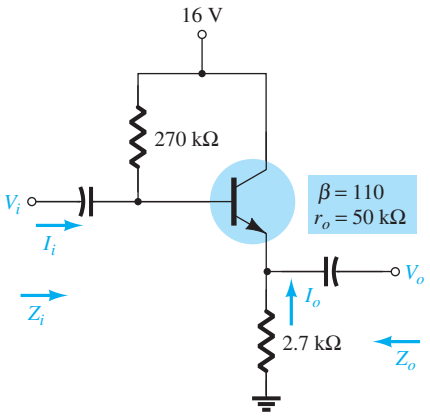



**FIG. 5.162**
*Problem 24.*

***25.** For the network of Fig. 5.163:
- **a.** Determine $Z_i$ and $Z_o$.
- **b.** Find $A_v$.
- **c.** Calculate $V_o$ if $V_i = 1$ mV.

***26.** For the network of Fig. 5.164:
- **a.** Calculate $I_B$ and $I_C$.
- **b.** Determine $r_e$.
- **c.** Determine $Z_i$ and $Z_o$.
- **d.** Find $A_v$.

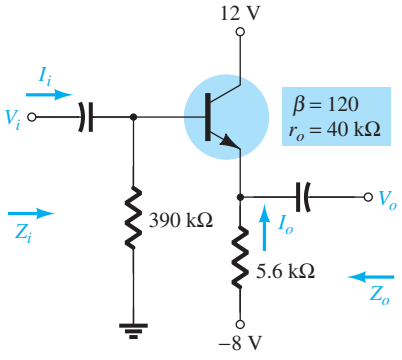



**FIG. 5.163**
*Problem 25.*

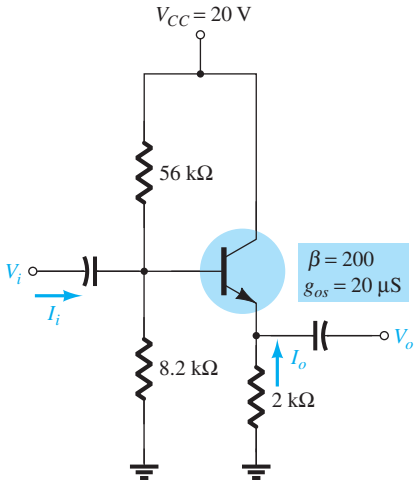



**FIG. 5.164**
*Problem 26.*

## 5.9 Common-Base Configuration

**27.** For the common-base configuration of Fig. 5.165:
- **a.** Determine $r_e$.
- **b.** Find $Z_i$ and $Z_o$.
- **c.** Calculate $A_v$.

***28.** For the network of Fig. 5.166, determine $A_v$.

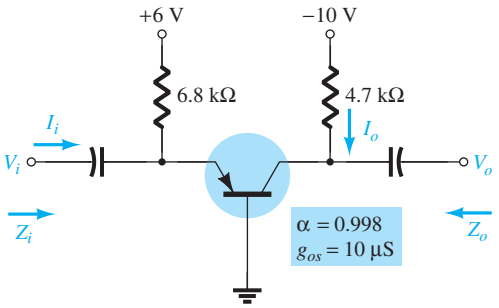



**FIG. 5.165**
*Problem 27.*

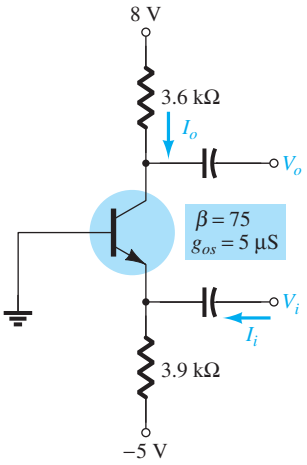



**FIG. 5.166**
*Problem 28.*

## 5.10 Collector Feedback Configuration

**29.** For the collector feedback configuration of Fig. 5.167:
- **a.** Determine $r_e$.
- **b.** Find $Z_i$ and $Z_o$.
- **c.** Calculate $A_v$.

***30.** Given $r_e = 10\ \Omega$, $\beta = 200$, $A_v = -160$, and $A_i = 19$ for the network of Fig. 5.168, determine $R_C$, $R_F$, and $V_{CC}$.

***31.** For the network of Fig. 5.49:
- **a.** Derive the approximate equation for $A_v$.
- **b.** Derive the approximate equations for $Z_i$ and $Z_o$.
- **c.** Given $R_C = 2.2\ \text{k}\Omega$, $R_F = 120\ \text{k}\Omega$, $R_E = 1.2\ \text{k}\Omega$, $\beta = 90$, and $V_{CC} = 10\ \text{V}$, calculate the magnitudes of $A_v$, $Z_i$, and $Z_o$ using the equations of parts (a) and (b).

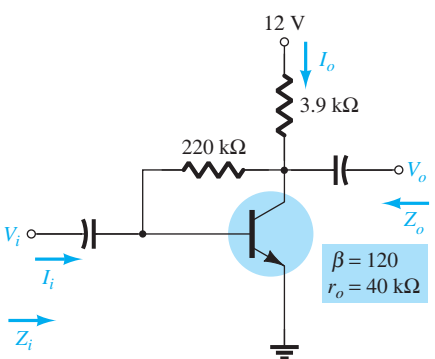



**FIG. 5.167**
*Problem 29.*

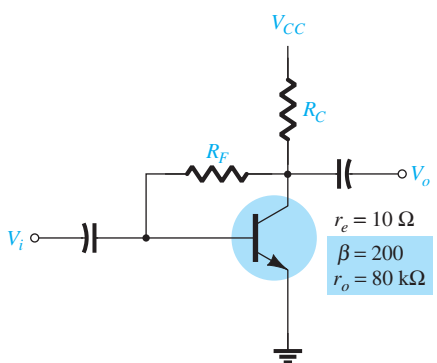



**FIG. 5.168**
*Problem 30.*

## 5.11 Collector DC Feedback Configuration

**32.** For the network of Fig. 5.169:
- **a.** Determine $Z_i$ and $Z_o$.
- **b.** Find $A_v$.

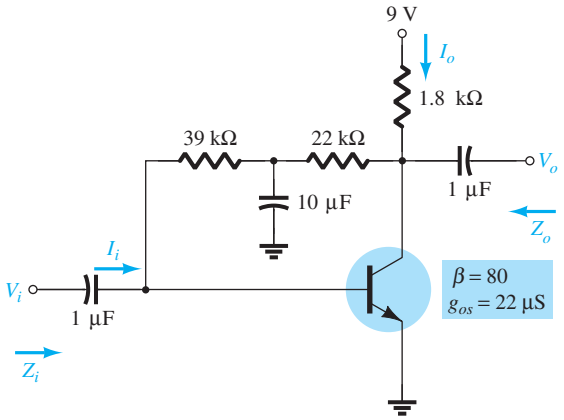



**FIG. 5.169**
*Problems 32 and 33.*

**33.** Repeat problem 32 with the addition of an emitter resistor $R_E = 0.68$ kΩ.

### 5.12–5.15 Effect of $R_L$ and $R_s$ and Two-Port Systems Approach

***34.** For the fixed-bias configuration of Fig. 5.170:
- **a.** Determine $A_{v_{NL}}$, $Z_i$, and $Z_o$.
- **b.** Sketch the two-port model of Fig. 5.63 with the parameters determined in part (a) in place.
- **c.** Calculate the gain $A_{v_L} = V_o/V_i$.
- **d.** Determine the current gain $A_{i_L} = I_o/I_i$.

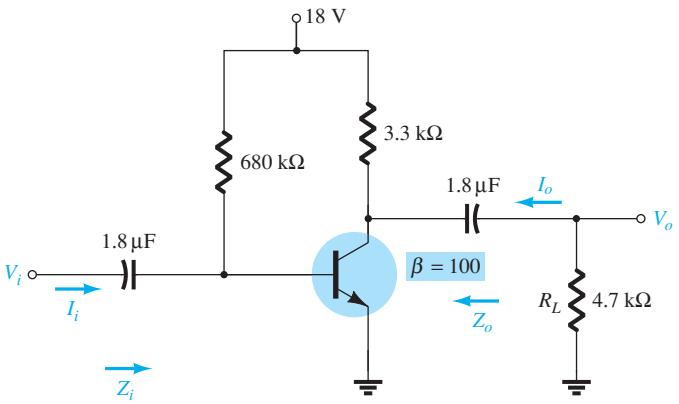



**FIG. 5.170**
*Problems 34 and 35.*

**35.**
- **a.** Determine the voltage gain $A_{v_L}$ for the network of Fig. 5.170 for $R_L = 4.7$ kΩ, 2.2 kΩ, and 0.5 kΩ. What is the effect of decreasing levels of $R_L$ on the voltage gain?
- **b.** How will $Z_i$, $Z_o$, and $A_{v_{NL}}$ change with decreasing values of $R_L$?

***36.** For the network of Fig. 5.171:
- **a.** Determine $A_{v_{NL}}$, $Z_i$, and $Z_o$.
- **b.** Sketch the two-port model of Fig. 5.63 with the parameters determined in part (a) in place.
- **c.** Determine $A_v = V_o/V_i$.
- **d.** Determine $A_{v_s} = V_o/V_s$.
- **e.** Change $R_s$ to 1 kΩ and determine $A_v$. How does $A_v$ change with the level of $R_s$?
- **f.** Change $R_s$ to 1 kΩ and determine $A_{v_s}$. How does $A_{v_s}$ change with the level of $R_s$?
- **g.** Change $R_s$ to 1 kΩ and determine $A_{v_{NL}}$, $Z_i$, and $Z_o$. How do they change with the change in $R_s$?
- **h.** For the original network of Fig. 5.171 calculate $A_i = I_o/I_i$.

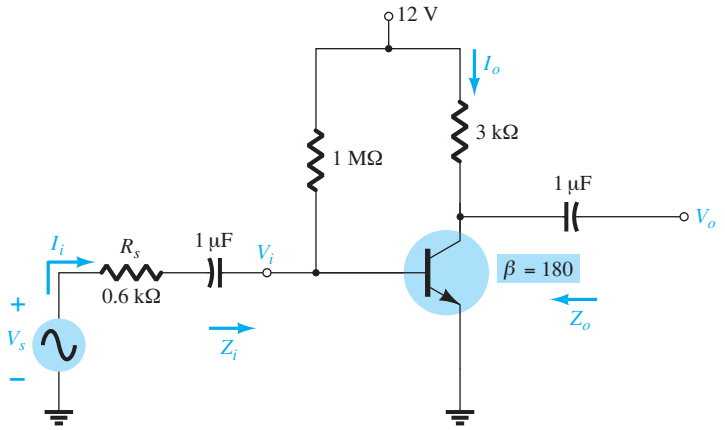



**FIG. 5.171**
*Problem 36.*

***37.** For the network of Fig. 5.172:

**a.** Determine $A_{v_{NL}}$, $Z_i$, and $Z_o$.

**b.** Sketch the two-port model of Fig. 5.63 with the parameters determined in part (a) in place.

**c.** Determine $A_{v_L}$ and $A_{v_s}$.

**d.** Calculate $A_{i_L}$.

**e.** Change $R_L$ to 5.6 kΩ and calculate $A_{v_s}$. What is the effect of increasing levels of $R_L$ on the gain?

**f.** Change $R_s$ to 0.5 kΩ (with $R_L$ at 2.7 kΩ) and comment on the effect of reducing $R_s$ on $A_{v_s}$.

**g.** Change $R_L$ to 5.6 kΩ and $R_s$ to 0.5 kΩ and determine the new levels of $Z_i$ and $Z_o$. How are the impedance parameters affected by changing levels of $R_L$ and $R_s$?

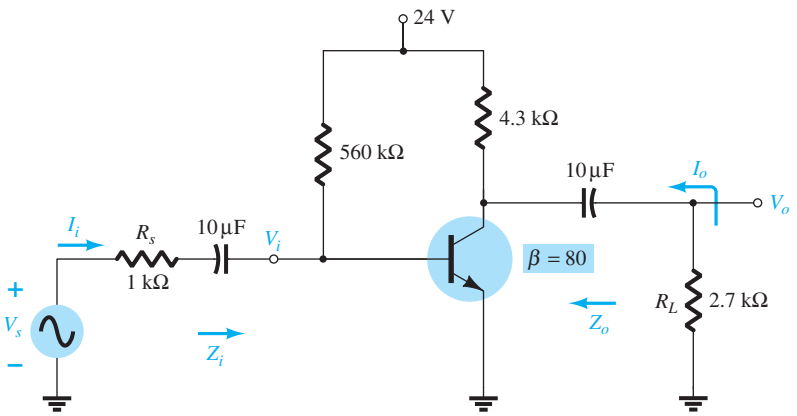



**FIG. 5.172**
*Problem 37.*

**38.** For the voltage-divider configuration of Fig. 5.173:

**a.** Determine $A_{v_{NL}}$, $Z_i$, and $Z_o$.

**b.** Sketch the two-port model of Fig. 5.63 with the parameters determined in part (a) in place.

**c.** Calculate the gain $A_{v_L}$.

**d.** Determine the current gain $A_{i_L}$.

**e.** Determine $A_{v_L}$, $A_{i_L}$, and $Z_o$ using the $r_e$ model and compare solutions.

**39. a.** Determine the voltage gain $A_{v_L}$ for the network of Fig. 5.173 with $R_L = 4.7$ kΩ, 2.2 kΩ, and 0.5 kΩ. What is the effect of decreasing levels of $R_L$ on the voltage gain?

**b.** How will $Z_i$, $Z_o$, and $A_{v_{NL}}$ change with decreasing levels of $R_L$?

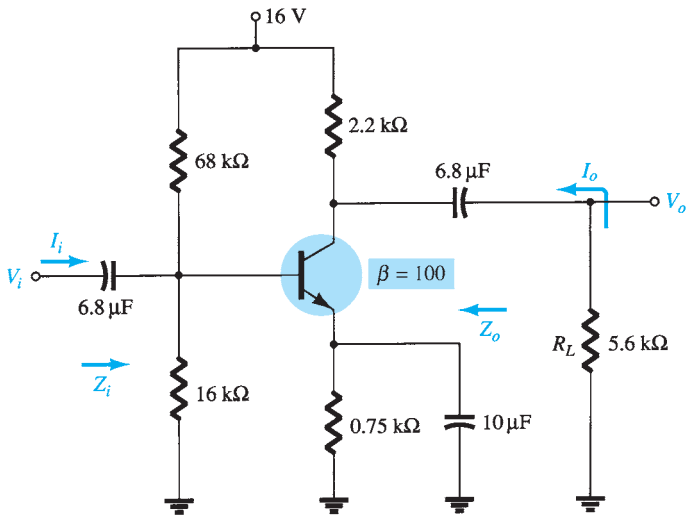



**FIG. 5.173**
*Problems 38 and 39.*

**40.** For the emitter-stabilized network of Fig. 5.174:
- **a.** Determine $A_{v_{NL}}$, $Z_i$, and $Z_o$.
- **b.** Sketch the two-port model of Fig. 5.63 with the values determined in part (a).
- **c.** Determine $A_{v_L}$ and $A_{v_s}$.
- **d.** Change $R_s$ to 1 kΩ. What is the effect on $A_{v_{NL}}$, $Z_i$, and $Z_o$?
- **e.** Change $R_s$ to 1 kΩ and determine $A_{v_L}$ and $A_{v_s}$. What is the effect of increasing levels of $R_s$ on $A_{v_L}$ and $A_{v_s}$?
- **f.** Determine $A_i = I_o/I_i$.

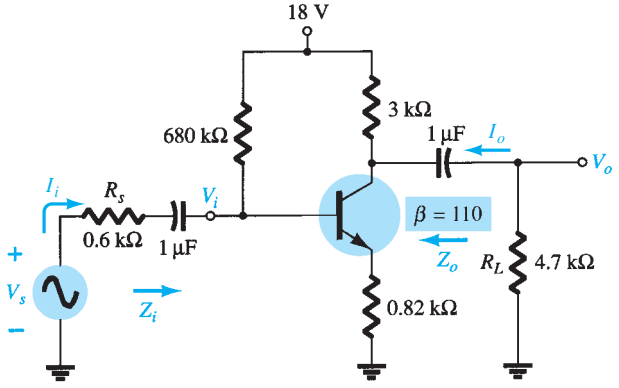



**FIG. 5.174**
*Problem 40.*

***41.** For the network of Fig. 5.175:
- **a.** Determine $A_{v_{NL}}$, $Z_i$, and $Z_o$.
- **b.** Sketch the two-port model of Fig. 5.63 with the values determined in part (a).
- **c.** Determine $A_{v_L}$ and $A_{v_s}$.
- **d.** Change $R_s$ to 1 kΩ and determine $A_{v_L}$ and $A_{v_s}$. What is the effect of increasing levels of $R_s$ on the voltage gains?
- **e.** Change $R_s$ to 1 kΩ and determine $A_{v_{NL}}$, $Z_i$, and $Z_o$. What is the effect of increasing levels of $R_s$ on the parameters?
- **f.** Change $R_L$ to 5.6 kΩ and determine $A_{v_L}$ and $A_{v_s}$. What is the effect of increasing levels of $R_L$ on the voltage gains? Maintain $R_s$ at its original level of 0.6 kΩ.
- **g.** Determine $A_i = \dfrac{I_o}{I_i}$ with $R_L = 2.7\ \text{k}\Omega$ and $R_s = 0.6\ \text{k}\Omega$.

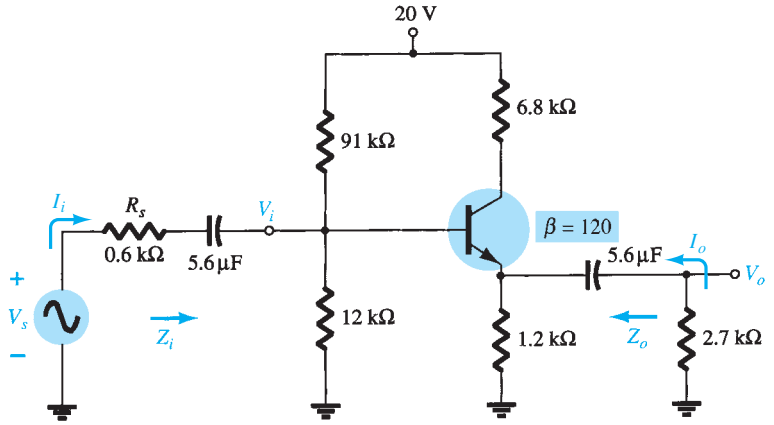



**FIG. 5.175**
*Problem 41.*

***42.** For the common-base network of Fig. 5.176:

- **a.** Determine $Z_i$, $Z_o$, and $A_{v_{NL}}$.
- **b.** Sketch the two-port model of Fig. 5.63 with the parameters of part (a) in place.
- **c.** Determine $A_{v_L}$ and $A_{v_s}$.
- **d.** Determine $A_{v_L}$ and $A_{v_s}$ using the $r_e$ model and compare with the results of part (c).
- **e.** Change $R_s$ to 0.5 kΩ and $R_L$ to 2.2 kΩ and calculate $A_{v_L}$ and $A_{v_s}$. What is the effect of changing levels of $R_s$ and $R_L$ on the voltage gains?
- **f.** Determine $Z_o$ if $R_s$ changed to 0.5 kΩ with all other parameters as appearing in Fig. 5.176. How is $Z_o$ affected by changing levels of $R_s$?
- **g.** Determine $Z_i$ if $R_L$ is reduced to 2.2 kΩ. What is the effect of changing levels of $R_L$ on the input impedance?
- **h.** For the original network of Fig. 5.176 determine $A_i = I_o/I_i$.

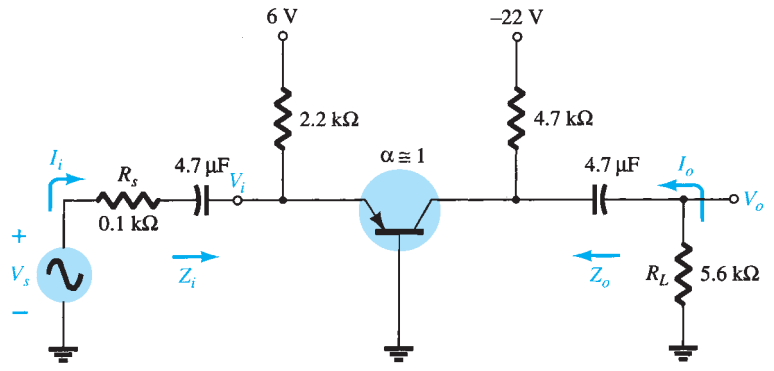



**FIG. 5.176**
*Problem 42.*

## 5.16 Cascaded Systems

***43.** For the cascaded system of Fig. 5.177 with two identical stages, determine:

- **a.** The loaded voltage gain of each stage.
- **b.** The total gain of the system, $A_v$ and $A_{v_s}$.
- **c.** The loaded current gain of each stage.
- **d.** The total current gain of the system $A_{i_L} = I_o/I_i$.
- **e.** How $Z_i$ is affected by the second stage and $R_L$.
- **f.** How $Z_o$ is affected by the first stage and $R_s$.
- **g.** The phase relationship between $V_o$ and $V_i$.

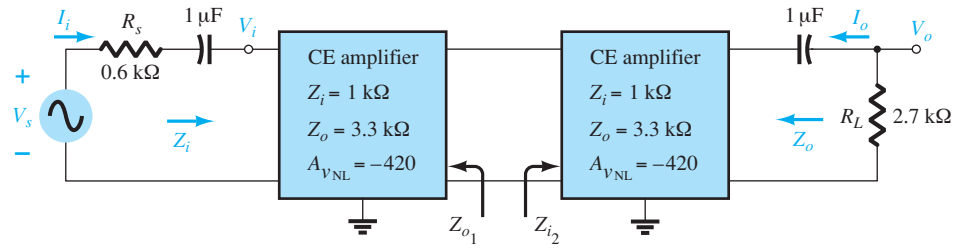



**FIG. 5.177**
*Problem 43.*

***44.** For the cascaded system of Fig. 5.178, determine:
- **a.** The loaded voltage gain of each stage.
- **b.** The total gain of the system, $A_{v_L}$ and $A_{v_s}$.
- **c.** The loaded current gain of each stage.
- **d.** The total current gain of the system.
- **e.** How $Z_i$ is affected by the second stage and $R_L$.
- **f.** How $Z_o$ is affected by the first stage and $R_s$.
- **g.** The phase relationship between $V_o$ and $V_i$.

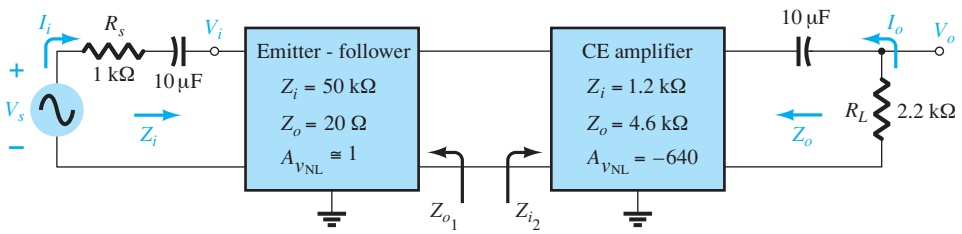



**FIG. 5.178**
*Problem 44.*

**45.** For the BJT cascade amplifier of Fig. 5.179, calculate the dc bias voltages and collector current for each stage.

**46.** **a.** Calculate the voltage gain of each stage and the overall ac voltage gain for the BJT cascade amplifier circuit of Fig. 5.179.
- **b.** Find $A_{i_T} = I_o/I_i$.

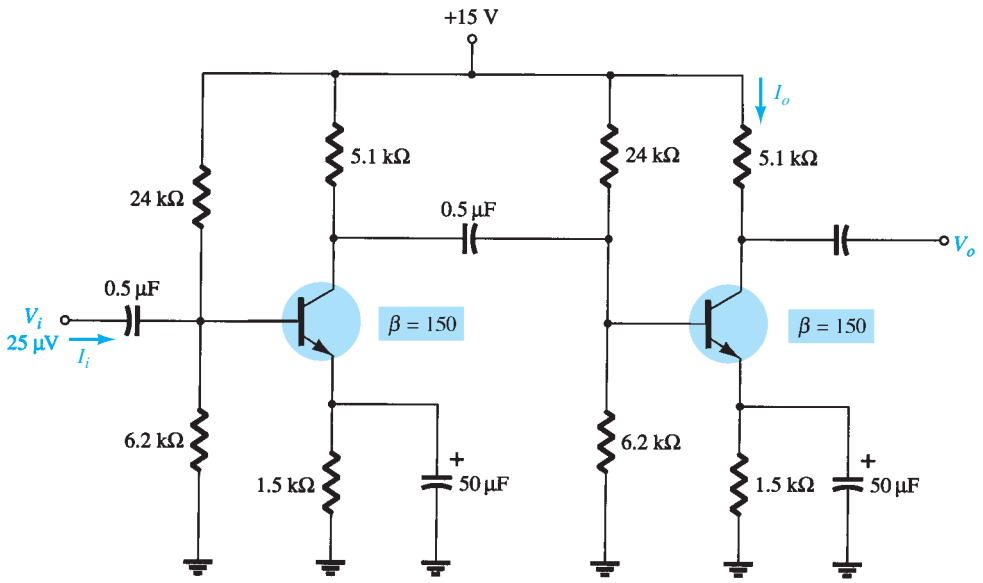



**FIG. 5.179**
*Problems 45 and 46.*

**47.** For the cascode amplifier circuit of Fig. 5.180, calculate the dc bias voltages $V_{B_1}$, $V_{B_2}$, and $V_{C_2}$.

***48.** For the cascode amplifier circuit of Fig. 5.180, calculate the voltage gain $A_v$ and output voltage $V_o$.

**49.** Calculate the ac voltage across a 10-kΩ load connected at the output of the circuit in Fig. 5.180.

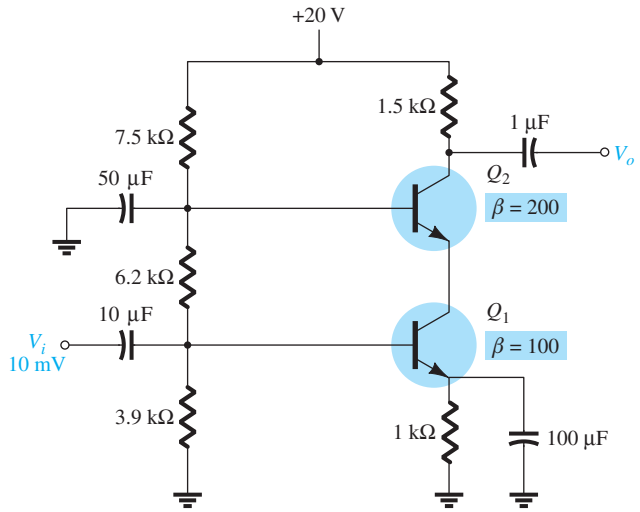



**FIG. 5.180**
*Problems 47 and 49.*

## 5.17 Darlington Connection

**50.** For the Darlington network of Fig. 5.181:

**a.** Determine the dc levels of $V_{B_1}$, $V_{C_1}$, $V_{E_2}$, $V_{CB_1}$, and $V_{CE_2}$.

**b.** Find the currents $I_{B_1}$, $I_{B_2}$, and $I_{E_2}$.

**c.** Calculate $Z_i$ and $Z_o$.

**d.** Determine the voltage gain $A_v = V_o/V_i$ and current gain $A_i = I_o/I_i$.

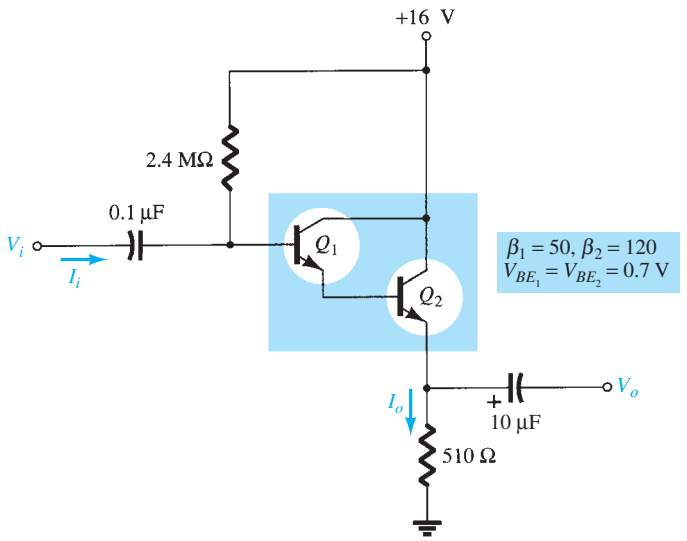



**FIG. 5.181**
*Problems 50 through 53.*

**51.** Repeat problem 50 with a load resistor of 1.2 kΩ.

**52.** Determine $A_v = V_o/V_s$ for the network of Fig. 5.181 if the source has an internal resistance of 1.2 kΩ and the applied load is 10 kΩ.

**53.** A resistor $R_C = 470\ \Omega$ is added to the network of Fig. 5.181 along with a bypass capacitor $C_E = 5\ \mu$F across the emitter resistor. If $\beta_D = 4000$, $V_{BE_T} = 1.6$ V, and $r_{o_1} = r_{o_2} = 40\ \text{k}\Omega$ for a packaged Darlington amplifier:

**a.** Find the dc levels of $V_{B_1}$, $V_{E_2}$, and $V_{CE_2}$.

**b.** Determine $Z_i$ and $Z_o$.

**c.** Determine the voltage gain $A_v = V_o/V_i$ if the output voltage $V_o$ is taken off the collector terminal via a coupling capacitor of 10 $\mu$F.

## 5.18 Feedback Pair

**54.** For the feedback pair of Fig. 5.182:
- **a.** Calculate the dc voltages $V_{B_1}$, $V_{B_2}$, $V_{C_1}$, $V_{C_2}$, $V_{E_1}$, and $V_{E_2}$.
- **b.** Determine the dc currents $I_{B_1}$, $I_{C_1}$, $I_{B_2}$, $I_{C_2}$, and $I_{E_2}$.
- **c.** Calculate the impedances $Z_i$ and $Z_o$.
- **d.** Find the voltage gain $A_v = V_o/V_i$.
- **e.** Determine the current gain $A_i = I_o/I_i$.

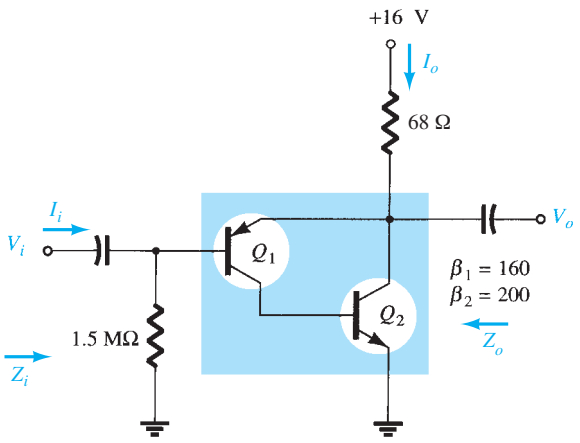



**FIG. 5.182**
*Problems 54 and 55.*

**55.** Repeat problem 54 if a 22-Ω resistor is added between $V_{E_2}$ and ground.

**56.** Repeat problem 54 if a load resistance of 1.2 kΩ is introduced.

## 5.19 The Hybrid Equivalent Model

**57.** Given $I_E(\text{dc}) = 1.2$ mA, $\beta = 120$, and $r_o = 40$ kΩ, sketch the following:
- **a.** Common-emitter hybrid equivalent model.
- **b.** Common-emitter $r_e$ equivalent model.
- **c.** Common-base hybrid equivalent model.
- **d.** Common-base $r_e$ equivalent model.

**58.** Given $h_{ie} = 2.4\,\text{k}\Omega$, $h_{fe} = 100$, $h_{re} = 4 \times 10^{-4}$, and $h_{oe} = 25\ \mu\text{S}$, sketch the following:
- **a.** Common-emitter hybrid equivalent model.
- **b.** Common-emitter $r_e$ equivalent model.
- **c.** Common-base hybrid equivalent model.
- **d.** Common-base $r_e$ equivalent model.

**59.** Redraw the common-emitter network of Fig. 5.3 for the ac response with the approximate hybrid equivalent model substituted between the appropriate terminals.

**60.** Redraw the network of Fig. 5.183 for the ac response with the $r_e$ model inserted between the appropriate terminals. Include $r_o$.

**61.** Redraw the network of Fig. 5.184 for the ac response with the $r_e$ model inserted between the appropriate terminals. Include $r_o$.

**62.** Given the typical values of $h_{ie} = 1\,\text{k}\Omega$, $h_{re} = 2 \times 10^{-4}$, and $A_v = -160$ for the input configuration of Fig. 5.185:
- **a.** Determine $V_o$ in terms of $V_i$.
- **b.** Calculate $I_b$ in terms of $V_i$.
- **c.** Calculate $I_b$ if $h_{re}V_o$ is ignored.
- **d.** Determine the percentage difference in $I_b$ using the following equation:

$$\%\ \text{difference in } I_b = \frac{I_b(\text{without } h_{re}) - I_b(\text{with } h_{re})}{I_b(\text{without } h_{re})} \times 100\%$$

- **e.** Is it a valid approach to ignore the effects of $h_{re}V_o$ for the typical values employed in this example?

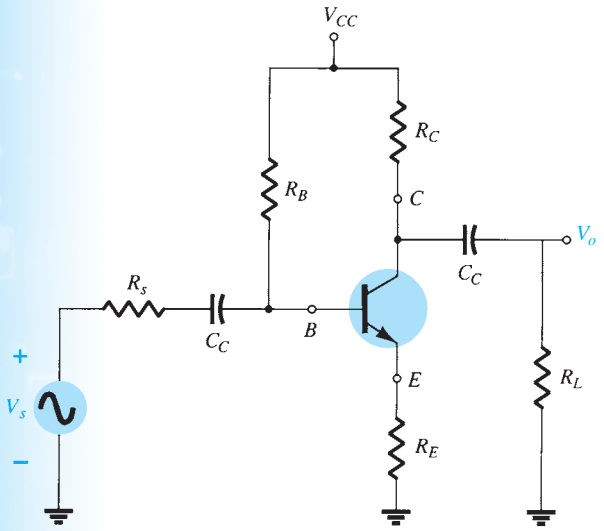



**FIG. 5.183**
*Problem 60.*

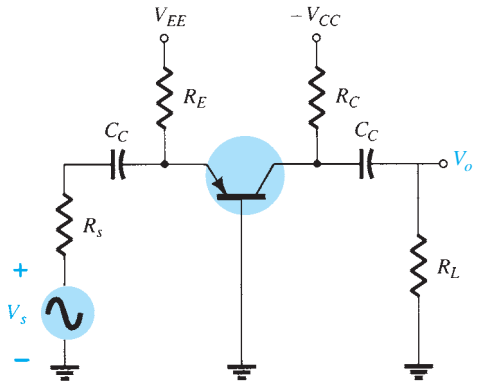



**FIG. 5.184**
*Problem 61.*

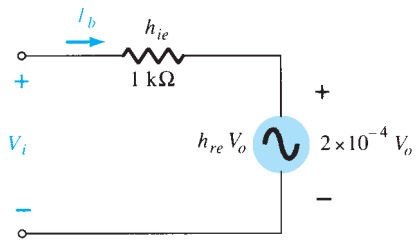



**FIG. 5.185**
*Problems 62 and 64.*

**63.** Given the typical values of $R_L = 2.2\,\text{k}\Omega$ and $h_{oe} = 20\,\mu\text{S}$, is it a good approximation to ignore the effects of $1/h_{oe}$ on the total load impedance? What is the percentage difference in total loading on the transistor using the following equation?

$$\%\text{ difference in total load} = \frac{R_L - R_L \| (1/h_{oe})}{R_L} \times 100\%$$

**64.** Repeat Problem 62 using the average values of the parameters of Fig. 5.92 with $A_v = -180$.

**65.** Repeat Problem 63 for $R_L = 3.3\,\text{k}\Omega$ and the average value of $h_{oe}$ in Fig. 5.92.

## 5.20 Approximate Hybrid Equivalent Circuit

**66.** **a.** Given $\beta = 120$, $r_e = 4.5\,\Omega$, and $r_o = 40\,\text{k}\Omega$, sketch the approximate hybrid equivalent circuit.
**b.** Given $h_{ie} = 1\,\text{k}\Omega$, $h_{re} = 2 \times 10^{-4}$, $h_{fe} = 90$, and $h_{oe} = 20\,\mu\text{S}$, sketch the $r_e$ model.

**67.** For the network of Problem 11:
**a.** Determine $r_e$.
**b.** Find $h_{fe}$ and $h_{ie}$.
**c.** Find $Z_i$ and $Z_o$ using the hybrid parameters.
**d.** Calculate $A_v$ and $A_i$ using the hybrid parameters.
**e.** Determine $Z_i$ and $Z_o$ if $h_{oe} = 50\,\mu\text{S}$.
**f.** Determine $A_v$ and $A_i$ if $h_{oe} = 50\,\mu\text{S}$.
**g.** Compare the solutions above with those of Problem 9. (Note: The solutions are available in Appendix E if Problem 11 was not performed.)

**68.** For the network of Fig. 5.186:
**a.** Determine $Z_i$ and $Z_o$.
**b.** Calculate $A_v$ and $A_i$.
**c.** Determine $r_e$ and compare $\beta r_e$ to $h_{ie}$.

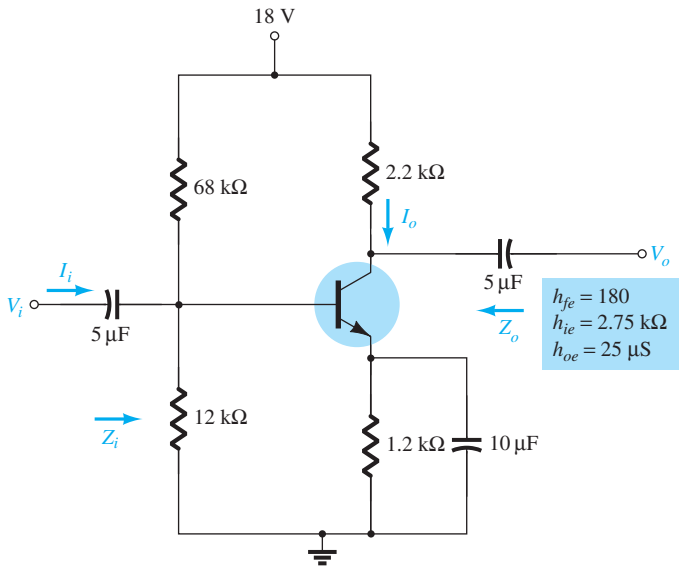



**FIG. 5.186**
*Problem 68.*

***69.** For the common-base network of Fig. 5.187:

**a.** Determine $Z_i$ and $Z_o$.
**b.** Calculate $A_v$ and $A_i$.
**c.** Determine $\alpha$, $\beta$, $r_e$, and $r_o$.

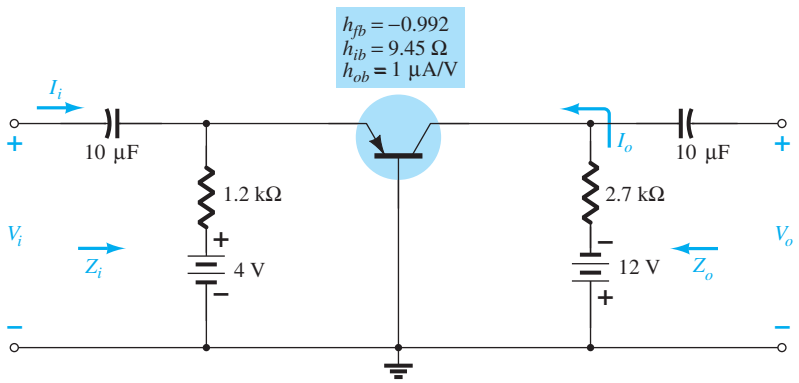



**FIG. 5.187**
*Problem 69.*

## 5.21 Complete Hybrid Equivalent Model

***70.** Repeat parts (a) and (b) of Problem 68 with $h_{re} = 2 \times 10^{-4}$ and compare results.

***71.** For the network of Fig. 5.188, determine:

**a.** $Z_i$.
**b.** $A_v$.
**c.** $A_i = I_o/I_i$.
**d.** $Z_o$.

***72.** For the common-base amplifier of Fig. 5.189, determine:

**a.** $Z_i$.
**b.** $A_i$.
**c.** $A_v$.
**d.** $Z_o$.

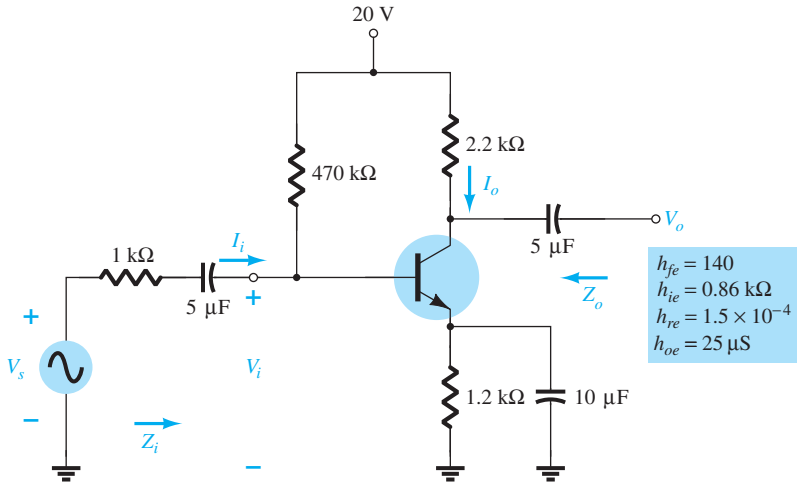



**FIG. 5.188**
*Problem 71.*

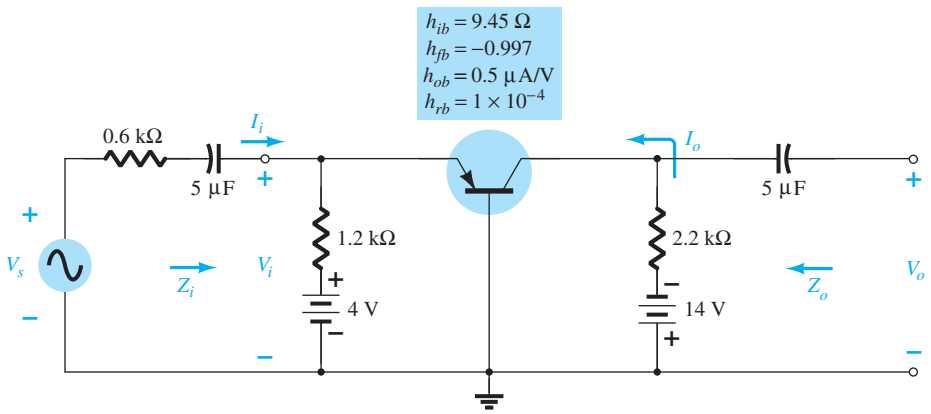



**FIG. 5.189**
*Problem 72.*

## 5.22 Hybrid $\pi$ Model

**73.** **a.** Sketch the Giacoletto (hybrid $\pi$) model for a common-emitter transistor if $r_b = 4\ \Omega$, $C_\pi = 5$ pF, $C_u = 1.5$ pF, $h_{oe} = 18\ \mu$S, $\beta = 120$, and $r_e = 14$.

**b.** If the applied load is 1.2 kΩ and the source resistance is 250 Ω, draw the approximate hybrid $\pi$ model for the low- and mid-frequency range.

## 5.23 Variations of Transistor Parameters

For Problems 74 through 80, use Figs. 5.124 through 5.126.

**74.** **a.** Using Fig. 5.124, determine the magnitude of the percentage change in $h_{fe}$ for an $I_C$ change from 0.2 mA to 1 mA using the equation

$$\%\ \text{change} = \left| \frac{h_{fe}(0.2\ \text{mA}) - h_{fe}(1\ \text{mA})}{h_{fe}(0.2\ \text{mA})} \right| \times 100\%$$

**b.** Repeat part (a) for an $I_C$ change from 1 mA to 5 mA.

**75.** Repeat Problem 74 for $h_{ie}$ (same changes in $I_C$).

**76.** **a.** If $h_{oe} = 20\ \mu$S at $I_C = 1$ mA on Fig. 5.124, what is the approximate value of $h_{oe}$ at $I_C = 0.2$ mA?

**b.** Determine its resistive value at 0.2 mA and compare to a resistive load of 6.8 kΩ. Is it a good approximation to ignore the effects of $1/h_{oe}$ in this case?

**77.** **a.** If $h_{oe} = 20\ \mu$S at $I_C = 1$ mA of Fig. 5.124, what is the approximate value of $h_{oe}$ at $I_C = 10$ mA?

**b.** Determine its resistive value at 10 mA and compare to a resistive load of 6.8 kΩ. Is it a good approximation to ignore the effects of $1/h_{oe}$ in this case?

**78.** **a.** If $h_{re} = 2 \times 10^{-4}$ at $I_C = 1$ mA on Fig. 5.124, determine the approximate value of $h_{re}$ at 0.1 mA.

**b.** For the value of $h_{re}$ determined in part (a), can $h_{re}$ be ignored as a good approximation if $A_v = 210$?

**79.** **a.** Based on a review of the characteristics of Fig. 5.124, which parameter changed the least for the full range of collector current?
**b.** Which parameter changed the most?
**c.** What are the maximum and minimum values of $1/h_{oe}$? Is the approximation $1/h_{oe} \| R_L \cong R_L$ more appropriate at high or low levels of collector current?
**d.** In which region of current spectrum is the approximation $h_{re}V_{ce} \cong 0$ the most appropriate?

**80.** **a.** Based on a review of the characteristics of Fig. 5.126, which parameter changed the most with increase in temperature?
**b.** Which changed the least?
**c.** What are the maximum and minimum values of $h_{fe}$? Is the change in magnitude significant? Was it expected?
**d.** How does $r_e$ vary with increase in temperature? Simply calculate its level at three or four points and compare their magnitudes.
**e.** In which temperature range do the parameters change the least?

## 5.24 Troubleshooting

***81.** Given the network of Fig. 5.190:
**a.** Is the network properly biased?
**b.** What problem in the network construction could cause $V_B$ to be 6.22 V and obtain the given waveform of Fig. 5.190?

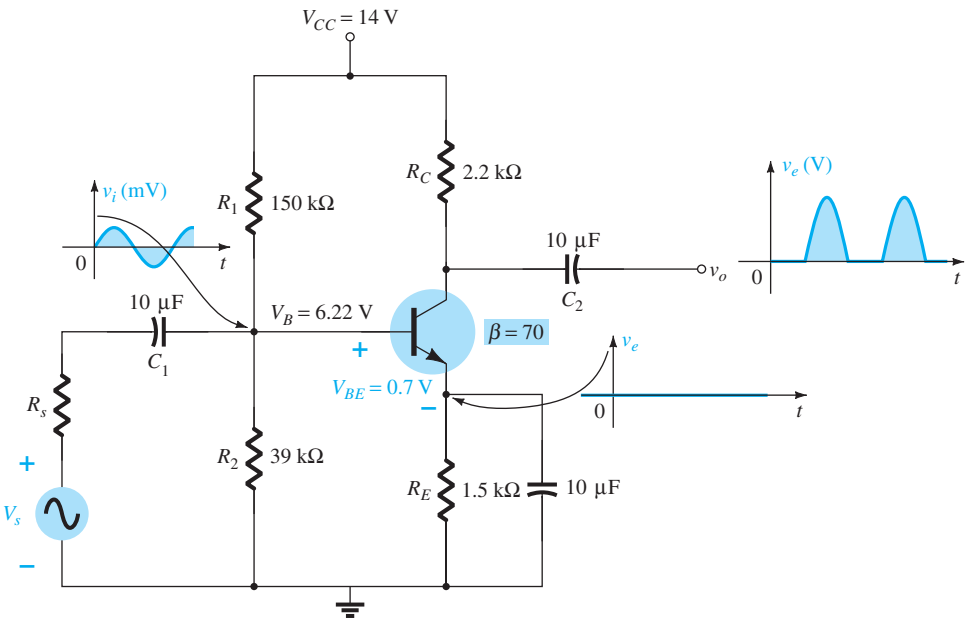



**FIG. 5.190**
*Problem 81.*

## 5.27 Computer Analysis

**82.** Using PSpice Windows, determine the voltage gain for the network of Fig. 5.25. Display the input and output waveforms.

**83.** Using PSpice Windows, determine the voltage gain for the network of Fig. 5.32. Display the input and output waveforms.

**84.** Using PSpice Windows, determine the voltage gain for the network of Fig. 5.44. Display the input and output waveforms.

**85.** Using Multisim, determine the voltage gain for the network of Fig. 5.28.

**86.** Using Multisim, determine the voltage gain for the network of Fig. 5.39.

**87.** Using PSpice Windows, determine the level of $V_o$ for $V_i = 1$ mV for the network of Fig. 5.69. For the capacitive elements assume a frequency of 1 kHz.

**88.** Repeat Problem 87 for the network of Fig. 5.71.

**89.** Repeat Problem 87 for the network of Fig. 5.82.

**90.** Repeat Problem 87 using Multisim.

**91.** Repeat Problem 87 using Multisim.