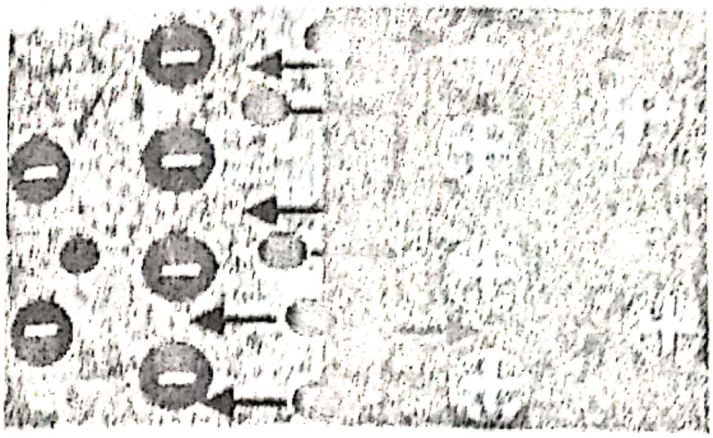

The P-N Junction

1. The *P-N* Junction
2. Formation of Depletion Layer
3. Junction or Barrier Voltage (V_B)
4. Effect of Temperature on Barrier Voltage
5. Forward Biased *P-N* Junction
6. Forward V/I Characteristics
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8. Reverse Saturation Current (I_s or I_0)
9. Reverse V/I Characteristic
10. Combined Forward and Reverse V/I Characteristics
11. Junction Breakdown
12. Junction Capacitance
13. Equivalent Circuit of a P-N Junction

13.1. The *P-N* Junction

It is possible to manufacture a single piece of a semi conductor material (either Ge or Si) one half of which is doped by *P*-type impurity and the other half by *N*-type impurity as shown in Fig. 13.1. The plane dividing the two halves or zones is called a ***P-N* Junction.** It should be noted that a useful *P-N* junction cannot be produced by connecting *P*-type material to *N*-type material by welding etc., because this would give rise to discontinuities across the crystal structure.

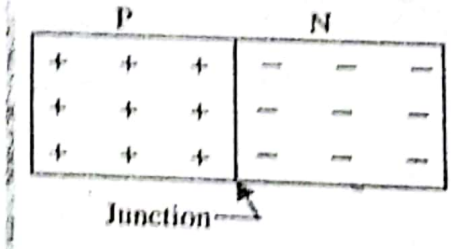
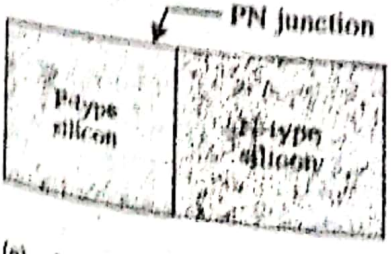
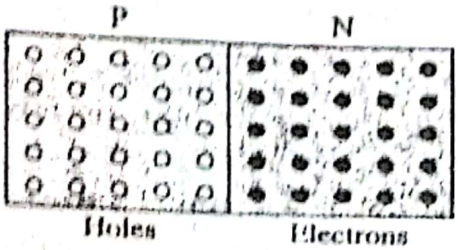


Fig. 13.1



(a) A P-N junction in a diode.



(b) The N region has in a diode many conduction electrons and the P region has many holes.

During the formation of a *P-N* junction, following two phenomena take place :

(*i*) a thin depletion layer (or region) is set up on both sides of the junction and is so-called because it is depleted or devoid of free charge carriers. Its width is about 1 μm (10^{-6} m);

(*ii*) a junction or barrier potential V_B is developed across the junction whose value is about 0.3 V for Ge and 0.7 V for Si.

When a *P-N* junction is packed as a semiconductor device, it is called a *P-N* junction diode.

13.2. Formation of Depletion Layer

Suppose that a *P-N* junction has just been formed. At that instant, holes are still in the *P*-region and electrons in the *N*-region. However, there is greater concentration of holes in *P*-region (where they form majority carriers) than in *N*-region (where they form minority carriers). Similarly, concentration of electrons is greater in *N*-region than in *P*-region (where they exist as minority carriers). This difference in concentration establishes a density gradient across the junction resulting in majority carrier diffusion. Holes diffuse from *P*- to *N*-region and electrons from *N*- to *P*-region and terminate their existence by recombination as shown in Fig. 13.2 (*a*).

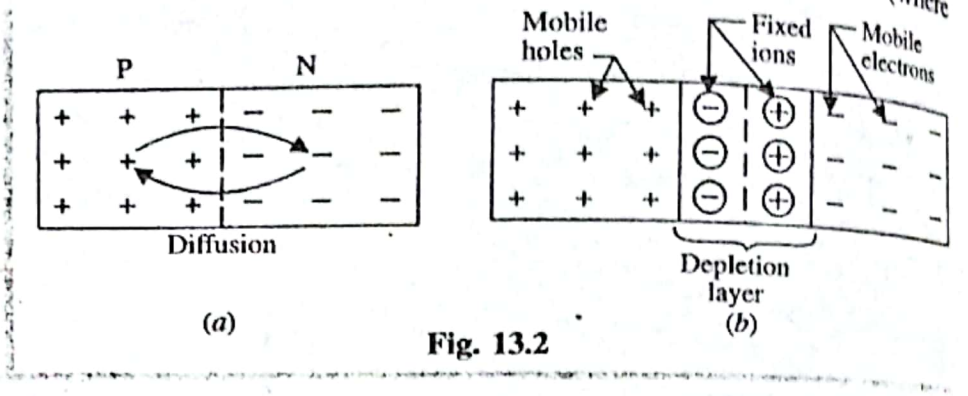
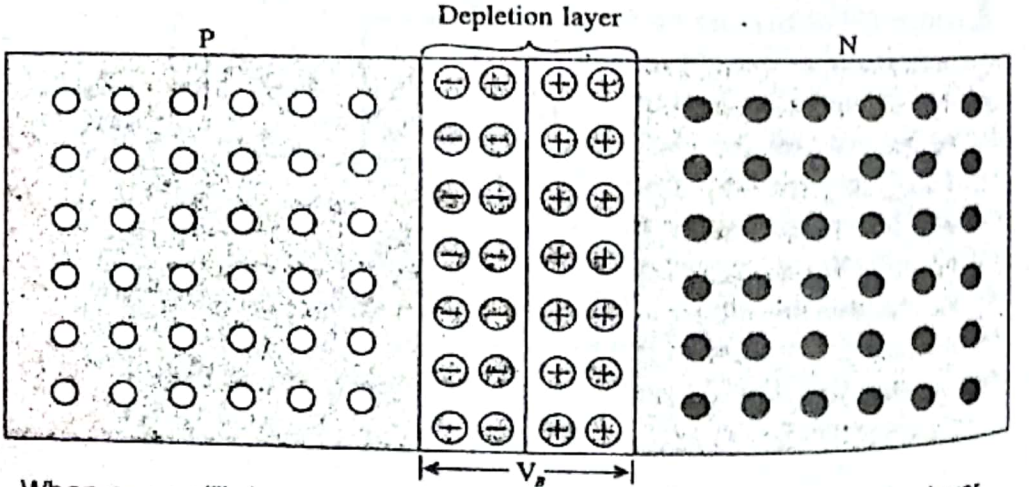


Fig. 13.2

This recombination of free and mobile holes and electrons produces the narrow region at the junction called *depletion layer*. It is so-called because this region is *devoid or depleted of free and mobile charge carriers* though it does contain **fixed** or **immobile** positive and negative ions.

This production of ions is due to the fact that the impurity atoms which provide migratory electrons and holes are themselves left behind in an ionised state bearing a charge which is opposite to that of the departed carrier. For example, when an electron migrates across the junction from *N*-region to *P*-region, it leaves behind an atom that is one electron short of its normal quota. This atom is now ionised and has a positive charge. It is said to be *uncovered*. These impurity ions so produced are fixed in their positions in the crystal lattice in the *P*- and *N*-regions. Hence, as shown in Fig. 13.2 (*b*), they form parallel rows or plates of opposite charges facing each other across the depletion layer. As seen, depletion layer contains no free and mobile charge carriers but only fixed and immobile ions. Hence, this layer (or region) behaves like an insulator and due to the presence of rows of fixed charges, it possesses capacitance as explained in Art. 13.11.



When an equilibrium condition is reached in a diode the depletion layer has widened to a point where no more electrons can across the P-N junction.

13.3. Junction or Barrier Voltage (V_B)

As explained in Art. 13.2, depletion layer of a *P-N* junction diode has no free charge carriers

but only fixed rows of oppositely-charged ions on its two sides. Because of this charge separation, an electric potential V_B is established across the junction *even when the junction is not connected to any external source of e.m.f.* (Fig. 13.3). It is known as *junction or barrier* potential. It stops further flow of carriers across the junction unless supplied by energy from an external source. At room temperature of 300° K, V_B is about 0.3 V for Ge and 0.7 V for Si. Its value depends on doping density, electronic charge and temperature.

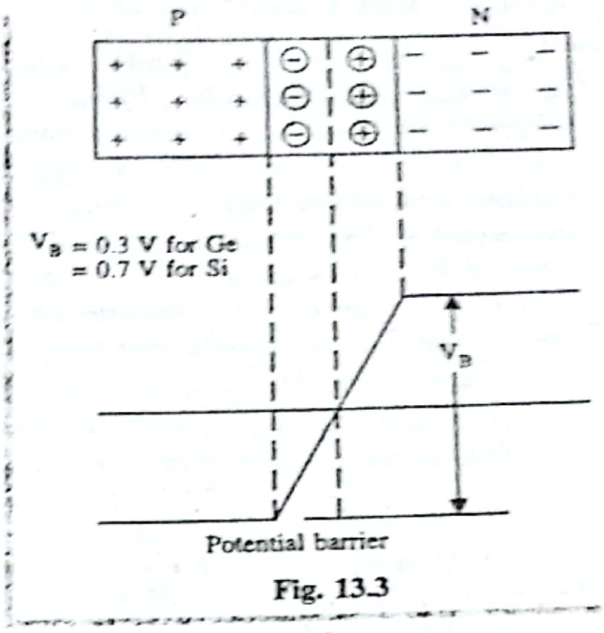


Fig. 13.3

The processes involved in the formation of a *P-N* junction are summarized below :

1. Holes from the *P*-side diffuse into the *N*-side where they combine with free electrons.
2. Free electrons from the *N*-side diffuse into the *P*-side where they combine with holes.
3. The diffusion current (also known as recombination current) decays exponentially both with time and distance from the junction.
4. Due to the departure of free and mobile carriers from both sides of the junction, a depletion layer (centred around the junction) is formed. This layer contains only immobile or fixed (also called uncovered) ions of opposite polarity.
5. These uncovered by fixed ions set up a potential barrier across the junction.
6. This potential difference opposes the diffusion of free majority charge carriers from one side of the junction to the other* till the process is completely stopped.
7. The width of depletion layer depends on the doping level. For heavy doping, depletion layer is physically thin because a diffusing charge carrier (either free electron or hole) has not to travel far across the junction for recombination (short lifetime). Opposite is the case if light doping is used.

13.4. Effect of Temperature on Barrier Voltage

Barrier voltage depends on doping density, electronic charge and temperature. For a given junction, the first two factors are constant, thus making V_B dependent on temperature. With increase in temperature, more minority charge carriers are produced leading to their increased drift across the junction. As a result, equilibrium occurs at a slightly lower barrier potential. It is found that both for Ge and Si, V_B decreases by about 2 mV/°C.

or $\Delta V_B = -0.002.\Delta t$

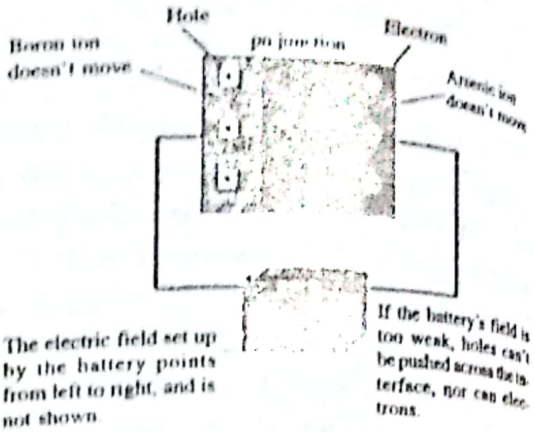
where Δt = change in temp. in °C.

13.5. Forward Biased *P-N* Junction

Suppose positive battery terminal is connected to *P*-region of a semiconductor and the negative battery terminal to the *N*-region as shown in Fig. 13.4. In that case, the junction is said to be biased in the forward direction because it permits easy flow of current across the junction. The current flow may be explained in the following two ways :

* Incidentally, this potential barrier *aids* in the transfer of thermally-generated minority charge carriers from one side of the junction to the other.

(*i*) As soon as battery connection is made, holes are *repelled* by the positive battery terminal and electrons are repelled by the negative battery terminal with the result that both the electrons and the holes are driven *towards* the junction where they recombine. This *en masse* movement of electrons to the left and that of holes to the right of the junction constitutes a large current flow through the semiconductor. Obviously, the crystal offers *low resistance in the forward direction*.



Incidentally, it may be noted that though there is movement of both electrons and holes *inside* the crystal, only free electrons move in the external circuit *i.e.*, in the battery-connected wire (Art. 12.20).

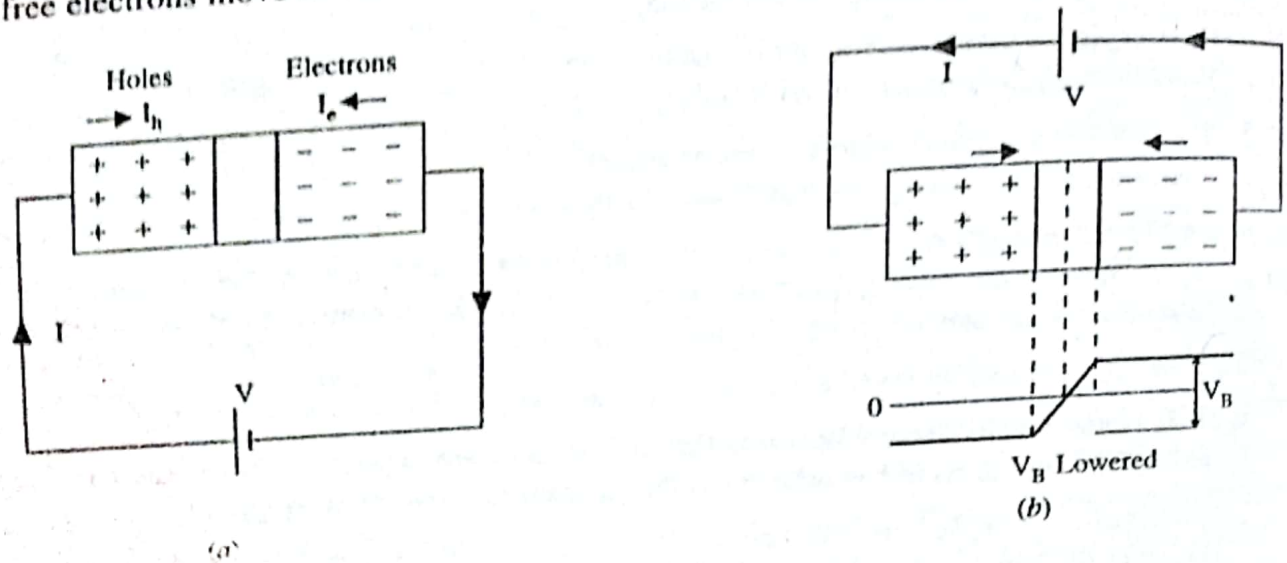


Fig. 13.4

(*ii*) Another way to explain current flow in the forward direction is to say that due to the applied external voltage, the barrier potential is reduced which now allows more current to flow across the junction [Fig. 13.4 (*b*)]. Incidentally, it may be noted that forward bias reduces the thickness of the depletion layer as shown in Fig. 13.5.

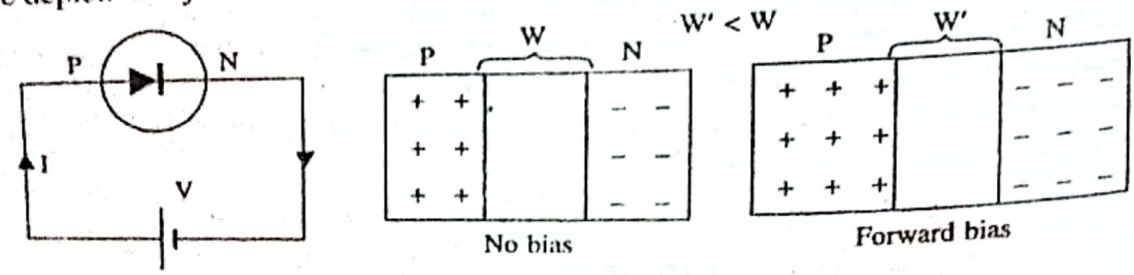


Fig. 13.5

13.6. Forward V/I Characteristics

A typical *V/I* characteristic for a forward-biased *P-N* junction is shown in Fig. 13.6. It is seen that forward current rises exponentially with the applied forward voltage. However, at ordinary room temperature, a p.d. of about 0.3 V is required before a reasonable amount of forward current starts flowing in a germanium junction. This voltage is known as *threshold voltage* (V_{th}) *or cut-in voltage or knee voltage* V_K. It is practically the same as barrier voltage V_B. Its value for silicon junction is about 0.7 volt. For $V < V_{th}$, current flow is negligible. But as applied voltage increases beyond the threshold value, the forward current increases sharply. If forward voltage is increased beyond a certain safe value, it will produce an extremely large current which may destroy the junction due to

overheating. **Ge devices can stand junction temperature around 100° C whereas Si units can function upto 175°C.**

Obviously, the *forward-biased junction has a low resistance.* For point *B* in Fig. 13.6, the forward resistance for Si is

$$R_F = \frac{0.8\ V}{20\,mA} = 40\ \Omega$$

Similarly, for point *A* on the Ge curve

$$R_F = \frac{0.36\ V}{20\ mA} = 18\ \Omega$$

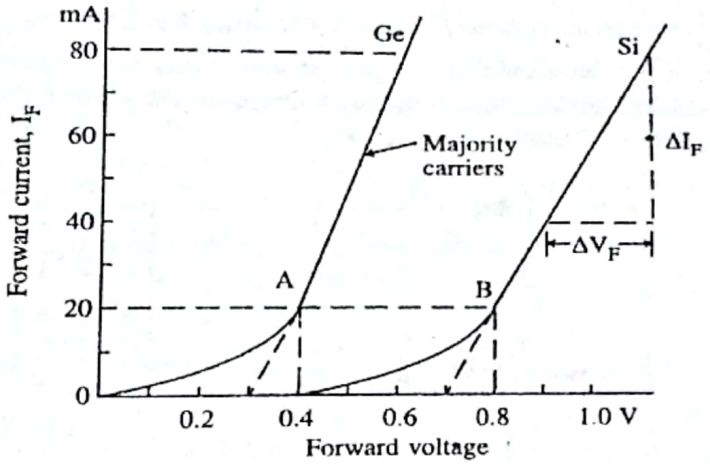


Fig. 13.6

In practice, this static forward resistance is not used. Instead, the **dynamic resistance** or **incremental** resistance or **ac resistance** of the junction is used. It is given by the reciprocal of the slope of the forward characteristic.

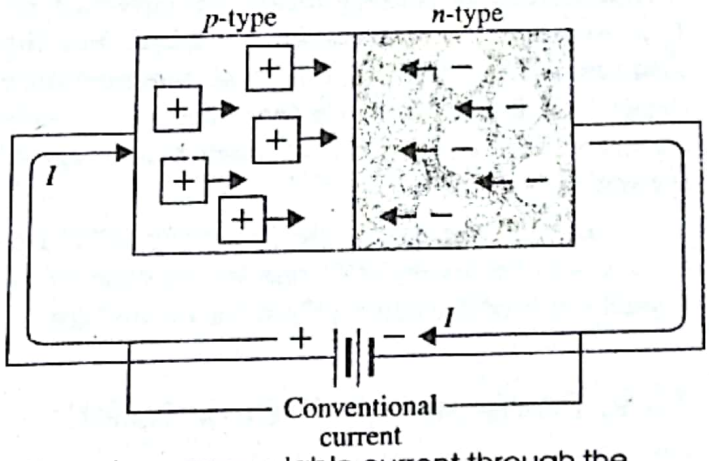
$$r_{ac} = \frac{1}{\Delta I_F / \Delta V_F} = \frac{\Delta V_F}{\Delta I_F}$$

Here, $\Delta V_F = 0.19\ V$ and $\Delta I_F = 37.6$ mA

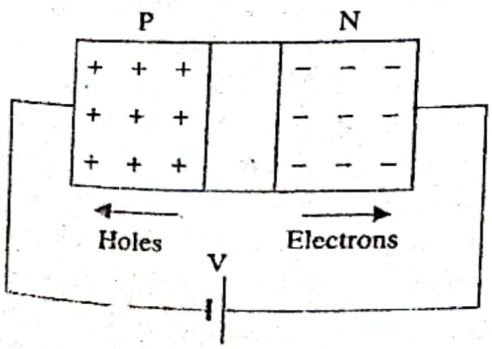
$$\therefore \quad r_{ac} = \frac{0.19}{3.76 \times 10^{-3}} \cong 5\ \Omega$$

13.7. Reverse Biased P-N Junction

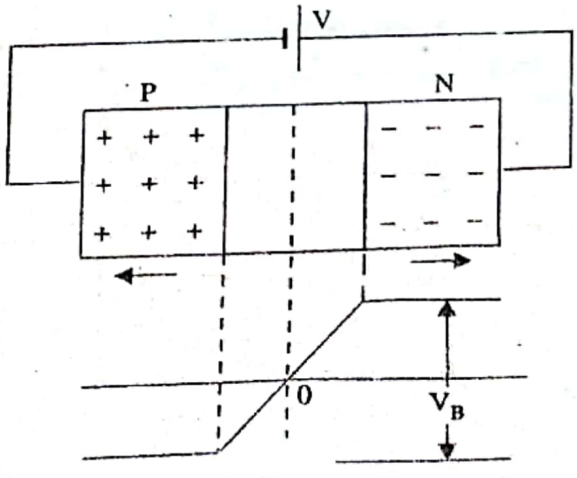
When battery connections to the semiconductor are made as shown in Fig. 13.7 (*a*), the junction is said to be *reverse-biased.* In this case, holes are attracted by the negative battery terminal and electrons by the positive terminal so that both holes and electrons move **away** from the junction and **away** from each other. Since there is no electron-hole combination, no current flows and the junction offers high resistance.



There is an appreciable current through the diode when the diode is forward biased.



(*a*)



V_B Increased

(*b*)

Fig. 13.7

Another way of looking at the above process is that, in this case, the applied voltage increases the barrier potential thereby blocking the flow of majority carriers as shown in Fig. 13.7 (*b*).

Incidentally, it may be noted that under reverse bias conditions, width of depletion layer is increased because majority charge carriers are pulled away from the junction. It also increases the potential barrier (Fig. 13.8).

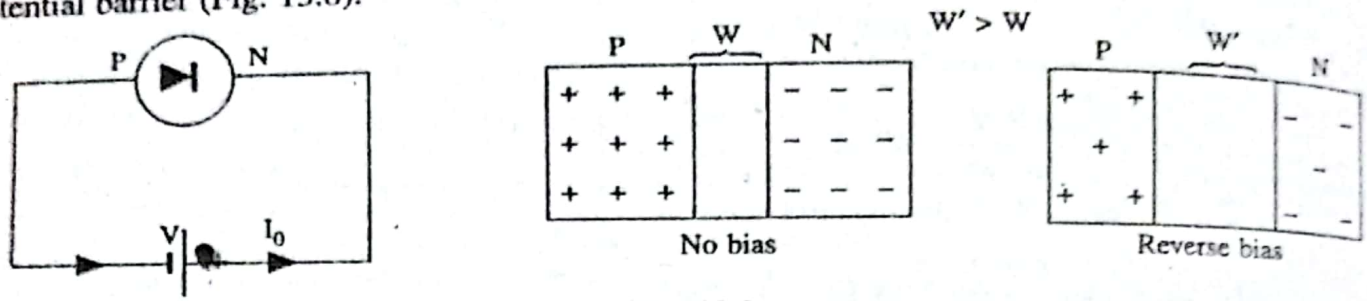
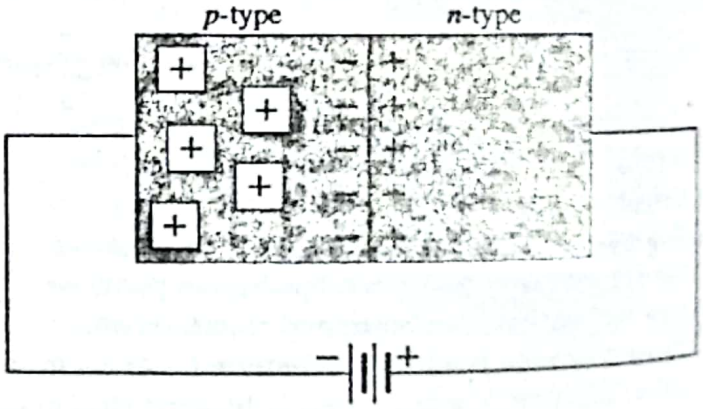


Fig. 13.8

13.8. Reverse Saturation Current (I_s or I_0)

Although under reverse-bias conditions, there is practically no current due to majority carriers, yet there is a small amount of current (a few μA only) due to the flow of minority carriers across the junction. As explained earlier in Art. 12.26, due to thermal energy, there are always generated some holes in the *N*-type region and some electrons in the *P*-type region of the semiconductor as shown in Fig. 12.21. The applied voltage acts as a forward bias for these minority carriers. The battery drives these minority carriers across the junction thereby producing a small current called reverse current or *reverse saturation current* I_s or I_0. Since minority carriers are thermally-generated, I_0 is *extremely temperature dependent.* For the same reason, forward current is also temperature dependent but to a much less degree because minority current forms a very small percentage of the majority current.

I_0 is found to double for every 10°C rise for Ge and for every 6°C rise in the case of Si. Usually, it is of the order of μA for Ge and nA for Si.



Under a reverse bias condition, there is almost no current through the diode.

13.9. Reverse V/I Characteristic

It may be noted that reverse saturation current is also referred to as *leakage current* of the *P-N* junction. Fig. 13.9 shows *V/I* characteristics of a reverse-biased *P-N* junction. It is seen that as reverse voltage is increased from zero, the reverse current quickly rises to its maximum or saturation value. Keeping temperature constant, as the reverse voltage is increased, I_0 is found to increase only slightly. This slight increase is due to the impurities on the surface of the semiconductor which behaves as a resistor and hence obeys Ohm's law. This gives rise to a very small current called *surface leakage*

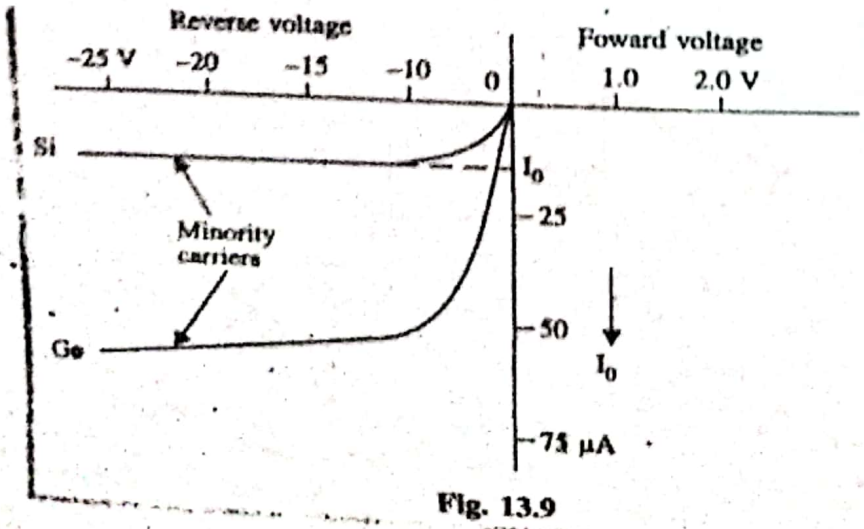


Fig. 13.9

current. Unlike the main leakage (or saturation) current, this surface leakage current is independent of temperature but depends on the magnitude of the reverse voltage.

A reverse-biased junction can be represented by a very large resistance. As seen from Fig. 13.9, in the case of Si, for a reverse voltage of about 15 V, $I_0 = 10\ \mu A$. Hence reverse resistance is

$$R_R = \frac{15\ V}{10\ \mu A} = 1.5\ M$$

13.10. Combined Forward and Reverse V/I Characteristics

Combined forward and reverse voltage-current characteristics for both Ge and Si are shown in Fig. 13.10. It is seen that leakage current of Ge junction is much more than that of Si junction. It is worthwhile to make note of the change in scale of I_0 and reverse voltage.

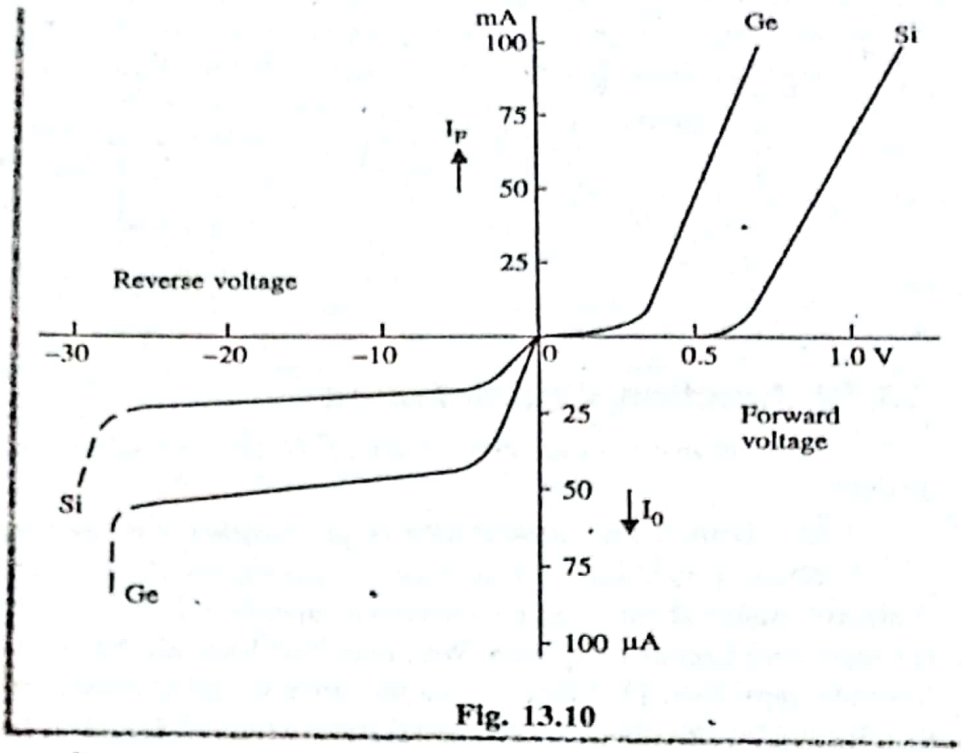


Fig. 13.10

13.11. Junction Breakdown

If the reverse bias applied to a *P-N* junction is increased, a point is reached when the junction breaksdown and reverse current rises sharply to a value limited only by the external resistance connected in series with the junction (Fig 13.10). This critical value of the voltage is known as **breakdown voltage** (V_{BR}). It is found that once breakdown has occurred, very little further increase in voltage is required to increase the current to relatively high values. The junction itself offers almost zero resistance at this point.

The breakdown voltage depends on the width of the depletion region which, in turn, depends on the doping level.

The following two mechanisms are responsible for breakdown under increasing reverse voltage :

1. Zener Breakdown

This form of breakdown occurs in junctions which, being heavily doped, have narrow depletion layers. The breakdown voltage sets up a very strong electric field (about 10^8 V/m) across this narrow layer. This field is strong enough to *break or rupture the covalent bonds* thereby generating electron-hole pairs. Even a small further increase in reverse voltage is capable of producing large number of current carriers. That is why the junction has very low resistance in the breakdown region.

2. Avalanche Breakdown

This form of breakdown occurs in junctions which, being lightly-doped, have wide depletion layers where the electric field is not strong enough to produce Zener breakdown. Instead, the minority carriers (accelerated by this field) collide with the semiconductor atoms in the depletion region. Upon collision with valence electrons, covalent bonds are broken and electron-hole pairs are generated. These newly-generated charge carriers are also accelerated by the electric field resulting in more

collisions and hence further production of charge carriers. This leads to an avalanche (or flood) of charge carriers and, consequently, to a very low reverse resistance. The two breakdown phenomena are shown in Fig. 13.11.

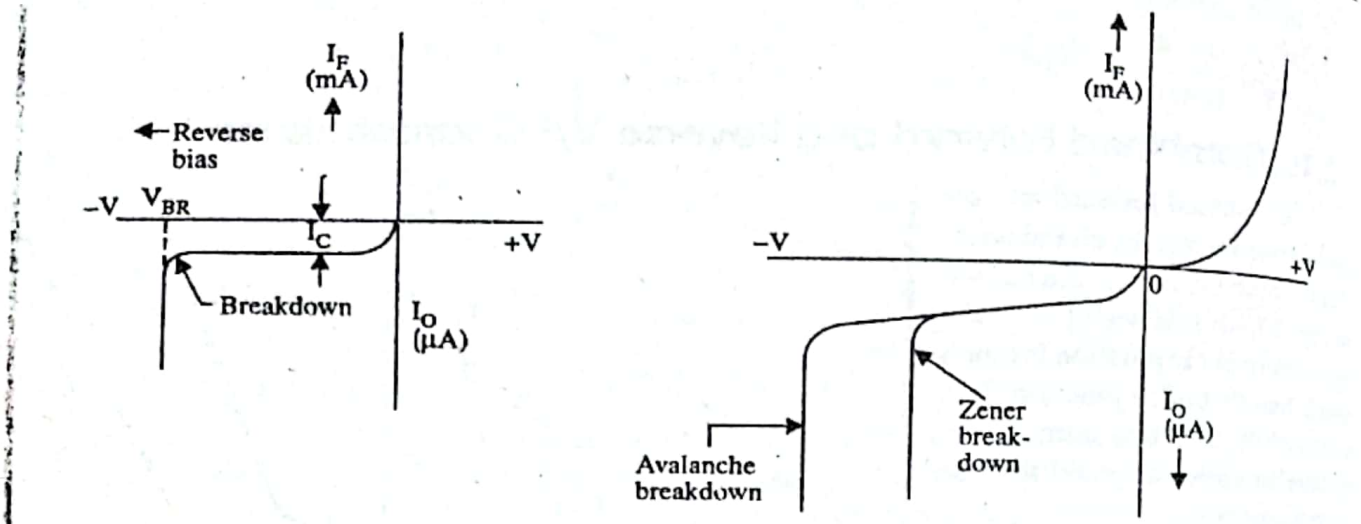


Fig. 13.11

13.12. Junction Capacitance

Capacitive effects are exhibited by *P-N* junctions when they are either forward-biased or reverse-biased.

(a) Transition Capacitance (C_T) or Space-charge Capacitance

When a *P-N* junction is reverse-biased, the depletion region acts like an insulator or as a dielectric material essential for making a capacitor. The *P*- and *N*-type regions on either side have low resistance and act as the plates. We, therefore, have all the components necessary for making a parallel-plate capacitor. This junction capacitance is called *transition* or *space charge* capacitance (C_{pn} or C_T). It may be calculated by the usual formula $C = \varepsilon A/d$. Its typical value is 40 pF. Since thickness of depletion (or transition) layer depends on the amount of reverse bias, capacitance C_T can be controlled with the help of applied bias. This property of variable capacitance possessed by a reverse-biased *P-N* junction is used in the construction of a device known as *varicap* or *varactor* (Art. 15.8).

This capacitance is voltage-dependent as given by the relation

$$C_T = \frac{K}{(V_K + V_R)^n}$$

where V_K = knee voltage (Art. 13.6)

V_R = applied reverse voltage

K = constant depending on semiconductor material.

$n = \frac{1}{2}$ — for alloy junction

$= \frac{1}{3}$ — for diffused junction

(b) Diffusion or Storage Capacitance (C_D)

This capacitive effect is present when the junction is *forward-biased*. It is called diffusion capacitance to account for the time delay in moving charges across the junction by diffusion process. Due to this fact, this capacitance cannot be identified in terms of a dielectric and plates. It varies directly with the magnitude of forward current as explained below in more details.

Consider a forward-biased junction which is carrying a forward current I_F. Suppose the applied voltage is suddenly reversed, then I_F ceases suddenly but leaves lot of majority charge carriers in the depletion region. These charge carriers must get out of the region which to their bad luck, becomes wider under the reverse bias. Hence, it is seen that when a forward-biased *P-N* junction is suddenly reverse biased, a reverse current flows which is large initially but gradually decreases to the level of saturation current I_0. This effect can be likened to the discharging current of a capacitor and is, therefore, rightly represented by a capacitance called *diffusion capacitance* C_D. Since the number of charge carriers left in depletion layer is proportional to forward current, C_D is directly proportional to I_F. Its typical value is 0.02 μF which is 5000 time C_T.

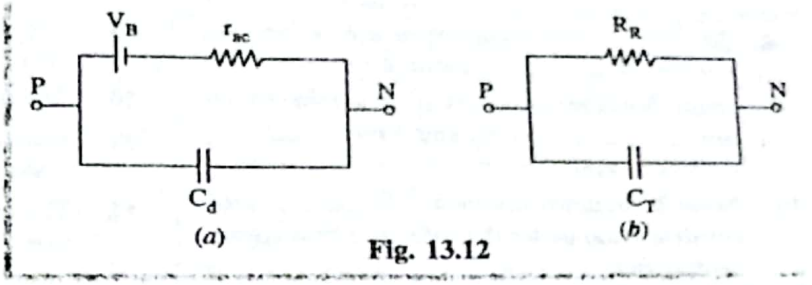


Fig. 13.12

This capacitance assumes great significance in the operation of devices which are required to switch rapidly from forward to reverse bias. If C_D is large, this switchover cannot be rapid. It will delay both the switch-on and the switch-off. This effect of C_D is variously known as *recovery time* or carrier storage.

13.13. Equivalent Circuit of a P-N Junction

We have seen from above that a forward-biased junction offers ac resistance r_{ac} and possesses diffusion capacitance C_D (which comes into the picture only when frequency of the applied voltage is very high). Hence, it can be represented by the equivalent circuit of Fig. 13.12 (*a*). An opposing battery has been connected in series with r_{ac} to account for the junction barrier potential (Art. 13.3).

As seen from Fig. 13.12 (*b*), a reverse-biased junction can simply represented by a reverse resistance R_R connected in *parallel* with a capacitance C_T or C_{pn}.

Example 13.1. *Calculate the barrier potential for Si junction at (a) 100°C and (b) 0°C if its value at 25°C is 0.7 V.*

Solution. As seen from Art. 13.4,

$$\Delta V = -0.002.\Delta t \simeq -0.002\,(t_2 - t_1)$$

(*a*) $\Delta t = (100 - 25) = 75°C$

$\therefore$ $\Delta V = -0.002 \times 75 = -0.15$ V

$\therefore$ V_B at 100°C $= 0.7 + (-0.15) = \mathbf{0.55V}$

(*b*) $\Delta t = (0 - 25) = -25°C$

$\therefore$ $\Delta V = -0.002 \times (-25) = 0.05$

$\therefore$ V_B at 0° C $= 0.7 + 0.05 = \mathbf{0.75}$ V.

SELF EXAMINATION QUESTIONS

A. Fill in the blanks with most appropriate word (s) or numerical value (s).

1. Depletion region exists on ..... sides of a *P-N* junction.
2. A ..... potential is developed across a *P-N* junction whose value for silicon is ..... volt.
3. As soon as a *P-N* junction is formed, ... charge carriers from both sides cross-over the junction.
4. The width of the depletion layer in an unbiased *P-N* junction depends on ..... level.
5. Barrier potential ..... with increase in junction temperature.
6. When a junction is forward-biased for majority carriers, it is ..... -biased for ..... carriers.
7. The forward-biased *P-N* junction has ..... forward resistance but ..... reverse resistance.