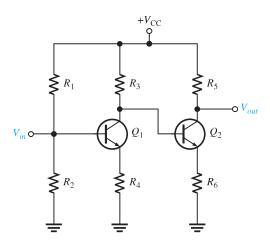
# **Direct-Coupled Multistage Amplifiers**

A basic two-stage, direct-coupled amplifier is shown in Figure 6–36. Notice that there are no coupling or bypass capacitors in this circuit. The dc collector voltage of the first stage provides the base-bias voltage for the second stage. Because of the direct coupling, this type of amplifier has a better low-frequency response than the capacitively coupled type in which the reactance of coupling and bypass capacitors at very low frequencies may become excessive. The increased reactance of capacitors at lower frequencies produces gain reduction in capacitively coupled amplifiers.

Direct-coupled amplifiers can be used to amplify low frequencies all the way down to dc (0 Hz) without loss of voltage gain because there are no capacitive reactances in the circuit. The disadvantage of direct-coupled amplifiers, on the other hand, is that small changes in the dc bias voltages from temperature effects or power-supply variation are amplified by the succeeding stages, which can result in a significant drift in the dc levels throughout the circuit.

#### ► FIGURE 6–36

A basic two-stage direct-coupled amplifier.



SECTION 6-6 CHECKUP

- 1. What does the term stage mean?
- 2. How is the overall voltage gain of a multistage amplifier determined?
- 3. Express a voltage gain of 500 in dB.
- 4. Discuss a disadvantage of a capacitively coupled amplifier.

# 6-7 THE DIFFERENTIAL AMPLIFIER

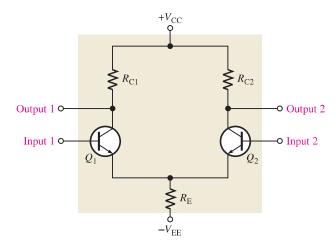
A **differential amplifier** is an amplifier that produces outputs that are a function of the difference between two input voltages. The differential amplifier has two basic modes of operation: differential (in which the two inputs are different) and common mode (in which the two inputs are the same). The differential amplifier is important in operational amplifiers, which are covered beginning in Chapter 12.

After completing this section, you should be able to

- Describe the differential amplifier and its operation
- Discuss the basic operation
  - Calculate dc currents and voltages
- Discuss the modes of signal operation
  - Describe single-ended differential input operation
     Describe double-ended differential input operation
     Determine common-mode operation
- □ Define and determine the common-mode rejection ratio (CMRR)

# **Basic Operation**

A basic differential amplifier (diff-amp) circuit is shown in Figure 6–37. Notice that the differential amplifier has two inputs and two outputs.



#### ▼ FIGURE 6-37

Basic differential amplifier.

The following discussion is in relation to Figure 6–38 and consists of a basic dc analysis of the diff-amp's operation. First, when both inputs are grounded (0 V), the emitters are at -0.7 V, as indicated in Figure 6–38(a). It is assumed that the transistors are identically matched by careful process control during manufacturing so that their dc emitter currents are the same when there is no input signal. Thus,

$$I_{\rm E1} = I_{\rm E2}$$

Since both emitter currents combine through  $R_{\rm E}$ ,

$$I_{\rm E1}=I_{\rm E2}=\frac{I_{R_{\rm E}}}{2}$$

where

$$I_{R_{\rm E}} = \frac{V_{\rm E} - V_{\rm EE}}{R_{\rm E}}$$

Based on the approximation that  $I_{\rm C} \cong I_{\rm E}$ ,

$$I_{\rm C1} = I_{\rm C2} \cong \frac{I_{R_{\rm E}}}{2}$$

Since both collector currents and both collector resistors are equal (when the input voltage is zero),

$$V_{\rm C1} = V_{\rm C2} = V_{\rm CC} - I_{\rm C1} R_{\rm C1}$$

This condition is illustrated in Figure 6–38(a).

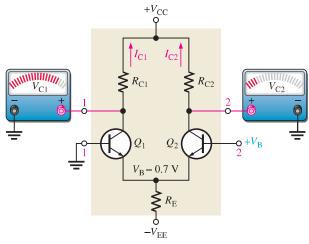
Next, input 2 is left grounded, and a positive bias voltage is applied to input 1, as shown in Figure 6–38(b). The positive voltage on the base of  $Q_1$  increases  $I_{C1}$  and raises the emitter voltage to

$$V_{\rm E} = V_{\rm B} - 0.7 \,\mathrm{V}$$

This action reduces the forward bias  $(V_{\rm BE})$  of  $Q_2$  because its base is held at 0 V (ground), thus causing  $I_{\rm C2}$  to decrease. The net result is that the increase in  $I_{\rm C1}$  causes a decrease in  $V_{\rm C1}$ , and the decrease in  $I_{\rm C2}$  causes an increase in  $V_{\rm C2}$ , as shown.

(a) Both inputs grounded

(b) Bias voltage on input 1 with input 2 grounded



(c) Bias voltage on input 2 with input 1 grounded

#### ▲ FIGURE 6-38

Basic operation of a differential amplifier (ground is zero volts) showing relative changes in voltages.

Finally, input 1 is grounded and a positive bias voltage is applied to input 2, as shown in Figure 6–38(c). The positive bias voltage causes  $Q_2$  to conduct more, thus increasing  $I_{C2}$ . Also, the emitter voltage is raised. This reduces the forward bias of  $Q_1$ , since its base is held at ground, and causes  $I_{C1}$  to decrease. The result is that the increase in  $I_{C2}$  produces a decrease in  $V_{C2}$ , and the decrease in  $I_{C1}$  causes  $V_{C1}$  to increase, as shown.

# **Modes of Signal Operation**

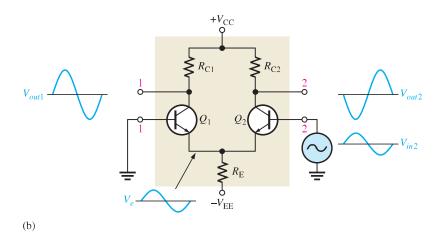
**Single-Ended Differential Input** When a diff-amp is operated with this input configuration, one input is grounded and the signal voltage is applied only to the other input, as shown in Figure 6–39. In the case where the signal voltage is applied to input 1 as in part (a), an inverted, amplified signal voltage appears at output 1 as shown. Also, a signal voltage appears in phase at the emitter of  $Q_1$ . Since the emitters of  $Q_1$  and  $Q_2$  are common, the emitter signal becomes an input to  $Q_2$ , which functions as a common-base amplifier. The signal is amplified by  $Q_2$  and appears, noninverted, at output 2. This action is illustrated in part (a).

In the case where the signal is applied to input 2 with input 1 grounded, as in Figure 6–39(b), an inverted, amplified signal voltage appears at output 2. In this situation,  $Q_1$  acts as a common-base amplifier, and a noninverted, amplified signal appears at output 1.

# $V_{out1}$ $V_{out1}$ $V_{out1}$ $V_{out2}$ $V_{out2}$

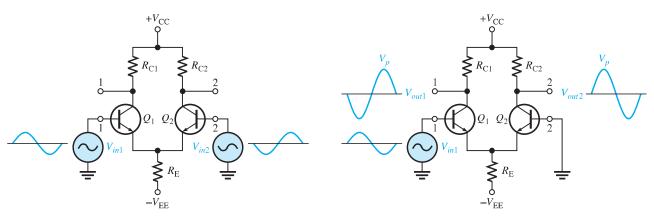
### **◄ FIGURE 6-39**

Single-ended differential input operation.



**Double-Ended Differential Inputs** In this input configuration, two opposite-polarity (out-of-phase) signals are applied to the inputs, as shown in Figure 6–40(a). Each input affects the outputs, as you will see in the following discussion.

Figure 6-40(b) shows the output signals due to the signal on input 1 acting alone as a single-ended input. Figure 6-40(c) on page 308 shows the output signals due to the signal on input 2 acting alone as a single-ended input. Notice in parts (b) and (c) that the signals on output 1 are of the same polarity. The same is also true for output 2. By superimposing both output 1 signals and both output 2 signals, you get the total output signals, as shown in Figure 6-40(d).



(a) Differential inputs (180° out of phase)

(a)

(b) Outputs due to  $V_{in1}$ 

# ▲ FIGURE 6-40

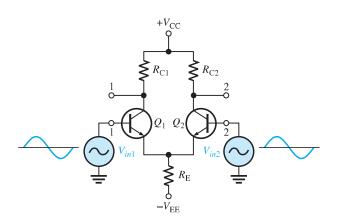
(c) Outputs due to  $V_{in2}$ 

(d) Total outputs

### ▲ FIGURE 6-40

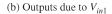
(continued)

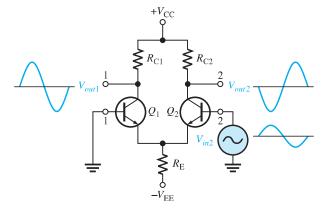
**Common-Mode Inputs** One of the most important aspects of the operation of a diffamp can be seen by considering the **common-mode** condition where two signal voltages of the same phase, frequency, and amplitude are applied to the two inputs, as shown in Figure 6–41(a). Again, by considering each input signal as acting alone, you can understand the basic operation.

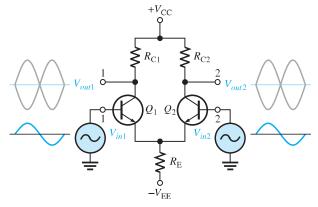


 $= V_{in1}$   $= V_{in1}$   $= V_{EE}$ 

(a) Common-mode inputs (in phase)







(c) Outputs due to  $V_{in2}$ 

(d) Outputs due to  $V_{in1}$  and  $V_{in2}$  cancel because they are equal in amplitude but opposite in phase. The resulting outputs are  $0~\rm V$  ac.

# ▲ FIGURE 6-41

Figure 6–41(b) shows the output signals due to the signal on only input 1, and Figure 6–41(c) shows the output signals due to the signal on only input 2. Notice that the corresponding signals on output 1 are of the opposite polarity, and so are the ones on output 2. When the input signals are applied to both inputs, the outputs are superimposed and they cancel, resulting in a zero output voltage, as shown in Figure 6-41(d).

This action is called *common-mode rejection*. Its importance lies in the situation where an unwanted signal appears commonly on both diff-amp inputs. Common-mode rejection means that this unwanted signal will not appear on the outputs and distort the desired signal. Common-mode signals (noise) generally are the result of the pick-up of radiated energy on the input lines from adjacent lines, the 60 Hz power line, or other sources.

# **Common-Mode Rejection Ratio**

Desired signals appear on only one input or with opposite polarities on both input lines. These desired signals are amplified and appear on the outputs as previously discussed. Unwanted signals (noise) appearing with the same polarity on both input lines are essentially cancelled by the diff-amp and do not appear on the outputs. The measure of an amplifier's ability to reject common-mode signals is a parameter called the **CMRR** (common-mode rejection ratio).

Ideally, a diff-amp provides a very high gain for desired signals (single-ended or differential) and zero gain for common-mode signals. Practical diff-amps, however, do exhibit a very small common-mode gain (usually much less than 1), while providing a high differential voltage gain (usually several thousand). The higher the differential gain with respect to the common-mode gain, the better the performance of the diff-amp in terms of rejection of common-mode signals. This suggests that a good measure of the diff-amp's performance in rejecting unwanted common-mode signals is the ratio of the differential voltage gain  $A_{v(d)}$  to the common-mode gain,  $A_{cm}$ . This ratio is the common-mode rejection ratio, CMRR.

$$CMRR = \frac{A_{v(d)}}{A_{cm}}$$

Equation 6–25

The higher the CMRR, the better. A very high value of CMRR means that the differential gain  $A_{v(d)}$  is high and the common-mode gain  $A_{cm}$  is low.

The CMRR is often expressed in decibels (dB) as

$$CMRR = 20 \log \left( \frac{A_{v(d)}}{A_{cm}} \right)$$

**Equation 6–26** 

### **EXAMPLE 6-13**

A certain diff-amp has a differential voltage gain of 2000 and a common-mode gain of 0.2. Determine the CMRR and express it in decibels.

**Solution**  $A_{\nu(d)} = 2000$ , and  $A_{cm} = 0.2$ . Therefore,

CMRR = 
$$\frac{A_{v(d)}}{A_{cm}} = \frac{2000}{0.2} = 10,000$$

Expressed in decibels,

$$CMRR = 20 \log (10,000) = 80 dB$$

**Related Problem** 

Determine the CMRR and express it in decibels for an amplifier with a differential voltage gain of 8500 and a common-mode gain of 0.25.

A CMRR of 10,000 means that the desired input signal (differential) is amplified 10,000 times more than the unwanted noise (common-mode). For example, if the amplitudes of the differential input signal and the common-mode noise are equal, the desired signal will appear on the output 10,000 times greater in amplitude than the noise. Thus, the noise or interference has been essentially eliminated.

SECTION 6–7 CHECKUP

- 1. Distinguish between double-ended and single-ended differential inputs.
- 2. Define common-mode rejection.
- 3. For a given value of differential gain, does a higher CMRR result in a higher or lower common-mode gain?

# 6-8 Troubleshooting



In working with any circuit, you must first know how it is supposed to work before you can troubleshoot it for a failure. The two-stage capacitively coupled amplifier discussed in Section 6–6 is used to illustrate a typical troubleshooting procedure.

After completing this section, you should be able to

- Troubleshoot amplifier circuits
- Discuss a troubleshooting procedure
  - Describe the analysis phase Describe the planning phase Describe the measurement phase



Chapter 18: Basic Programming Concepts for Automated Testing
Selected sections from Chapter 18 may be introduced as part of this troubleshooting
coverage or, optionally, the entire Chapter 18 may be covered later or not at all.

When you are faced with having to troubleshoot a circuit, the first thing you need is a schematic with the proper dc and signal voltages labeled. You must know what the correct voltages in the circuit should be before you can identify an incorrect voltage. Schematics of some circuits are available with voltages indicated at certain points. If this is not the case, you must use your knowledge of the circuit operation to determine the correct voltages. Figure 6–42 is the schematic for the two-stage amplifier that was analyzed in Section 6–6. The correct voltages are indicated at each point.

# **Troubleshooting Procedure**

The analysis, planning, and measurement approach to troubleshooting, discussed in Chapter 2, will be used.

**Analysis** It has been found that there is no output voltage,  $V_{out}$ . You have also determined that the circuit did work properly and then failed. A visual check of the circuit board or assembly for obvious problems such as broken or poor connections, solder splashes,

311

#### ► FIGURE 6-42

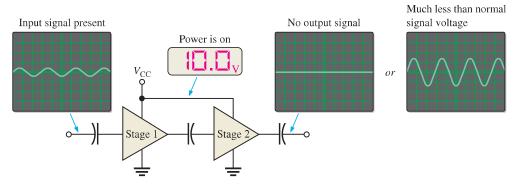
A two-stage common-emitter amplifier with correct voltages indicated. Both transistors have dc and ac betas of 150. Different values of  $\beta$  will produce slightly different results.

wire clippings, or burned components turns up nothing. You conclude that the problem is most likely a faulty component in the amplifier circuit or an open connection. Also, the dc supply voltage may not be correct or may be missing.

**Planning** You decide to use an oscilloscope to check the dc levels and the ac signals (you prefer to use a DMM to measure the dc voltages) at certain test points. Also, you decide to apply the half-splitting method to trace the voltages in the circuit and use an in-circuit transistor tester if a transistor is suspected of being faulty.

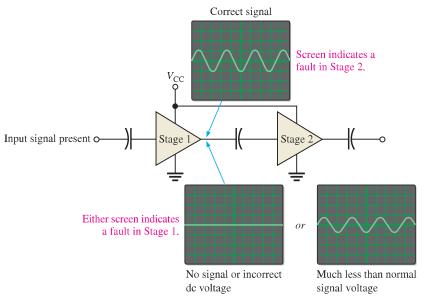
**Measurement** To determine the faulty component in a multistage amplifier, use the general five-step troubleshooting procedure which is illustrated as follows.

- **Step 1:** *Perform a power check.* Assume the dc supply voltage is correct as indicated in Figure 6–43.
- **Step 2:** Check the input and output voltages. Assume the measurements indicate that the input signal voltage is correct. However, there is no output signal voltage or the output signal voltage is much less than it should be, as shown by the diagram in Figure 6–43.



# ▲ FIGURE 6-43

Step 3: Apply the half-splitting method of signal tracing. Check the voltages at the output of the first stage. No signal voltage or a much less than normal signal voltage indicates that the problem is in the first stage. An incorrect dc voltage also indicates a first-stage problem. If the signal voltage and the dc voltage are correct at the output of the first stage, the problem is in the second stage. After this check, you have narrowed the problem to one of the two stages. This step is illustrated in Figure 6–44.



#### ▲ FIGURE 6-44

Half-splitting signal tracing isolates the faulty stage.

**Step 4:** *Apply fault analysis.* Focus on the faulty stage and determine the component failure that can produce the incorrect output.

Symptom: DC voltages incorrect.

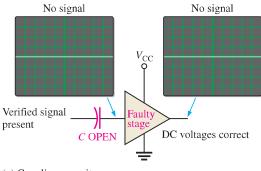
*Likely faults:* A failure of any resistor or the transistor will produce an incorrect dc bias voltage. A leaky bypass or coupling capacitor will also affect the dc bias voltages. Further measurements in the stage are necessary to isolate the faulty component.

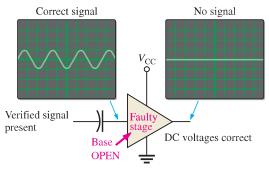
Incorrect ac voltages and the most likely fault(s) are illustrated in Figure 6–45 as follows:

- (a) Symptom 1: Signal voltage at output missing; dc voltage correct. Symptom 2: Signal voltage at base missing; dc voltage correct. Likely fault: Input coupling capacitor open. This prevents the signal from getting to the base.
- (b) *Symptom:* Correct signal at base but no output signal. *Likely fault:* Transistor base open.
- (c) *Symptom:* Signal voltage at output much less than normal; dc voltage correct.

Likely fault: Bypass capacitor open.

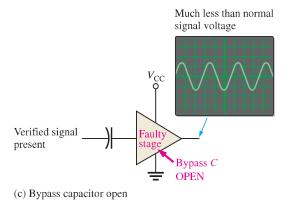
**Step 5:** *Replace or repair.* With the power turned off, replace the defective component or repair the defective connection. Turn on the power, and check for proper operation.





(a) Coupling capacitor open

(b) Transistor base open



#### ▲ FIGURE 6-45

Troubleshooting a faulty stage.

# **EXAMPLE 6-14**

The two-stage amplifier in Figure 6–42 has malfunctioned. Specify the step-by-step troubleshooting procedure for an assumed fault.

Solution

Assume there are no visual or other indications of a problem such as a charred resistor, solder splash, wire clipping, broken connection, or extremely hot component. The troubleshooting procedure for a certain fault scenario is as follows:

- **Step 1:** There is power to the circuit as indicated by a correct  $V_{CC}$  measurement.
- Step 2: There is a verified input signal voltage, but no output signal voltage is measured.
- Step 3: The signal voltage and the dc voltage at the collector of  $Q_1$  are correct. This means that the problem is in the second stage or the coupling capacitor  $C_3$  between the stages.
- Step 4: The correct signal voltage and dc bias voltage are measured at the base of  $Q_2$ . This eliminates the possibility of a fault in  $C_3$  or the second stage bias circuit.

The collector of  $Q_2$  is at 10 V and there is no signal voltage. This measurement, made directly on the transistor collector, indicates that either the collector is shorted to  $V_{CC}$  or the transistor is internally open. It is unlikely that the collector resistor  $R_7$  is shorted but to verify, turn off the power and use an ohmmeter to check.

The possibility of a short is eliminated by the ohmmeter check. The other possible faults are (a) transistor  $Q_2$  internally open or (b) emitter resistor or

connection open. Use a transistor tester and/or ohmmeter to check each of these possible faults with power off.

**Step 5:** Replace the faulty component or repair open connection and retest the circuit for proper operation.

Related Problem

Determine the possible fault(s) if, in Step 4, you find no signal voltage at the base of  $Q_2$  but the dc voltage is correct.



# **Multisim Troubleshooting Exercises**

These file circuits are in the Troubleshooting Exercises folder on the companion website. Open each file and determine if the circuit is working properly. If it is not working properly, determine the fault.

- 1. Multisim file TSE06-01
- 2. Multisim file TSE06-02
- 3. Multisim file TSE06-03
- 4. Multisim file TSE06-04
- 5. Multisim file TSE06-05

SECTION 6-8 CHECKUP

- 1. If  $C_4$  in Figure 6–42 were open, how would the output signal be affected? How would the dc level at the collector of  $Q_2$  be affected?
- 2. If  $R_5$  in Figure 6–42 were open, how would the output signal be affected?
- 3. If the coupling capacitor  $C_3$  in Figure 6–42 shorted out, would any of the dc voltages in the amplifier be changed? If so, which ones?

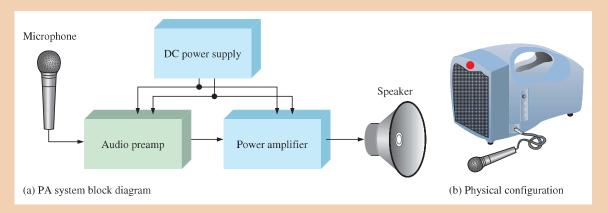


# Application Activity: Audio Preamplifier for PA System

An audio preamplifier is to be developed for use in a small portable public address (PA) system. The preamplifier will have a microphone input, and its output will drive a power amplifier to be developed in Chapter 7. A block diagram of the complete PA system is shown in Figure 6–46(a), and its physical configuration is shown in part (b). The dc supply voltages are provided by a battery pack or by an electronic power supply.

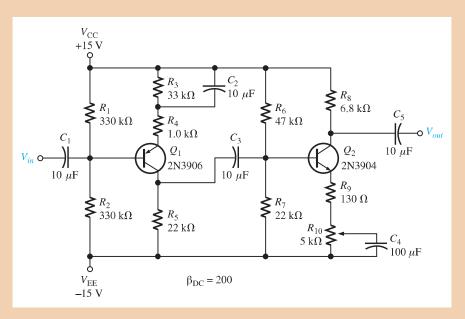
# The Circuit

A 2-stage audio voltage preamplifier is shown in Figure 6–47. The first stage is a common-emitter *pnp* with voltage-divider bias, and the second stage is a common-emitter *npn* with voltage-divider bias. It has been decided that the amplifier should operate from 30 V dc to get a large enough signal voltage swing to provide a maximum of 6 W to the speaker. Because small IC regulators such as the 78xx and 79xx series are not available above 24 V,



#### ▲ FIGURE 6-46

The public address system.



### ▲ FIGURE 6-47

Two-stage voltage preamplifier.

dual  $\pm 15$  V dc supplies are used in this particular system instead of a single supply. The operation is essentially the same as if a single  $\pm 30$  V dc source had been used. The potentiometer at the output provides gain adjustment for volume control. The input to the first stage is from the microphone, and the output of the second stage will drive a power amplifier to be developed in Chapter 7. The power amplifier will drive the speaker. The preamp is to operate with a peak input signal range of from 25 mV to 50 mV. The minimum range of voltage gain adjustment is from 90 to 170.

- 1. Calculate the theoretical voltage gain of the first stage when the second stage is set for maximum gain.
- 2. Calculate the theoretical maximum voltage gain of the second stage.
- 3. Determine the overall theoretical voltage gain.
- 4. Calculate the circuit power dissipation with no signal (quiescent).