5 Transistor Bias Circuits

CHAPTER OUTLINE

CHAPTER OBJECTIVES

- Discuss and determine the dc operating point of a linear amplifier
- Analyze a voltage-divider biased circuit
- Analyze an emitter bias circuit, a base bias circuit, an emitter-feedback bias circuit, and a collector-feedback bias circuit
- Troubleshoot faults in transistor bias circuits

KEY TERMS

- Q-point
- DC load line
- Linear region
- Stiff voltage divider
- Feedback

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Study aids and Multisim files for this chapter are available at http://www.pearsonhighered.com/electronics

INTRODUCTION

As you learned in Chapter 4, a transistor must be properly biased in order to operate as an amplifier. DC biasing is used to establish fixed dc values for the transistor currents and voltages called the *dc operating point* or *quiescent point* (*Q-point*). In this chapter, several types of bias circuits are discussed. This material lays the groundwork for the study of amplifiers, and other circuits that require proper biasing.

APPLICATION ACTIVITY PREVIEW

The Application Activity focuses on a system for controlling temperature in an industrial chemical process. You will be dealing with a circuit that converts a temperature measurement to a proportional voltage that is used to adjust the temperature of a liquid in a storage tank. The first step is to learn all you can about transistor operation. You will then apply your knowledge to the Application Activity at the end of the chapter.

5–1 THE DC OPERATING POINT

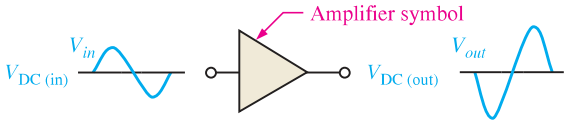
A transistor must be properly biased with a dc voltage in order to operate as a linear amplifier. A dc operating point must be set so that signal variations at the input terminal are amplified and accurately reproduced at the output terminal. As you learned in Chapter 4, when you bias a transistor, you establish the dc voltage and current values. This means, for example, that at the dc operating point, I_C and V_{CE} have specified values. The dc operating point is often referred to as the Q-point (quiescent point).

After completing this section, you should be able to

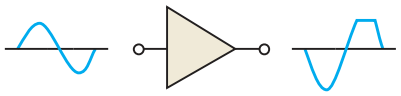
- **Discuss and determine the dc operating point of a linear amplifier**
- Explain the purpose of dc bias
  - Define *Q-point* and describe how it affects the output of an amplifier
  - Explain how collector characteristic curves are produced ◆ Describe and draw a dc load line ◆ State the conditions for linear operation ◆ Explain what causes waveform distortion

DC Bias

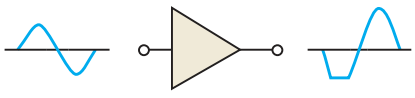
Bias establishes the dc operating point (**Q-point**) for proper linear operation of an amplifier. If an amplifier is not biased with correct dc voltages on the input and output, it can go into saturation or cutoff when an input signal is applied. Figure 5–1 shows the effects of proper and improper dc biasing of an inverting amplifier. In part (a), the output signal is an amplified replica of the input signal except that it is inverted, which means that it is 180° out of phase with the input. The output signal swings equally above and below the dc bias level of the output, $V_{DC(out)}$. Improper biasing can cause distortion in the output signal, as illustrated in parts (b) and (c). Part (b) illustrates limiting of the positive portion of the output voltage as a result of a Q-point (dc operating point) being too close to cutoff. Part (c) shows limiting of the negative portion of the output voltage as a result of a dc operating point being too close to saturation.



(a) Linear operation: larger output has same shape as input except that it is inverted



(b) Nonlinear operation: output voltage limited (clipped) by cutoff



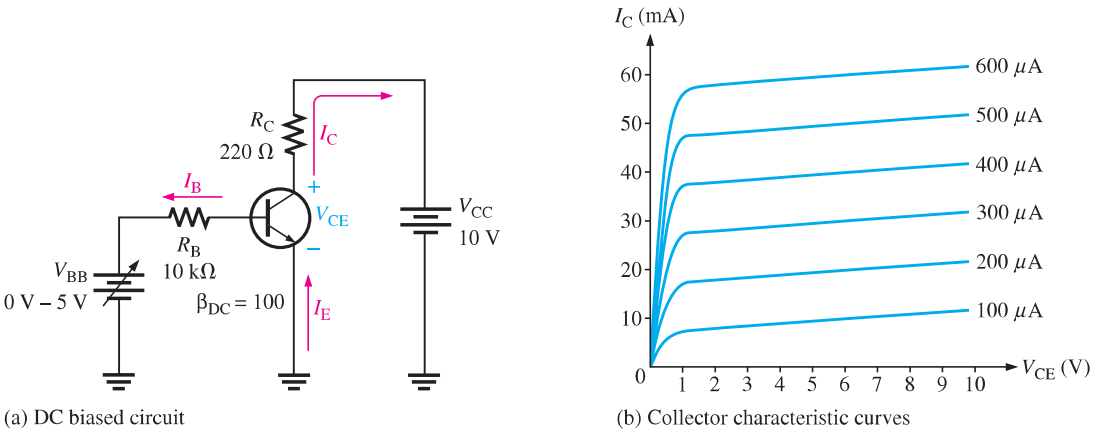
(c) Nonlinear operation: output voltage limited (clipped) by saturation

▲ FIGURE 5–1

Examples of linear and nonlinear operation of an inverting amplifier (the triangle symbol).

Graphical Analysis The transistor in Figure 5–2(a) is biased with V_{CC} and V_{BB} to obtain certain values of I_B, I_C, I_E, and V_{CE}. The collector characteristic curves for this particular

transistor are shown in Figure 5–2(b); we will use these curves to graphically illustrate the effects of dc bias.



▲ FIGURE 5–2

A dc-biased transistor circuit with variable bias voltage (V_{BB}) for generating the collector characteristic curves shown in part (b).

FYI

In 1965, a single transistor cost more than a dollar. By 1975, the cost of a transistor had dropped to less than a penny, while transistor size allowed for almost 100,000 transistors on a single chip. From 1979 to 1999, processor performance went from about 1.5 million instructions per second (MIPS) to over 1,000 MIPS. Today's processors, some topping out at well above one billion transistors, run at 3.2 GHz and higher, deliver over 10,000 MIPS, and can be manufactured in high volumes with transistors that cost less than 1/10,000th of a cent.

In Figure 5–3, we assign three values to I_B and observe what happens to I_C and V_{CE}. First, V_{BB} is adjusted to produce an I_B of 200 μA, as shown in Figure 5–3(a). Since $I_C = \beta_{DC} I_B$, the collector current is 20 mA, as indicated, and

$$V_{CE} = V_{CC} - I_C R_C = 10\text{ V} - (20\text{ mA})(220\ \Omega) = 10\text{ V} - 4.4\text{ V} = 5.6\text{ V}$$

This Q-point is shown on the graph of Figure 5–3(a) as Q_1.

Next, as shown in Figure 5–3(b), V_{BB} is increased to produce an I_B of 300 μA and an I_C of 30 mA.

$$V_{CE} = 10\text{ V} - (30\text{ mA})(220\ \Omega) = 10\text{ V} - 6.6\text{ V} = 3.4\text{ V}$$

The Q-point for this condition is indicated by Q_2 on the graph.

Finally, as in Figure 5–3(c), V_{BB} is increased to give an I_B of 400 μA and an I_C of 40 mA.

$$V_{CE} = 10\text{ V} - (40\text{ mA})(220\ \Omega) = 10\text{ V} - 8.8\text{ V} = 1.2\text{ V}$$

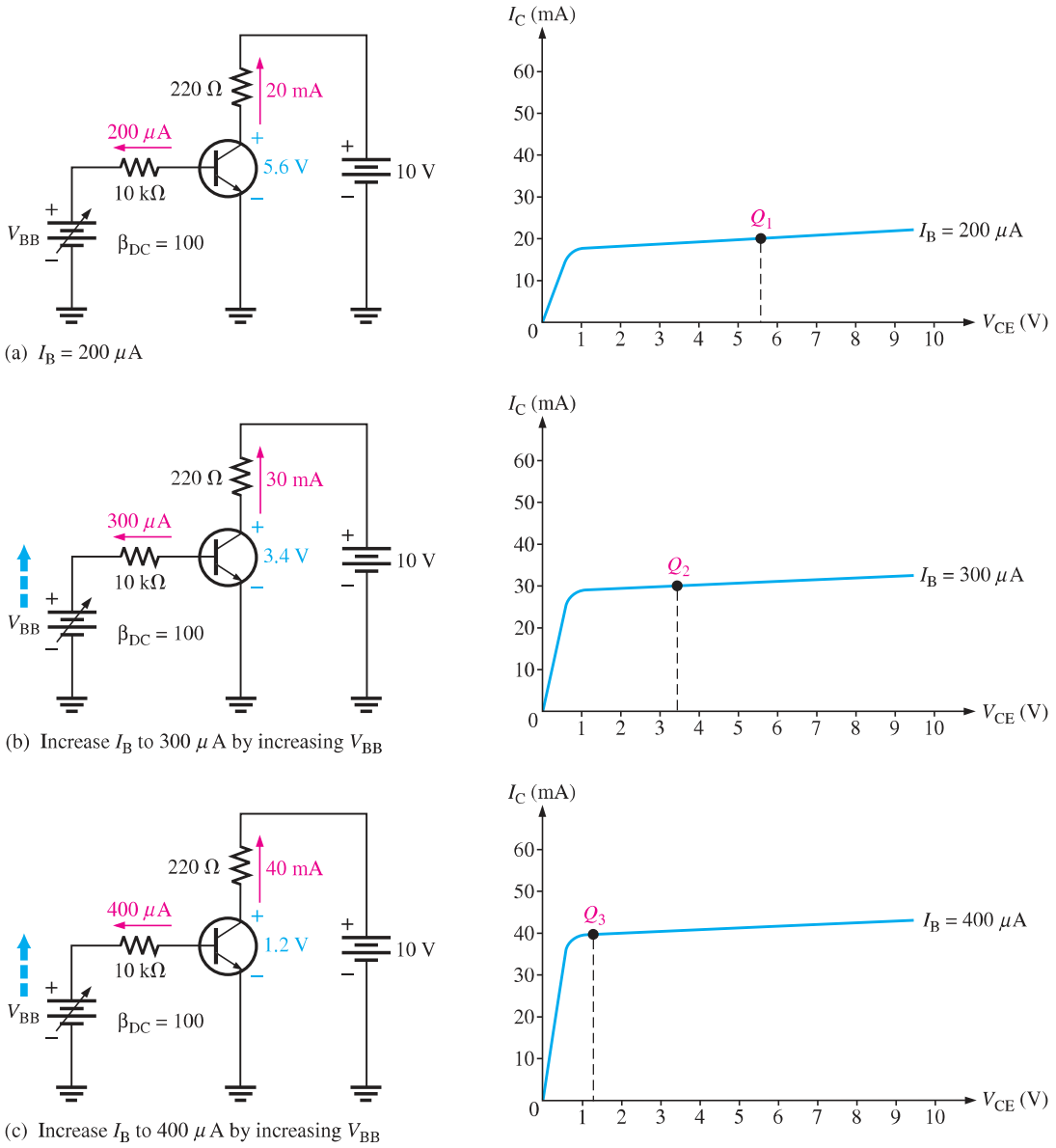
Q_3 is the corresponding Q-point on the graph.

DC Load Line The dc operation of a transistor circuit can be described graphically using a **dc load line**. This is a straight line drawn on the characteristic curves from the saturation value where $I_C = I_{C(sat)}$ on the y-axis to the cutoff value where $V_{CE} = V_{CC}$ on the x-axis, as shown in Figure 5–4(a). The load line is determined by the external circuit (V_{CC} and R_C), not the transistor itself, which is described by the characteristic curves.

In Figure 5–3, the equation for I_C is

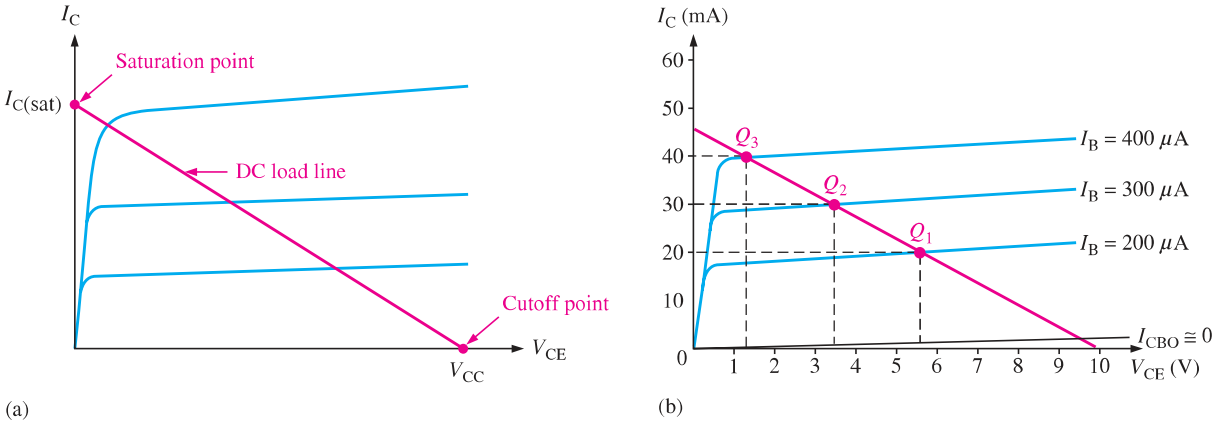
$$I_C = \frac{V_{CC} - V_{CE}}{R_C} = \frac{V_{CC}}{R_C} - \frac{V_{CE}}{R_C} = -\frac{V_{CE}}{R_C} + \frac{V_{CC}}{R_C} = -\left(\frac{1}{R_C}\right)V_{CE} + \frac{V_{CC}}{R_C}$$

This is the equation of a straight line with a slope of $-1/R_C$, an x intercept of $V_{CE} = V_{CC}$, and a y intercept of V_{CC}/R_C, which is $I_{C(sat)}$.



▲ **FIGURE 5–3**

Illustration of Q-point adjustment.



▲ **FIGURE 5–4**

The dc load line.

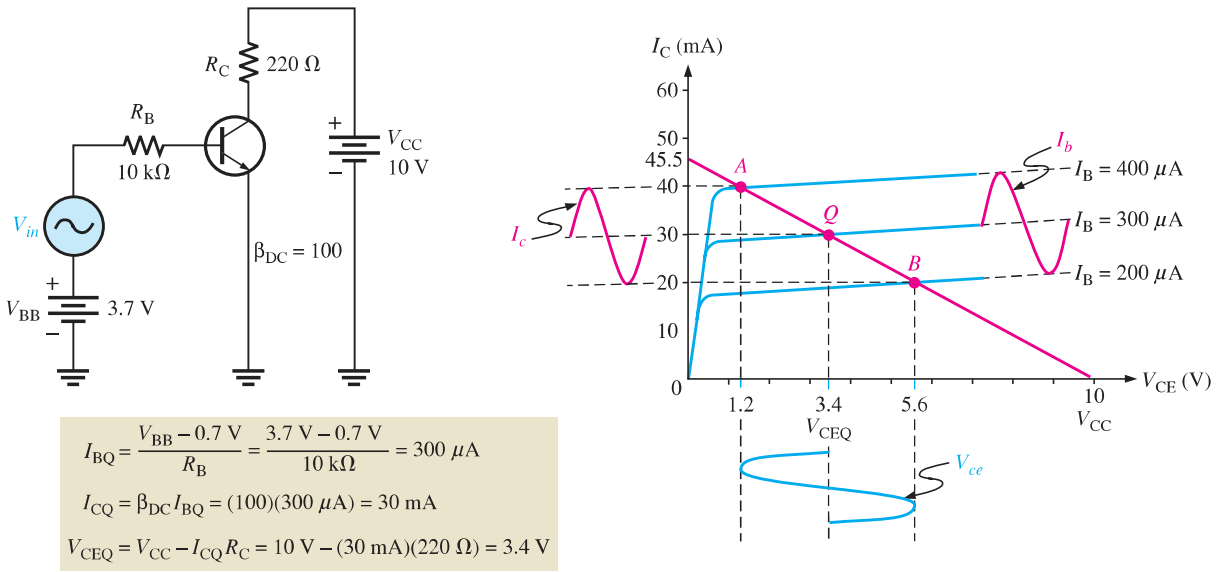
FYI

Gordon Moore, one of the founders of Intel, observed in an article in the April, 1965, issue of *Electronics* magazine that innovations in technology would allow a doubling of the number of transistors in a given space every year (in an update article in 1975, Moore adjusted the rate to every two years to account for the growing complexity of chips), and that the speed of those transistors would increase. This prediction has become widely known as Moore's law.

The point at which the load line intersects a characteristic curve represents the Q-point for that particular value of I_B. Figure 5–4(b) illustrates the Q-point on the load line for each value of I_B in Figure 5–3.

Linear Operation The region along the load line including all points between saturation and cutoff is generally known as the **linear region** of the transistor's operation. As long as the transistor is operated in this region, the output voltage is ideally a linear reproduction of the input.

Figure 5–5 shows an example of the linear operation of a transistor. AC quantities are indicated by lowercase italic subscripts. Assume a sinusoidal voltage, V_{in}, is superimposed on V_{BB}, causing the base current to vary sinusoidally 100 μA above and below its Q-point value of 300 μA. This, in turn, causes the collector current to vary 10 mA above and below its Q-point value of 30 mA. As a result of the variation in collector current, the collector-to-emitter voltage varies 2.2 V above and below its Q-point value of 3.4 V. Point *A* on the load line in Figure 5–5 corresponds to the positive peak of the sinusoidal input voltage. Point *B* corresponds to the negative peak, and point *Q* corresponds to the zero value of the sine wave, as indicated. V_{CEQ}, I_{CQ}, and I_{BQ} are dc Q-point values with no input sinusoidal voltage applied.



$$I_{BQ} = \frac{V_{BB} - 0.7\text{ V}}{R_B} = \frac{3.7\text{ V} - 0.7\text{ V}}{10\text{ k}\Omega} = 300\ \mu\text{A}$$

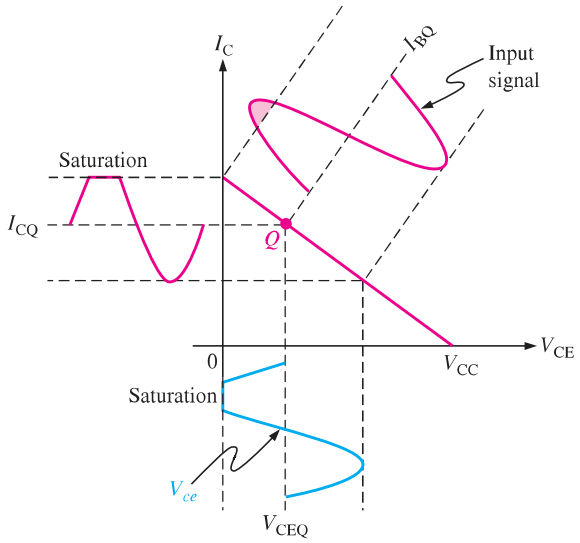
$$I_{CQ} = \beta_{DC} I_{BQ} = (100)(300\ \mu\text{A}) = 30\text{ mA}$$

$$V_{CEQ} = V_{CC} - I_{CQ} R_C = 10\text{ V} - (30\text{ mA})(220\ \Omega) = 3.4\text{ V}$$

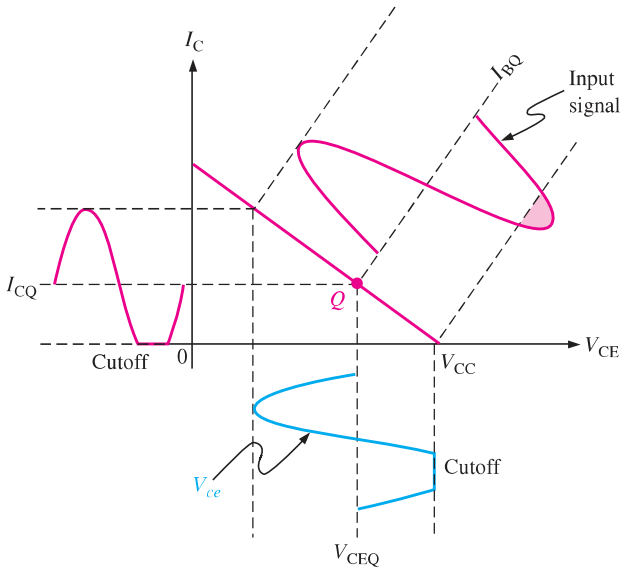
▲ **FIGURE 5–5**

Variations in collector current and collector-to-emitter voltage as a result of a variation in base current.

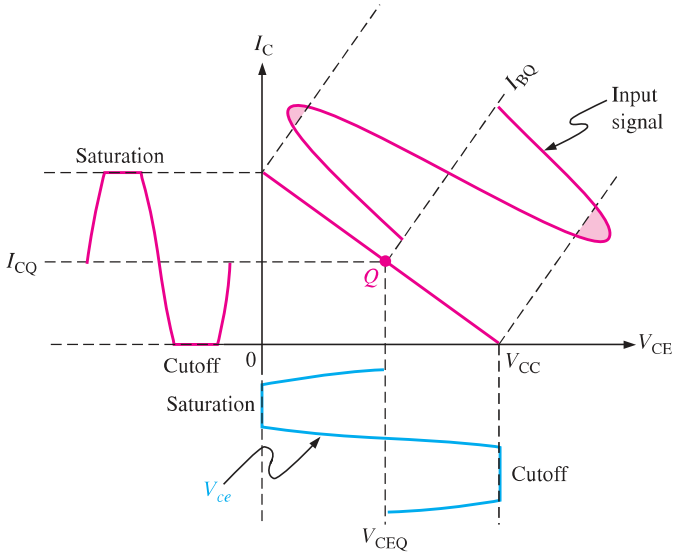
Waveform Distortion As previously mentioned, under certain input signal conditions the location of the Q-point on the load line can cause one peak of the V_{ce} waveform to be limited or clipped, as shown in parts (a) and (b) of Figure 5–6. In each case the input signal is too large for the Q-point location and is driving the transistor into cutoff or saturation during a portion of the input cycle. When both peaks are limited as in Figure 5–6(c), the transistor is being driven into both saturation and cutoff by an excessively large input signal. When only the positive peak is limited, the transistor is being driven into cutoff but not saturation. When only the negative peak is limited, the transistor is being driven into saturation but not cutoff.



(a) Transistor is driven into saturation because the Q-point is too close to saturation for the given input signal.



(b) Transistor is driven into cutoff because the Q-point is too close to cutoff for the given input signal.



(c) Transistor is driven into both saturation and cutoff because the input signal is too large.

▲ **FIGURE 5–6**

Graphical load line illustration of a transistor being driven into saturation and/or cutoff.

EXAMPLE 5–1

Determine the Q-point for the circuit in Figure 5–7 and draw the dc load line. Find the maximum peak value of base current for linear operation. Assume $\beta_{DC} = 200$.

Solution

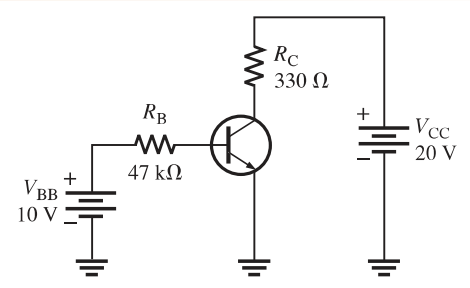
The Q-point is defined by the values of I_C and V_{CE}.

$$I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{10\text{ V} - 0.7\text{ V}}{47\text{ k}\Omega} = 198\ \mu\text{A}$$

$$I_C = \beta_{DC} I_B = (200)(198\ \mu\text{A}) = \mathbf{39.6\ mA}$$

$$V_{CE} = V_{CC} - I_C R_C = 20\text{ V} - 13.07\text{ V} = \mathbf{6.93\ V}$$

▶ FIGURE 5–7



The Q-point is at $I_C = 39.6$ mA and at $V_{CE} = 6.93$ V.

Since $I_{C(cutoff)} = 0$, you need to know $I_{C(sat)}$ to determine how much variation in collector current can occur and still maintain linear operation of the transistor.

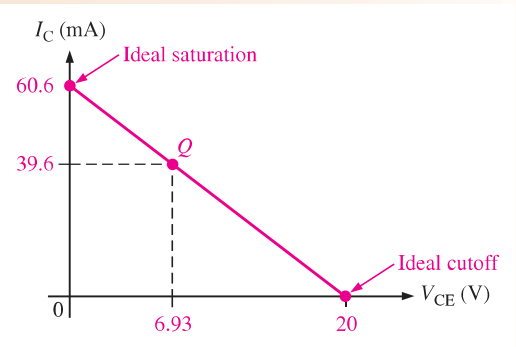
$$I_{C(sat)} = \frac{V_{CC}}{R_C} = \frac{20\text{ V}}{330\ \Omega} = 60.6\text{ mA}$$

The dc load line is graphically illustrated in Figure 5–8, showing that before saturation is reached, I_C can increase an amount ideally equal to

$$I_{C(sat)} - I_{CQ} = 60.6\text{ mA} - 39.6\text{ mA} = 21.0\text{ mA}$$

However, I_C can decrease by 39.6 mA before cutoff ($I_C = 0$) is reached. Therefore, the limiting excursion is 21 mA because the *Q-point is closer to saturation than to cutoff*. The 21 mA is the maximum peak variation of the collector current. Actually, it would be slightly less in practice because $V_{CE(sat)}$ is not quite zero.

▶ FIGURE 5–8



Determine the maximum peak variation of the base current as follows:

$$I_{b(peak)} = \frac{I_{c(peak)}}{\beta_{DC}} = \frac{21\text{ mA}}{200} = \mathbf{105\ \mu A}$$

*Related Problem** Find the Q-point for the circuit in Figure 5–7, and determine the maximum peak value of base current for linear operation for the following circuit values: $\beta_{DC} = 100$, $R_C = 1.0\text{ k}\Omega$, and $V_{CC} = 24$ V.

*Answers can be found at www.pearsonhighered.com/floyd.

Open the Multisim file E05-01 in the Examples folder on the companion website. Measure I_C and V_{CE} and compare with the calculated values.

SECTION 5–1 CHECKUP
Answers can be found at www.pearsonhighered.com/floyd.

1. What are the upper and lower limits on a dc load line in terms of V_{CE} and I_C?
2. Define *Q-point.*
3. At what point on the load line does saturation occur? At what point does cutoff occur?
4. For maximum V_{ce}, where should the Q-point be placed?

5–2 VOLTAGE-DIVIDER BIAS

You will now study a method of biasing a transistor for linear operation using a single-source resistive voltage divider. This is the most widely used biasing method. Four other methods are covered in Section 5–3.

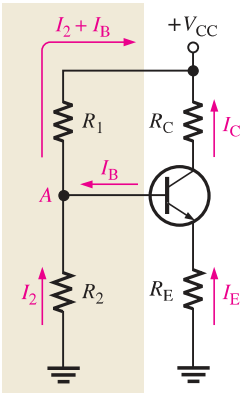
After completing this section, you should be able to

- **Analyze a voltage-divider biased circuit**
  - Define the term *stiff voltage-divider*
  - Calculate currents and voltages in a voltage-divider biased circuit
- Explain the loading effects in voltage-divider bias
  - Describe how dc input resistance at the transistor base affects the bias
- Apply Thevenin's theorem to the analysis of voltage-divider bias
  - Analyze both *npn* and *pnp* circuits

Up to this point a separate dc source, V_{BB}, was used to bias the base-emitter junction because it could be varied independently of V_{CC} and it helped to illustrate transistor operation. A more practical bias method is to use V_{CC} as the single bias source, as shown in Figure 5–9. To simplify the schematic, the battery symbol is omitted and replaced by a line termination circle with a voltage indicator (V_{CC}) as shown.

A dc bias voltage at the base of the transistor can be developed by a resistive voltage-divider that consists of R_1 and R_2, as shown in Figure 5–9. V_{CC} is the dc collector supply voltage. Two current paths are between point A and ground: one through R_2 and the other through the base-emitter junction of the transistor and R_E.

Generally, voltage-divider bias circuits are designed so that the base current is much smaller than the current (I_2) through R_2 in Figure 5–9. In this case, the voltage-divider circuit is very straightforward to analyze because the loading effect of the base current can be ignored. A voltage divider in which the base current is small compared to the current in R_2 is said to be a **stiff voltage divider** because the base voltage is relatively independent of different transistors and temperature effects.



▲ FIGURE 5–9
Voltage-divider bias.

To analyze a voltage-divider circuit in which I_B is small compared to I_2, first calculate the voltage on the base using the unloaded voltage-divider rule:

$$V_B \cong \left(\frac{R_2}{R_1 + R_2}\right)V_{CC} \qquad \text{Equation 5–1}$$

Once you know the base voltage, you can find the voltages and currents in the circuit, as follows:

$$V_E = V_B - V_{BE} \qquad \text{Equation 5–2}$$

and

$$I_C \cong I_E = \frac{V_E}{R_E} \qquad \text{Equation 5–3}$$

Then,

$$V_C = V_{CC} - I_C R_C \qquad \text{Equation 5–4}$$

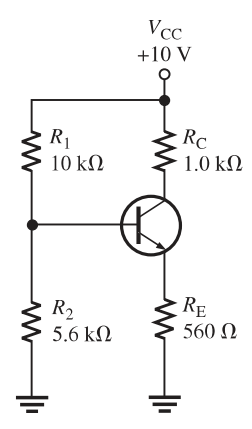
Once you know V_C and V_E, you can determine V_{CE}.

$$V_{CE} = V_C - V_E$$

EXAMPLE 5–2

Determine V_{CE} and I_C in the stiff voltage-divider biased transistor circuit of Figure 5–10 if $\beta_{DC} = 100$.

▶ FIGURE 5–10



Solution

The base voltage is

$$V_B \cong \left(\frac{R_2}{R_1 + R_2}\right)V_{CC} = \left(\frac{5.6\,\text{k}\Omega}{15.6\,\text{k}\Omega}\right)10\,\text{V} = 3.59\,\text{V}$$

So,

$$V_E = V_B - V_{BE} = 3.59\,\text{V} - 0.7\,\text{V} = 2.89\,\text{V}$$

and

$$I_E = \frac{V_E}{R_E} = \frac{2.89\,\text{V}}{560\,\Omega} = 5.16\,\text{mA}$$

Therefore,

$$I_C \cong I_E = \mathbf{5.16\,mA}$$

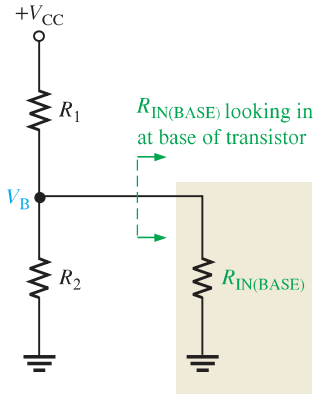
and

$$V_C = V_{CC} - I_C R_C = 10\,\text{V} - (5.16\,\text{mA})(1.0\,\text{k}\Omega) = 4.84\,\text{V}$$
$$V_{CE} = V_C - V_E = 4.84\,\text{V} - 2.89\,\text{V} = \mathbf{1.95\,V}$$

Related Problem If the voltage divider in Figure 5–10 was not stiff, how would V_B be affected?

Open the Multisim file E05-02 in the Examples folder on the companion website. Measure I_C and V_{CE}. If these results do not agree very closely with those in the Example, what original assumption was incorrect?

The basic analysis developed in Example 5–2 is all that is needed for most voltage-divider circuits, but there may be cases where you need to analyze the circuit with more accuracy. Ideally, a voltage-divider circuit is stiff, which means that the transistor does not appear as a significant load. All circuit design involves trade-offs; and one trade-off is that stiff voltage dividers require smaller resistors, which are not always desirable because of potential loading effects on other circuits and added power requirements. If the circuit designer wanted to raise the input resistance, the divider string may not be stiff; and more detailed analysis is required to calculate circuit parameters. To determine if the divider is stiff, you need to examine the dc input resistance looking in at the base as shown in Figure 5–11.



Stiff:

$R_{IN(BASE)} \geqq 10R_2$

$V_B \cong \left(\frac{R_2}{R_1 + R_2}\right) V_{CC}$

Not stiff:

$R_{IN(BASE)} < 10R_2$

$V_B = \left(\frac{R_2 \parallel R_{IN(BASE)}}{R_1 + R_2 \parallel R_{IN(BASE)}}\right) V_{CC}$

◀ FIGURE 5–11

Voltage divider with load.

Loading Effects of Voltage-Divider Bias

DC Input Resistance at the Transistor Base The dc input resistance of the transistor is proportional to β_{DC}, so it will change for different transistors. When a transistor is operating in its linear region, the emitter current (I_E) is $\beta_{DC}I_B$. When the emitter resistor is viewed from the base circuit, the resistor appears to be larger than its actual value because of the dc current gain in the transistor. That is, $R_{IN(BASE)} = V_B/I_B = V_B/(I_E/\beta_{DC})$.

$$R_{IN(BASE)} = \frac{\beta_{DC} V_B}{I_E}$$ Equation 5–5

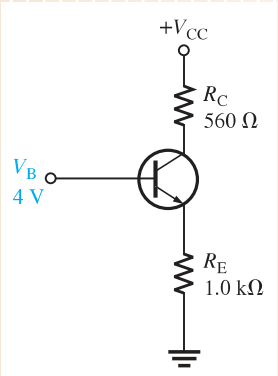
This is the effective load on the voltage divider illustrated in Figure 5–11.

You can quickly estimate the loading effect by comparing $R_{IN(BASE)}$ to the resistor R_2 in the voltage divider. As long as $R_{IN(BASE)}$ is at least ten times larger than R_2, the loading effect will be 10% or less and the voltage divider is stiff. If $R_{IN(BASE)}$ is less than ten times R_2, it should be combined in parallel with R_2.

EXAMPLE 5–3

Determine the dc input resistance looking in at the base of the transistor in Figure 5–12. $\beta_{DC} = 125$ and $V_B = 4\,V$.

▶ FIGURE 5–12



Solution

$$I_E = \frac{V_B - 0.7\,V}{R_E} = \frac{3.3\,V}{1.0\,k\Omega} = 3.3\,mA$$

$$R_{IN(BASE)} = \frac{\beta_{DC} V_B}{I_E} = \frac{125(4\,V)}{3.3\,mA} = \mathbf{152\,k\Omega}$$

Related Problem What is $R_{IN(BASE)}$ in Figure 5–12 if $\beta_{DC} = 60$ and $V_B = 2\,V$?

Thevenin's Theorem Applied to Voltage-Divider Bias

To analyze a voltage-divider biased transistor circuit for base current loading effects, we will apply Thevenin's theorem to evaluate the circuit. First, let's get an equivalent base-emitter circuit for the circuit in Figure 5–13(a) using Thevenin's theorem. Looking out from the base terminal, the bias circuit can be redrawn as shown in Figure 5–13(b). Apply Thevenin's theorem to the circuit left of point *A*, with V_{CC} replaced by a short to ground and the transistor disconnected from the circuit. The voltage at point *A* with respect to ground is

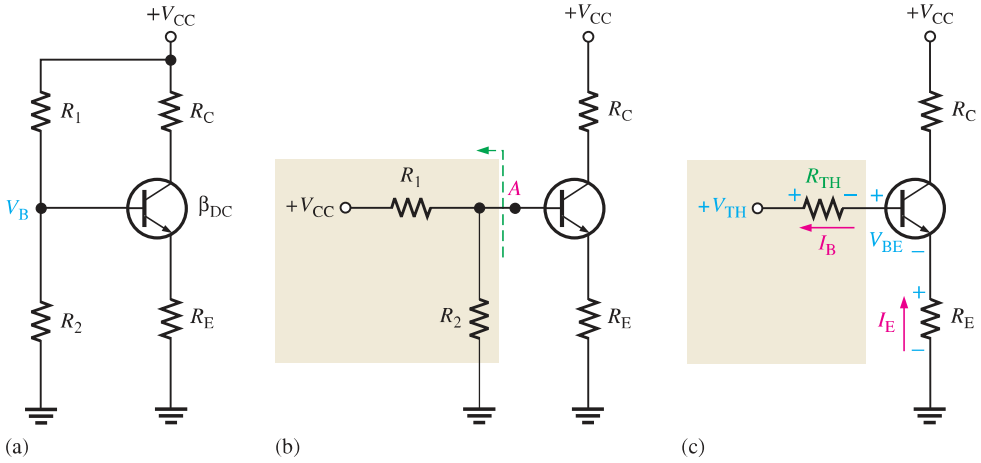
$$V_{TH} = \left(\frac{R_2}{R_1 + R_2}\right)V_{CC}$$

and the resistance is

$$R_{TH} = \frac{R_1 R_2}{R_1 + R_2}$$

▶ FIGURE 5–13

Thevenizing the bias circuit.



The Thevenin equivalent of the bias circuit, connected to the transistor base, is shown in the beige box in Figure 5–13(c). Applying Kirchhoff's voltage law around the equivalent base-emitter loop gives

$$V_{TH} - V_{R_{TH}} - V_{BE} - V_{R_E} = 0$$

Substituting, using Ohm's law, and solving for V_{TH},

$$V_{TH} = I_B R_{TH} + V_{BE} + I_E R_E$$

Substituting I_E/β_{DC} for I_B,

$$V_{TH} = I_E(R_E + R_{TH}/\beta_{DC}) + V_{BE}$$

Then solving for I_E,

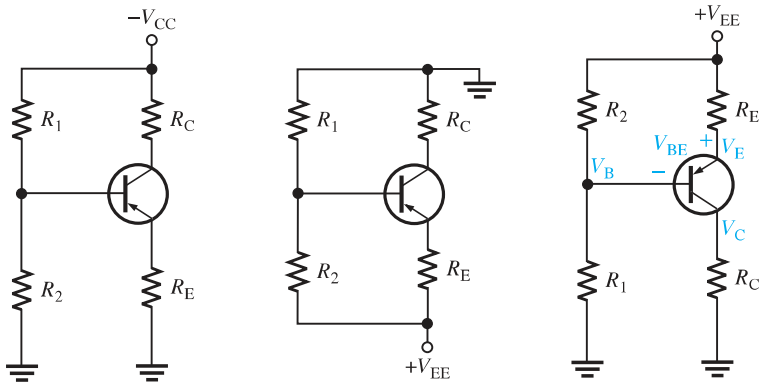
Equation 5–6

$$\boldsymbol{I_E = \frac{V_{TH} - V_{BE}}{R_E + R_{TH}/\beta_{DC}}}$$

If R_{TH}/β_{DC} is small compared to R_E, the result is the same as for an unloaded voltage divider.

Voltage-divider bias is widely used because reasonably good bias stability is achieved with a single supply voltage.

Voltage-Divider Biased PNP Transistor As you know, a *pnp* transistor requires bias polarities opposite to the *npn*. This can be accomplished with a negative collector supply voltage, as in Figure 5–14(a), or with a positive emitter supply voltage, as in Figure 5–14(b).



(a) Negative collector supply voltage, V_{CC}

(b) Positive emitter supply voltage, V_{EE}

(c) The circuit in (b) redrawn

▲ FIGURE 5–14

Voltage-divider biased *pnp* transistor.

In a schematic, the *pnp* is often drawn upside down so that the supply voltage is at the top of the schematic and ground at the bottom, as in Figure 5–14(c).

The analysis procedure is the same as for an *npn* transistor circuit using Thevenin's theorem and Kirchhoff's voltage law, as demonstrated in the following steps with reference to Figure 5–14. For Figure 5–14(a), applying Kirchhoff's voltage law around the base-emitter circuit gives

$$V_{TH} + I_B R_{TH} - V_{BE} + I_E R_E = 0$$

By Thevenin's theorem,

$$V_{TH} = \left(\frac{R_2}{R_1 + R_2}\right) V_{CC}$$

$$R_{TH} = \frac{R_1 R_2}{R_1 + R_2}$$

The base current is

$$I_B = \frac{I_E}{\beta_{DC}}$$

The equation for I_E is

$$\boldsymbol{I_E = \frac{-V_{TH} + V_{BE}}{R_E + R_{TH}/\beta_{DC}}} \qquad \textbf{Equation 5–7}$$

For Figure 5–14(b), the analysis is as follows:

$$-V_{TH} + I_B R_{TH} - V_{BE} + I_E R_E - V_{EE} = 0$$

$$V_{TH} = \left(\frac{R_1}{R_1 + R_2}\right) V_{EE}$$

$$R_{TH} = \frac{R_1 R_2}{R_1 + R_2}$$

$$I_B = \frac{I_E}{\beta_{DC}}$$

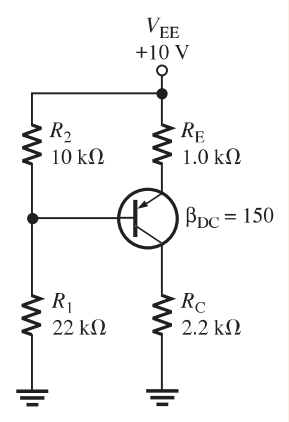
The equation for I_E is

$$\boldsymbol{I_E = \frac{V_{TH} + V_{BE} - V_{EE}}{R_E + R_{TH}/\beta_{DC}}} \qquad \textbf{Equation 5–8}$$

EXAMPLE 5–4

Find I_C and V_{EC} for the *pnp* transistor circuit in Figure 5–15.

▶ FIGURE 5–15



Solution This circuit has the configuration of Figures 5–14(b) and (c). Apply Thevenin's theorem.

$$V_{TH} = \left(\frac{R_1}{R_1 + R_2}\right)V_{EE} = \left(\frac{22\,\text{k}\Omega}{22\,\text{k}\Omega + 10\,\text{k}\Omega}\right)10\,\text{V} = (0.688)10\,\text{V} = 6.88\,\text{V}$$

$$R_{TH} = \frac{R_1R_2}{R_1 + R_2} = \frac{(22\,\text{k}\Omega)(10\,\text{k}\Omega)}{22\,\text{k}\Omega + 10\,\text{k}\Omega} = 6.88\,\text{k}\Omega$$

Use Equation 5–8 to determine I_E.

$$I_E = \frac{V_{TH} + V_{BE} - V_{EE}}{R_E + R_{TH}/\beta_{DC}} = \frac{6.88\,\text{V} + 0.7\,\text{V} - 10\,\text{V}}{1.0\,\text{k}\Omega + 45.9\,\Omega} = \frac{-2.42\,\text{V}}{1.0459\,\text{k}\Omega} = -2.31\,\text{mA}$$

The negative sign on I_E indicates that the assumed current direction in the Kirchhoff's analysis is opposite from the actual current direction. From I_E, you can determine I_C and V_{EC} as follows:

$$I_C = I_E = \mathbf{2.31\,mA}$$
$$V_C = I_CR_C = (2.31\,\text{mA})(2.2\,\text{k}\Omega) = 5.08\,\text{V}$$
$$V_E = V_{EE} - I_ER_E = 10\,\text{V} - (2.31\,\text{mA})(1.0\,\text{k}\Omega) = 7.68\,\text{V}$$
$$V_{EC} = V_E - V_C = 7.68\,\text{V} - 5.08\,\text{V} = \mathbf{2.6\,V}$$

Related Problem Determine $R_{IN(BASE)}$ for Figure 5–15.

Open the Multisim file E05-04 in the Examples folder on the companion website. Measure I_C and V_{EC}.

EXAMPLE 5–5

Find I_C and V_{CE} for a *pnp* transistor circuit with these values: $R_1 = 68\,\text{k}\Omega$, $R_2 = 47\,\text{k}\Omega$, $R_C = 1.8\,\text{k}\Omega$, $R_E = 2.2\,\text{k}\Omega$, $V_{CC} = -6\,\text{V}$, and $\beta_{DC} = 75$. Refer to Figure 5–14(a), which shows the schematic with a negative supply voltage.

Solution Apply Thevenin's theorem.

$$V_{TH} = \left(\frac{R_2}{R_1 + R_2}\right)V_{CC} = \left(\frac{47\,\text{k}\Omega}{68\,\text{k}\Omega + 47\,\text{k}\Omega}\right)(-6\,\text{V})$$
$$= (0.409)(-6\,\text{V}) = -2.45\,\text{V}$$

$$R_{TH} = \frac{R_1R_2}{R_1 + R_2} = \frac{(68\,\text{k}\Omega)(47\,\text{k}\Omega)}{(68\,\text{k}\Omega + 47\,\text{k}\Omega)} = 27.8\,\text{k}\Omega$$

Use Equation 5–7 to determine I_E.

$$I_E = \frac{-V_{TH} + V_{BE}}{R_E + R_{TH}/\beta_{DC}} = \frac{2.45\,\text{V} + 0.7\,\text{V}}{2.2\,\text{k}\Omega + 371\,\Omega}$$
$$= \frac{3.15\,\text{V}}{2.57\,\text{k}\Omega} = 1.23\,\text{mA}$$

From I_E, you can determine I_C and V_{CE} as follows:

$$I_C = I_E = \mathbf{1.23\,mA}$$
$$V_C = -V_{CC} + I_CR_C = -6\,\text{V} + (1.23\,\text{mA})(1.8\,\text{k}\Omega) = -3.79\,\text{V}$$
$$V_E = -I_ER_E = -(1.23\,\text{mA})(2.2\,\text{k}\Omega) = -2.71\,\text{V}$$
$$V_{CE} = V_C - V_E = -3.79\,\text{V} + 2.71\,\text{V} = \mathbf{-1.08\,V}$$

Related Problem What value of β_{DC} is required in this example in order to neglect $R_{IN(BASE)}$ in keeping with the basic ten-times rule for a stiff voltage divider?

SECTION 5–2 CHECKUP

1. If the voltage at the base of a transistor is 5 V and the base current is 5 μA, what is the dc input resistance at the base?
2. If a transistor has a dc beta of 190, $V_B = 2$ V, and $I_E = 2$ mA, what is the dc input resistance at the base?
3. What bias voltage is developed at the base of a transistor if both resistors in a stiff voltage divider are equal and $V_{CC} = +10$ V?
4. What are two advantages of voltage-divider bias?

5–3 OTHER BIAS METHODS

In this section, four additional methods for dc biasing a transistor circuit are discussed. Although these methods are not as common as voltage-divider bias, you should be able to recognize them when you see them and understand the basic differences.

After completing this section, you should be able to

- **Analyze four more types of bias circuits**
- Discuss emitter bias
  - Analyze an emitter-biased circuit
- Discuss base bias
  - Analyze a base-biased circuit
  - Explain Q-point stability of base bias
- Discuss emitter-feedback bias
  - Define negative feedback
  - Analyze an emitter-feedback biased circuit
- Discuss collector-feedback bias
  - Analyze a collector-feedback biased circuit
  - Discuss Q-point stability over temperature

Emitter Bias

Emitter bias provides excellent bias stability in spite of changes in β or temperature. It uses both a positive and a negative supply voltage. To obtain a reasonable estimate of the key dc values in an emitter-biased circuit, analysis is quite easy. In an *npn* circuit, such as shown

in Figure 5–17, the small base current causes the base voltage to be slightly below ground. The emitter voltage is one diode drop less than this. The combination of this small drop across R_B and V_{BE} forces the emitter to be at approximately -1 V. Using this approximation, you can obtain the emitter current as

$$I_E = \frac{-V_{EE} - 1\text{ V}}{R_E}$$

V_{EE} is entered as a negative value in this equation.

You can apply the approximation that $I_C \cong I_E$ to calculate the collector voltage.

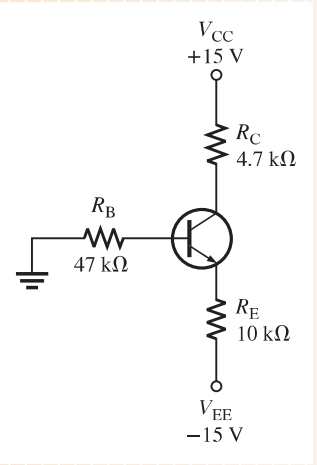
$$V_C = V_{CC} - I_C R_C$$

The approximation that $V_E \cong -1$ V is useful for troubleshooting because you won't need to perform any detailed calculations. As in the case of voltage-divider bias, there is a more rigorous calculation for cases where you need a more exact result.

EXAMPLE 5–6

Calculate I_E and V_{CE} for the circuit in Figure 5–16 using the approximations $V_E \cong -1$ V and $I_C \cong I_E$.

▶ FIGURE 5–16



Solution

$$V_E \cong -1\text{ V}$$

$$I_E = \frac{-V_{EE} - 1\text{ V}}{R_E} = \frac{-(-15\text{ V}) - 1\text{ V}}{10\text{ k}\Omega} = \frac{14\text{ V}}{10\text{ k}\Omega} = \mathbf{1.4\text{ mA}}$$

$$V_C = V_{CC} - I_C R_C = +15\text{ V} - (1.4\text{ mA})(4.7\text{ k}\Omega) = 8.4\text{ V}$$

$$V_{CE} = 8.4\text{ V} - (-1) = \mathbf{9.4\text{ V}}$$

Related Problem If V_{EE} is changed to -12 V, what is the new value of V_{CE}?

The approximation that $V_E \cong -1$ V and the neglect of β_{DC} may not be accurate enough for design work or detailed analysis. In this case, Kirchhoff's voltage law can be applied as follows to develop a more detailed formula for I_E. Kirchhoff's voltage law applied around the base-emitter circuit in Figure 5–17(a), which has been redrawn in part (b) for analysis, gives the following equation:

$$V_{EE} + V_{R_B} + V_{BE} + V_{R_E} = 0$$

Substituting, using Ohm's law,

$$V_{EE} + I_B R_B + V_{BE} + I_E R_E = 0$$