Boolean Algebra and Logic Simplification

BY UNSA SHAKIR

Boolean Algebra

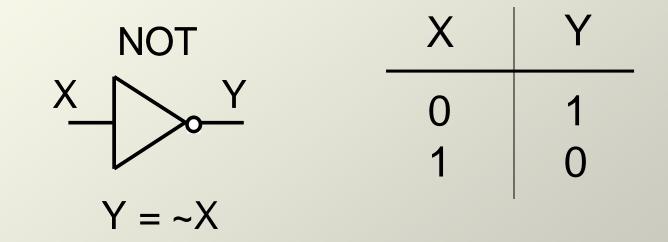
- Boolean algebra is a mathematical system for the manipulation of variables that can have one of two values.
 - In formal logic, these values are "true" and "false."
 - In digital systems, these values are "on" and "off," 1 and 0, or "high" and "low."
- When we learned numbers like 1, 2, 3, we also then learned how to add, multiply, etc. with them. Boolean Algebra covers operations that we can do with 0's and 1's. Computers do these operations ALL THE TIME and they are basic building blocks of computation inside your computer program.

How does Boolean Algebra fit into the big picture?

- It is part of the Combinational Logic topics (memoryless)
 - Different from the Sequential logic topics (can store information)
- Learning Axioms and theorems of Boolean algebra
 - Allows you to design logic functions
 - Allows you to know how to combine different logic gates
 - Allows you to simplify or optimize on the complex operations

Basic Logic Gates

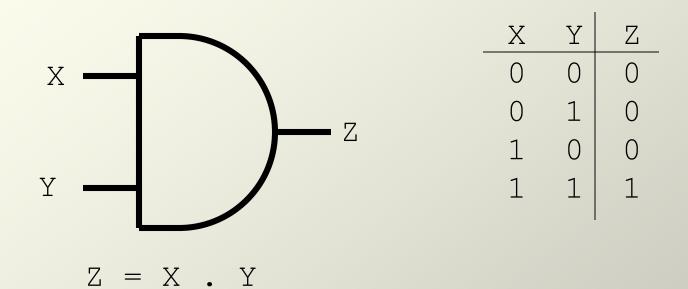
NOT Gate -- Inverter



The NOT operation is most often designated by an overbar. It is sometimes indicated by a prime mark (') or an "elbow" (¬).

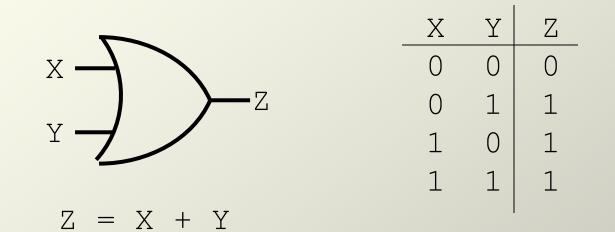
AND Gate

AND (Multiplication)

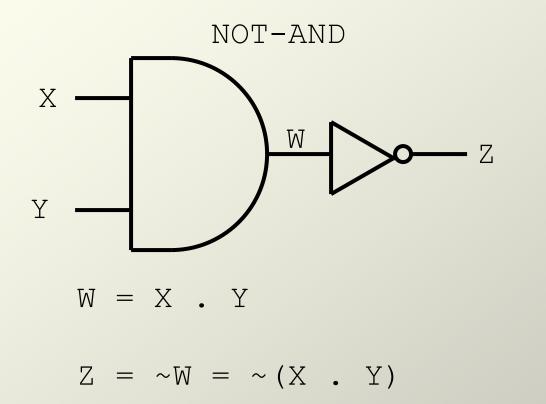


OR Gate

OR (Addition)

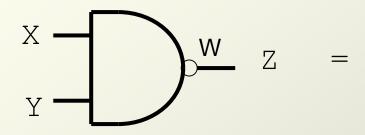


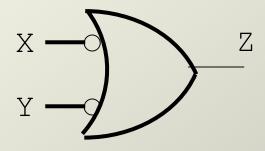
NAND Gate



Х	Y	W	Z
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

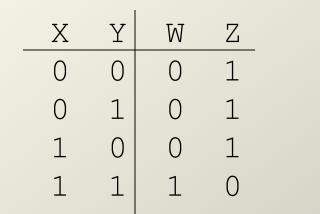
NAND Gate





$$Z = \sim (X \cdot Y)$$

$$Z = -X + -Y$$



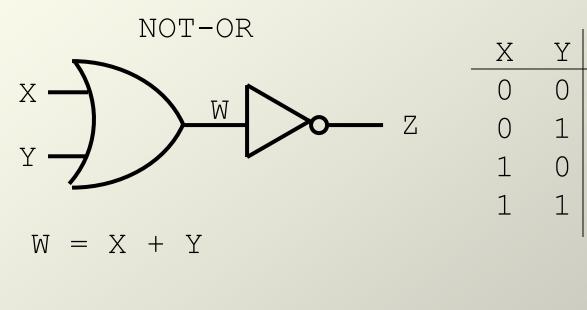
NOR Gate

W Z

0 1

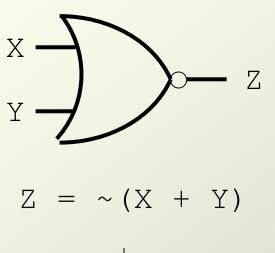
1 0

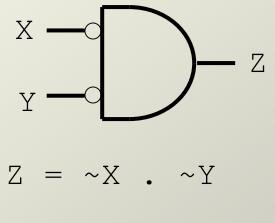
1 0 1 0



 $Z = \sim W = \sim (X + Y)$

NOR Gate

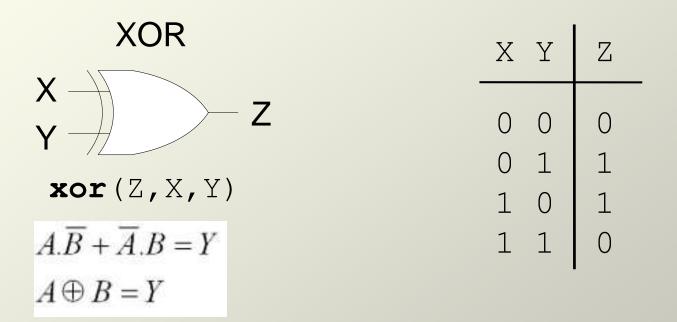




Х	Y	Z
0	0	1
0	1	0
1	0	0
1	1	0

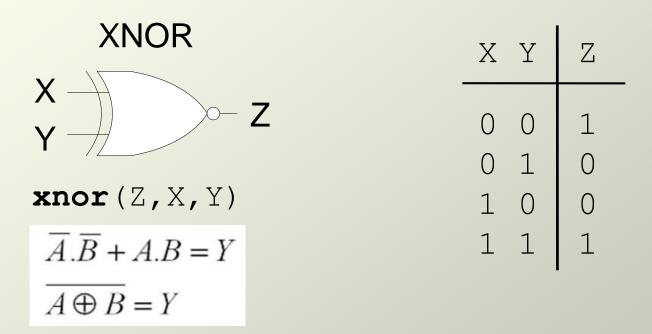
Х	Y	~X	~Y	Z
0	0	1	1	1
0	1	1	0	0
1	0	0	1	0
1	1	0	0	0

Exclusive-OR Gate



The output of an XOR gate is true (1) only when exactly one of its inputs is true (1). If both of an XOR gate's inputs are false (0), or if both of its inputs are true (1), then the output of the XOR gate is false (0).

Exclusive-NOR Gate



• The output of an XNOR gate is **true (1)** when all of its inputs are **true (1)** or when all of its inputs are **false (0)**. If some of its inputs are **true (1)** and others are **false (0)**, then the output of the XNOR gate is **false(0)**.

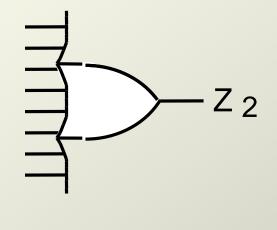
Multiple-input AND Gate

$$z_1$$

Output Z₁ is HIGH only if all inputs are HIGH

Inpu	its	Output
А	B	AB
0	0	0
0	1	0
1	0	0
1	1	1

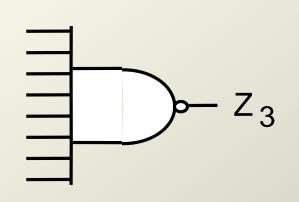
Multiple-input OR Gate

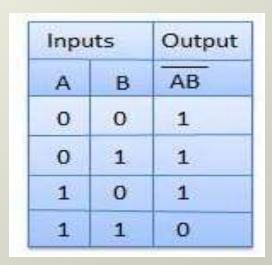


Inpu	ts	Output
А	В	A + B
0	0	0
0	1	1
1	0	1
1	1	1

Output Z₂ is LOW only if all inputs are LOW

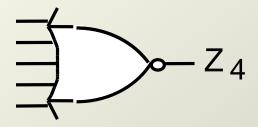
Multiple-input NAND Gate



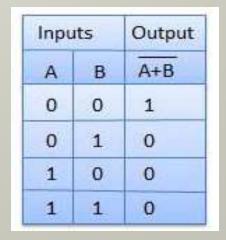


Output Z₃ is LOW only if all inputs are HIGH

Multiple-input NOR Gate



Output Z₄ is HIGH only if all inputs are LOW



Some notation

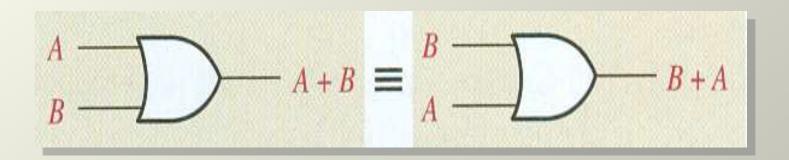
• **Priorities:** $\overline{A} \bullet B + C = ((\overline{A}) \bullet B) + C$

1.Parentheses 2.NOT > AND > XOR > OR

 Variables and their complements are sometimes called literals

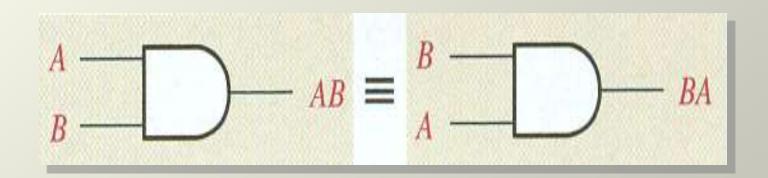
Commutative Law of Addition:

$\mathbf{A} + \mathbf{B} = \mathbf{B} + \mathbf{A}$

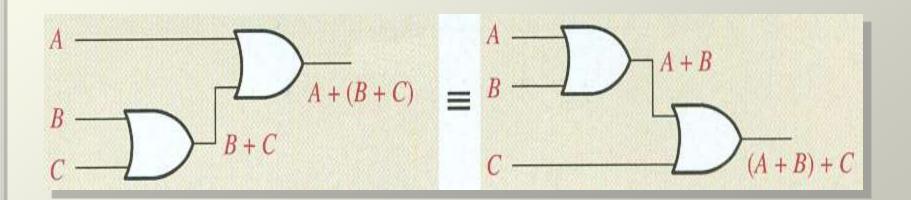


Commutative Law of Multiplication:

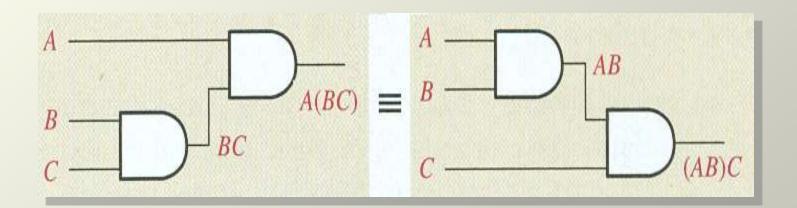
$\mathbf{A} * \mathbf{B} = \mathbf{B} * \mathbf{A}$



Associative Law of Addition:
 A + (B + C) = (A + B) + C

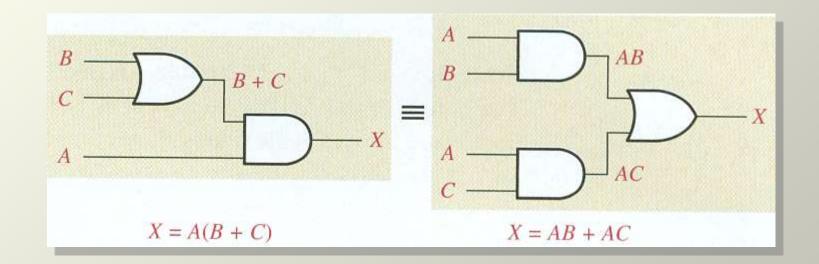


Associative Law of Multiplication:
 A * (B * C) = (A * B) * C

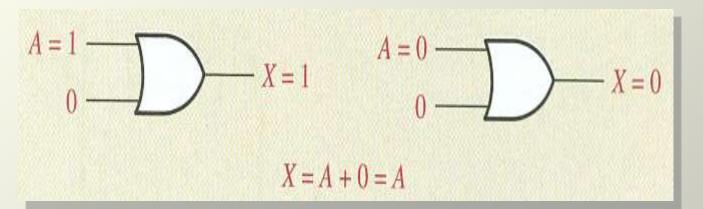


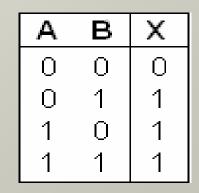
• Distributive Law:

A(B + C) = AB + AC



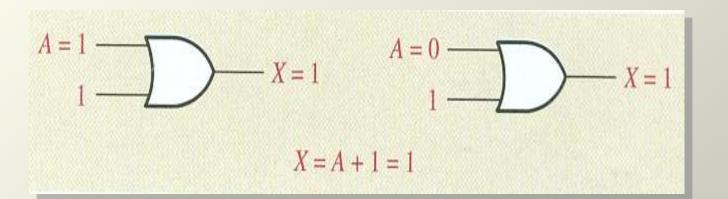
Rule 1 IDENTITY w.r.t ADDITION

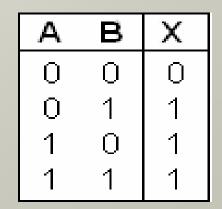




OR Truth Table

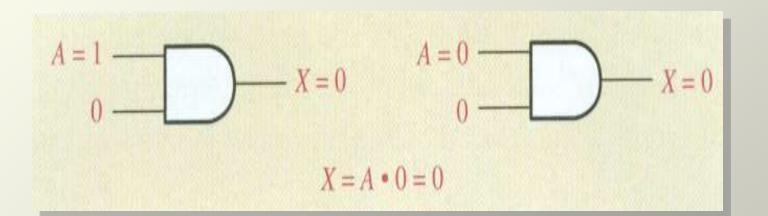
Rule 2 NULL w.r.t ADDITION





OR Truth Table

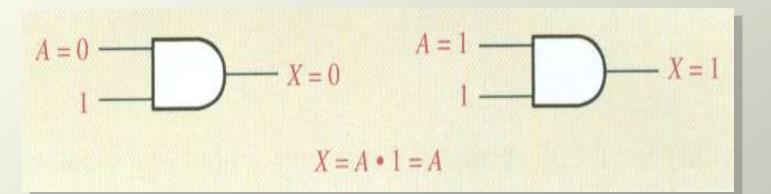
Rule 3 NULL w.r.t MULTIPLICATION

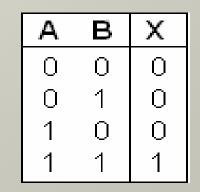


А	в	Х
0	0	0
0	1	0
1	0	0
1	1	1

AND Truth Table

Rule 4 IDENTITY w.r.t MULTIPLICATION

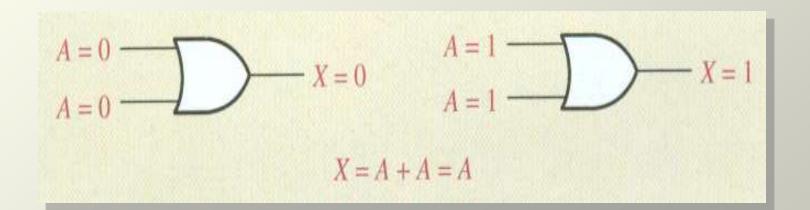




AND Truth Table



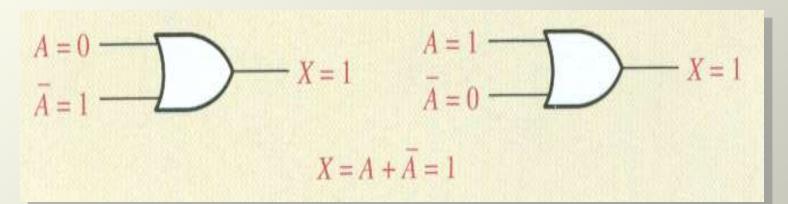
Rule 5 IDEMPOTENT w.r.t ADDITION

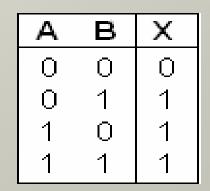


Α	в	X
0	0	0
0	1	1
1	0	1
1	1	1

OR Truth Table

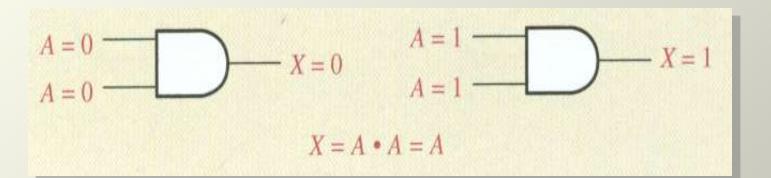
Rule 6 COMPLEMENTARITY w.r.t
 ADDITION







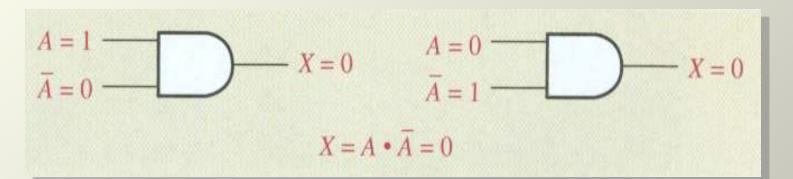
Rule 7 IDEMPOTENT w.r.t MULTIPLICATION

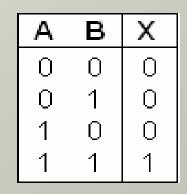


Α	в	Х
0	0	0
0	1	0
1	0	0
1	1	1

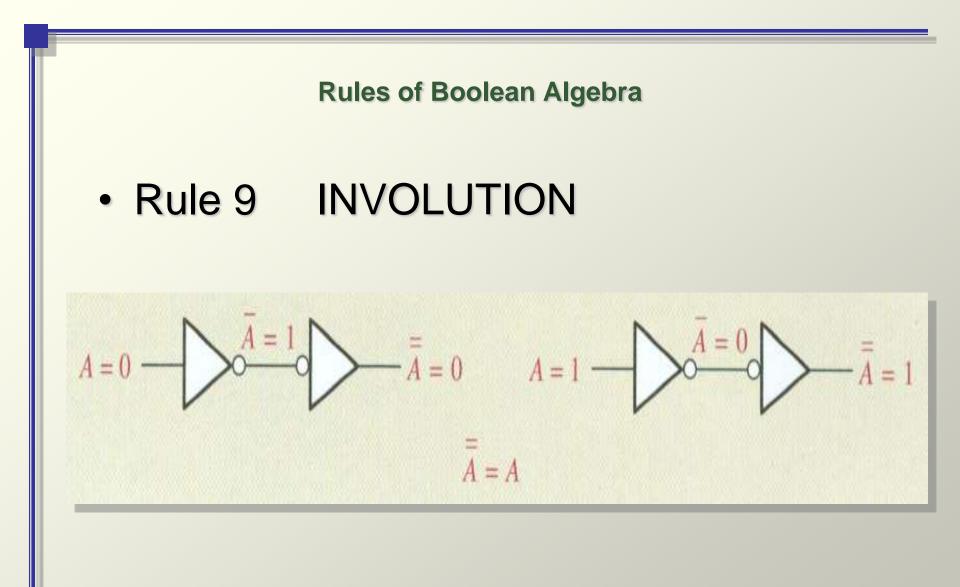
AND Truth Table

Rule 8 COMPLEMENTARITY w.r.t MULTIPLICATION

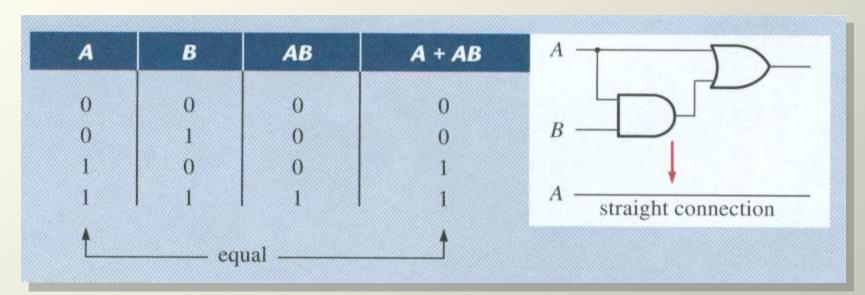




AND Truth Table



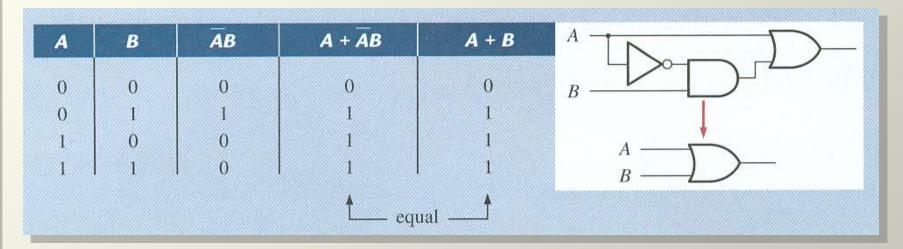
• Rule 10: A + AB = A



Α	в	Х	А	в	Х
0	0	0	0	0	0
0	1	0	0	1	1
1	0	0	1	0	1
1	1	1	1	1	1

AND Truth Table OR Truth Table

• Rule 11: A + AB = A + B



Α	В	Х	А	В	Х
0	0	0	0	0	0
0	1	0	0	1	1
1	0	0	1	0	1
1	1	1	1	1	1

AND Truth Table OR Truth Table

Rule 12: (A + B)(A + C) = A + BC

A	B	C	A + B	A + C	(A + B)(A + C)	BC	A + BC	AT
0	0	0	0	0	0	0	0	
0	0	1	0	1	0	0	0	
0	1	0	1	0	0	0	0	c—
0	1	1	1	1	1	1	1	
1	0	0	1	1	1	0	1	
1	0	1	1	1	1	0	1	
1	1	0	1	1	1	0	1	
1	1		1	1 1	1	1	1	
					t	equal —	1	

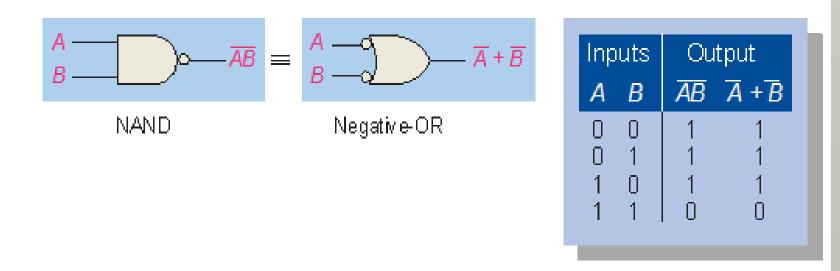
Α	в	Х	А	в	Х
0	0	0	0	0	0
0	1	0	0	1	1
1	0	0	1	0	1
1	1	1	1	1	1

AND Truth Table OR Truth Table

DeMorgan's 1st Theorem

The complement of a product of variables is equal to the sum of the complemented variables. $\overline{AB} = \overline{A} + \overline{B}$

Applying DeMorgan's first theorem to gates:

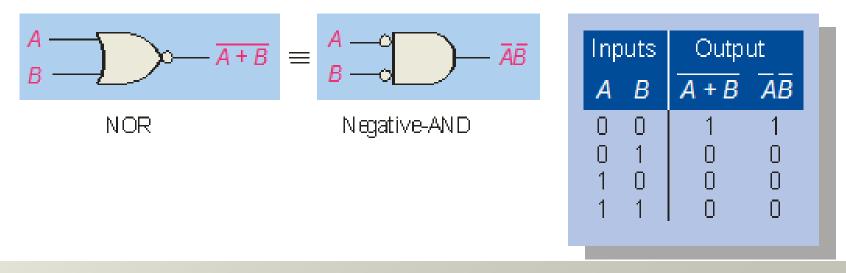


DeMorgan's 2nd Theorem

The complement of a sum of variables is equal to the product of the complemented variables.

 $\overline{A + B} = \overline{A} \cdot \overline{B}$

Applying DeMorgan's second theorem to gates:

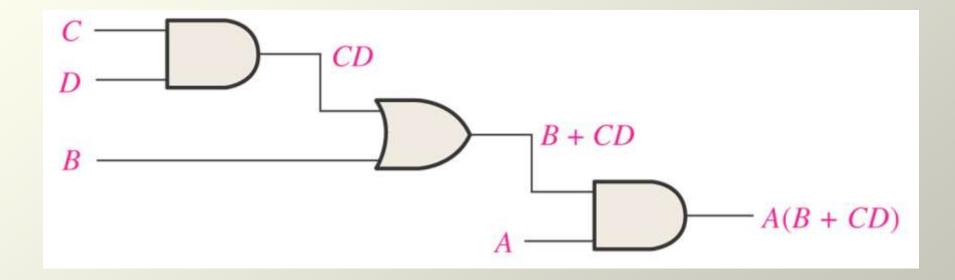


DeMorgan's Theorem

Apply DeMorgan's theorem to remove the overbar covering both terms from the expression $X = \overline{C} + D$.

To apply DeMorgan's theorem to the expression, you can break the overbar covering both terms and change the sign between the terms. This results in $X = \overline{C} \cdot \overline{D}$. Deleting the double bar gives $X = C \cdot \overline{D}$.

A logic circuit showing the development of the Boolean expression for the output.



Example 1

Determine if the following equation is valid

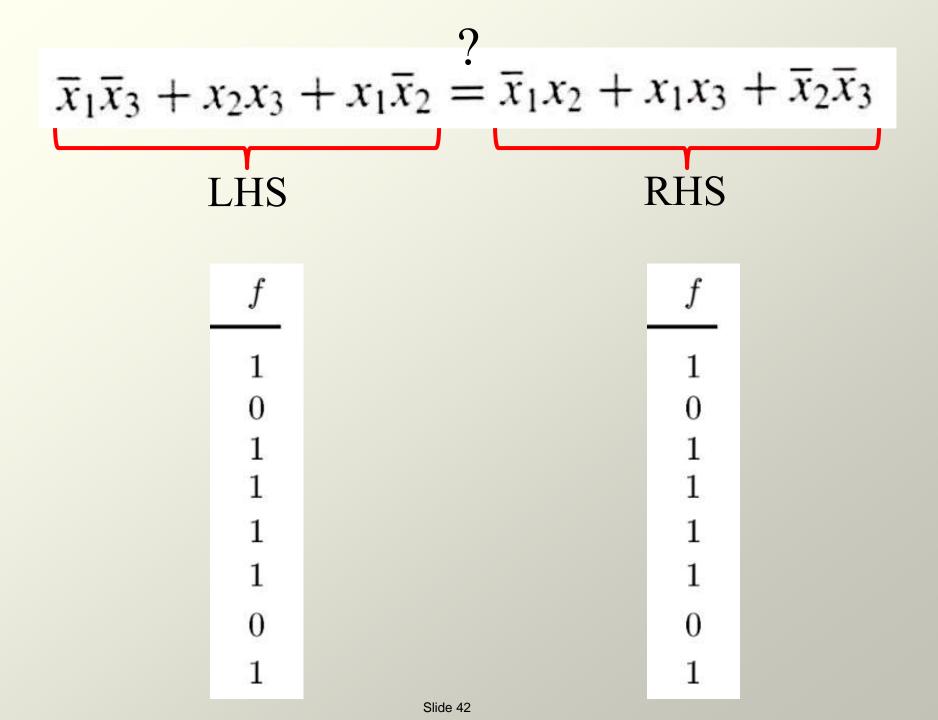
 $\overline{x}_1\overline{x}_3 + x_2x_3 + x_1\overline{x}_2 = \overline{x}_1x_2 + x_1x_3 + \overline{x}_2\overline{x}_3$

Left-Hand Side (LHS)

Row number	x_1	x_2	x_3	$\overline{x_1}\overline{x_3}$	$x_2 x_3$	$x_1 \overline{x_2}$	f
0 1	0	0	0 1	1	0	0	
1 2	0	1	0		0	0	
$\frac{3}{4}$	$0 \\ 1$	$1\\0$	$\begin{array}{c} 1 \\ 0 \end{array}$	0	1 0	$\begin{array}{c} 0 \\ 1 \end{array}$	
5 6	1 1	0 1	$\begin{array}{c} 1\\ 0 \end{array}$	0	0	1	1
7	1	1	1	0	1	0	

Right-Hand Side (RHS)

Row number	x_1	x_2	x_3	$\overline{x_1}x_2$	x_1x_3	$\overline{x_2} \ \overline{x_3}$	f
0	0	0	0	0	0	1	1
1	0	0	1	0	0	0	0
2	0	1	0	1	0	0	1
3	0	1	1	1	0	0	1
4	1	0	0	0	0	1	1
5	1	0	1	0	1	0	1
6	1	1	0	0	0	0	0
7	1	1	1	0	1	$\overset{\circ}{0}$	1

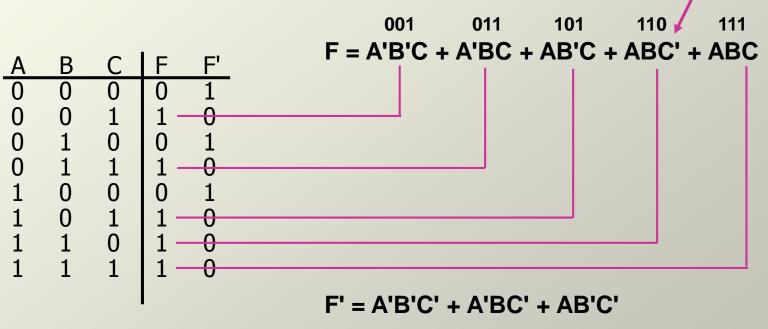


Canonical forms

- Canonical forms
 - Standard forms for Boolean expressions
 - Derived from truth table
 - Generally not the simplest forms (can be minimized)
- Two canonical forms
 - Sum-of-products (minterms)
 - Product-of-sums (maxterms)

Sum-of-products (SOP)

 Also called *disjunctive normal form* (DNF) or *minterm expansion*



0= ' NOTICE 1 TO SOLVE

Minterms

 Variables appear exactly once in each minterm in true or inverted form (but not both)

Α	В	С	minterms	
0	0	0	A'B'C' m0	F in canonical form:
0	0	1	A'B'C m1	$F(A,B,C) = \Sigma m(1,3,5,6,7)$
0			A'BC' m2	= m1 + m3 + m5 + m6 + m7
0			A'BC m3	= A'B'C+A'BC+AB'C+ABC'+ABC'
1	-		AB'C' m4	
1			AB'C m5	
1			ABC' m6	
1	1	1	ABC m7	
			1	
		ch	/ ort-hand not	ation

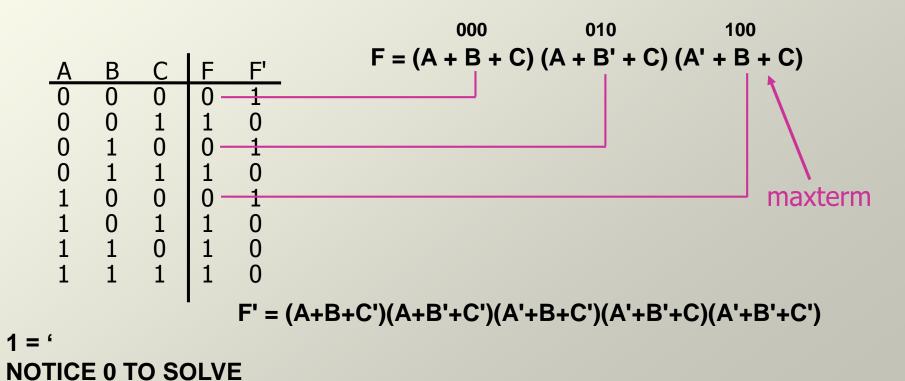
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Product-of-sums (POS)

 Also called conjunctive normal form (CNF) or maxterm expansion



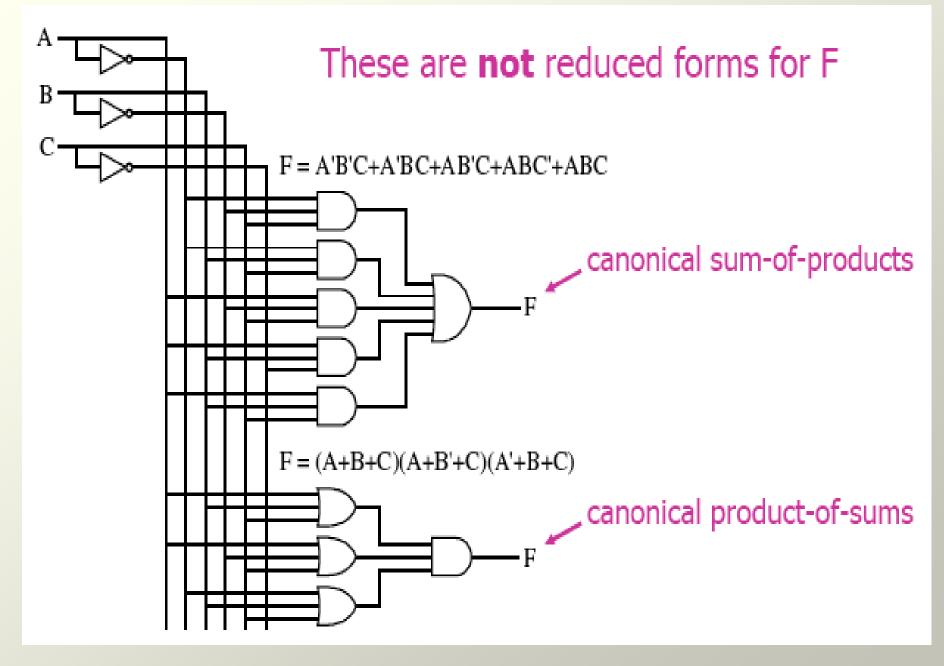
Maxterms

 Variables appear exactly once in each maxterm in true or inverted form (but not both)

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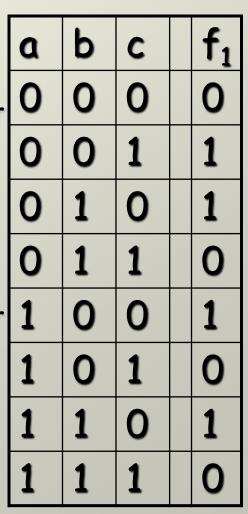
Α	В	С	maxterms
0	0	0	A+B+C M0
0	0	1	A+B+C' M1
0	1	0	A+B'+C M2
0	1	1	A+B'+C' M3
1	0	0	A'+B+C M4
1	0	1	A'+B+C' M5
1	1	0	A'+B'+C M6
1	1	1	A'+B'+C' M7
			1
		shc	ort-hand notation

F in canonical form: $F(A,B,C) = \Pi M(0,2,4)$ $= M0 \bullet M2 \bullet M4$ = (A+B+C)(A+B'+C)(A'+B+C)



Example

- Truth table for f₁(a,b,c) at right
- The canonical sum-of-products form for f_1 is $f_1(a,b,c) = m_1 + m_2 + m_4 + m_6$ = a'b'c + a'bc' + ab'c' + abc'
- The canonical product-of-sums form for f_1 is $f_1(a,b,c) = M_0 \cdot M_3 \cdot M_5 \cdot M_7$ $= (a+b+c)\cdot(a+b'+c')\cdot(a'+b'+c').$



Example 2

Design the minimum-cost product-ofsums and sum-of-product expression for the function $f(x_1, x_2, x_3) = \Sigma m(0, 2, 4, 5, 6, 7)$

Minterms and Maxterms (with three variables)

Row number	x_1	x_2	x_3	Minterm	Maxterm
$egin{array}{ccc} 0 \ 1 \ 2 \ 3 \ 4 \ 5 \ 6 \ 7 \end{array}$	$egin{array}{c} 0 \\ 0 \\ 0 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \end{array}$	$egin{array}{c} 0 \\ 0 \\ 1 \\ 1 \\ 0 \\ 0 \\ 1 \\ 1 \\ 1 \end{array}$	$egin{array}{ccc} 0 \\ 1 \\ 0 \\ 1 \\ 0 \\ 1 \\ 0 \\ 1 \\ 1 \end{array}$	$ \begin{array}{c} m_0 = \overline{x}_1 \overline{x}_2 \overline{x}_3 \\ m_1 = \overline{x}_1 \overline{x}_2 x_3 \\ m_2 = \overline{x}_1 \overline{x}_2 \overline{x}_3 \\ m_3 = \overline{x}_1 x_2 \overline{x}_3 \\ m_4 = x_1 \overline{x}_2 \overline{x}_3 \\ m_5 = x_1 \overline{x}_2 \overline{x}_3 \\ m_6 = x_1 \overline{x}_2 \overline{x}_3 \\ m_7 = x_1 \overline{x}_2 x_3 \end{array} $	$M_{0} = x_{1} + x_{2} + x_{3}$ $M_{1} = x_{1} + x_{2} + \overline{x}_{3}$ $M_{2} = x_{1} + \overline{x}_{2} + \overline{x}_{3}$ $M_{3} = x_{1} + \overline{x}_{2} + \overline{x}_{3}$ $M_{4} = \overline{x}_{1} + x_{2} + \overline{x}_{3}$ $M_{5} = \overline{x}_{1} + x_{2} + \overline{x}_{3}$ $M_{6} = \overline{x}_{1} + \overline{x}_{2} + \overline{x}_{3}$ $M_{7} = \overline{x}_{1} + \overline{x}_{2} + \overline{x}_{3}$

Minterms and Maxterms (with three variables)

Row number	x_1	x_2	x_3	Minterm	Maxterm
0	0	0	0	$m_0 = \overline{x}_1 \overline{x}_2 \overline{x}_3$	$M_0 = x_1 + x_2 + x_3$
1	0	0	1	$m_1 = \overline{x}_1 \overline{x}_2 x_3$	$M_1 = x_1 + x_2 + \overline{x}_3$
2	0	1	0	$m_2 = \overline{x}_1 x_2 \overline{x}_3$	$M_2 = x_1 + \overline{x}_2 + x_3$
3	0	1	1	$m_3 = \overline{x}_1 x_2 x_3$	$M_3 = x_1 + \overline{x}_2 + \overline{x}_3$
4	1	0	0	$m_4 = x_1 \overline{x}_2 \overline{x}_3$	$M_4 = \overline{x}_1 + x_2 + x_3$
5	1	0	1	$m_5 = x_1 \overline{x}_2 x_3$	$M_5 = \overline{x}_1 + x_2 + \overline{x}_3$
6	1	1	0	$m_6 = x_1 x_2 \overline{x}_3$	$M_6 = \overline{x}_1 + \overline{x}_2 + x_3$
7	1	1	1	$m_7 = x_1 x_2 x_3$	$M_7 = \overline{x}_1 + \overline{x}_2 + \overline{x}_3$

The function is 1 for these rows

Minterms and Maxterms (with three variables)

Row number	x_1	x_2	x_3	Minterm	Maxterm
$\begin{array}{c} 0 \\ 1 \\ 2 \\ 3 \\ 4 \\ 5 \\ 6 \end{array}$	0 0 0 0 1 1 1	0 0 1 1 0 0 1	0 1 0 1 0 1	$m_0 = \overline{x}_1 \overline{x}_2 \overline{x}_3$ $m_1 = \overline{x}_1 \overline{x}_2 x_3$ $m_2 = \overline{x}_1 x_2 \overline{x}_3$ $m_3 = \overline{x}_1 x_2 x_3$ $m_4 = x_1 \overline{x}_2 \overline{x}_3$ $m_5 = x_1 \overline{x}_2 x_3$	$M_{0} = x_{1} + x_{2} + x_{3}$ $M_{1} = x_{1} + x_{2} + \overline{x}_{3}$ $M_{2} = x_{1} + \overline{x}_{2} + x_{3}$ $M_{3} = x_{1} + \overline{x}_{2} + \overline{x}_{3}$ $M_{4} = \overline{x}_{1} + x_{2} + \overline{x}_{3}$ $M_{5} = \overline{x}_{1} + x_{2} + \overline{x}_{3}$ $M_{5} = \overline{x}_{1} + x_{2} + \overline{x}_{3}$
0 7	1	1	$\begin{array}{c} 0 \\ 1 \end{array}$	$m_6 = x_1 x_2 \overline{x}_3$ $m_7 = x_1 x_2 x_3$	$M_6 = \overline{x}_1 + \overline{x}_2 + x_3$ $M_7 = \overline{x}_1 + \overline{x}_2 + \overline{x}_3$

The function is 1 for these rows The function is 0 for these rows

From SOP to POS and back

- Minterm to maxterm
 - Use maxterms that aren't in minterm expansion
 - $-F(A,B,C) = \sum m(1,3,5,6,7) = \prod M(0,2,4)$
- Maxterm to minterm
 - Use minterms that aren't in maxterm expansion

 $-F(A,B,C) = \prod M(0,2,4) = \sum m(1,3,5,6,7)$

From SOP to POS and back

- Minterm of F to minterm of F'
 - Use minterms that don't appear

 $-F(A,B,C) = \sum m(1,3,5,6,7)$ F' = $\sum m(0,2,4)$

Maxterm of F to maxterm of F'

– Use maxterms that don't appear – $F(A,B,C) = \prod M(0,2,4)F' = \prod M(1,3,5,6,7)$

SOP, POS, and DeMorgan's

- Product-of-sums

 F' = (A+B+C')(A+B'+C')(A'+B+C')(A'+B'+C')
- Apply DeMorgan's to get SOP

- (F')' = ((A+B+C')(A+B'+C')(A'+B+C')(A'+B'+C'))' - F = A'B'C + A'BC + AB'C + ABC

SOP, POS, and DeMorgan's

• Sum-of-products -F' = A'B'C' + A'BC' + AB'C'

Apply DeMorgan's to get POS

$$\overline{A \cdot B} = \overline{A} + \overline{B} \dots \dots \dots (2)$$

-(F')' = (A'B'C' + A'BC' + AB'C')'-F = (A+B+C)(A+B'+C)(A'+B+C) **Conversion of SOP from standard to canonical form**

- Expand non-canonical terms by inserting equivalent of 1 in each missing variable x: (x + x') = 1
- Remove duplicate minterms
- f₁(a,b,c) = a'b'c + bc' + ac'
 - = a'b'c + (a+a')bc' + a(b+b')c'
 - = a'b'c + abc' + a'bc' + abc' + ab'c'
 - = a'b'c + abc' + a'bc + ab'c'

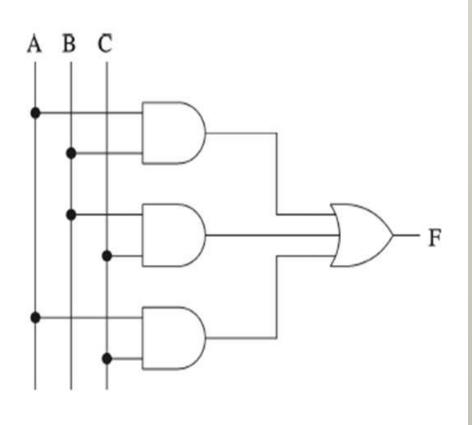
Conversion of POS from standard to canonical form

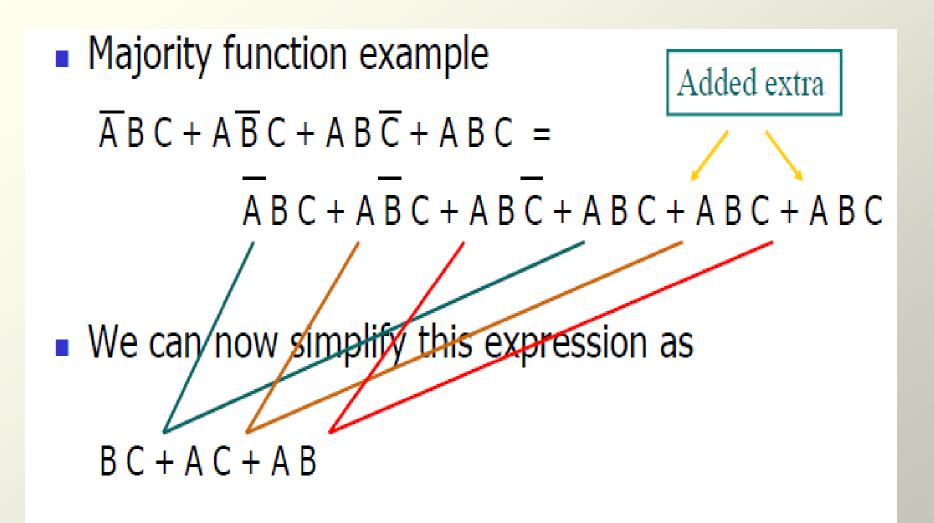
- Expand noncanonical terms by adding 0 in terms of missing variables (*e.g.*, xx' = 0) and using the distributive law (e.g., A + (BC) = (A + B).(A + C))
- Remove duplicate maxterms

Exercise

3-input majority function						
Α	В	С	F			
0	0	0	0			
0	0	1	0			
0	1	0	0			
0	1	1	1			
1 1	0	0	0			
1	0	1	1			
1	1	0	1			
1	1	1	1			

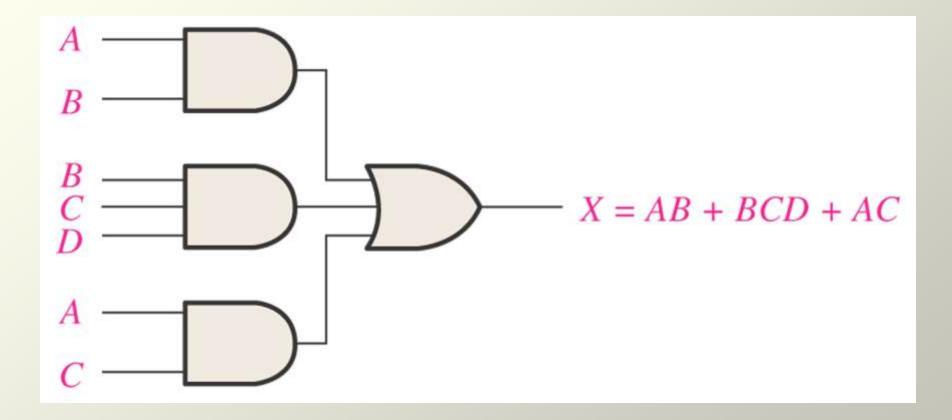
Logical expression form F = A B + B C + A C



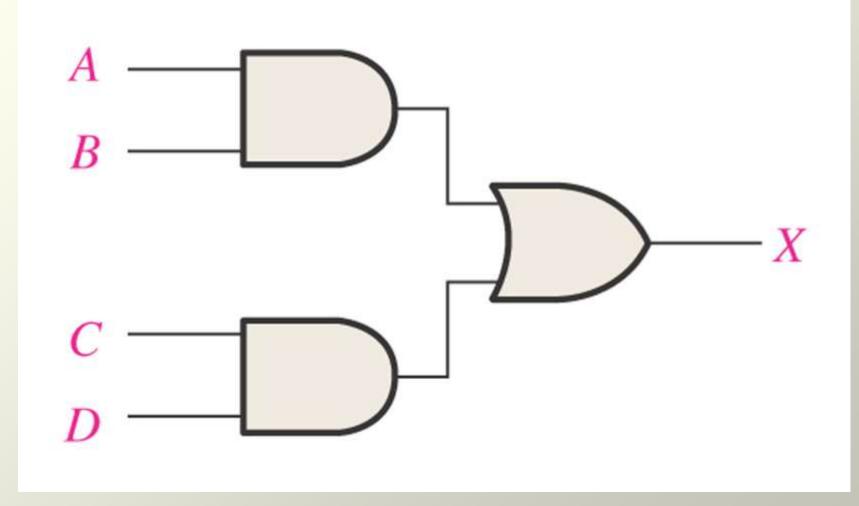


A difficult method to use for complex expressions

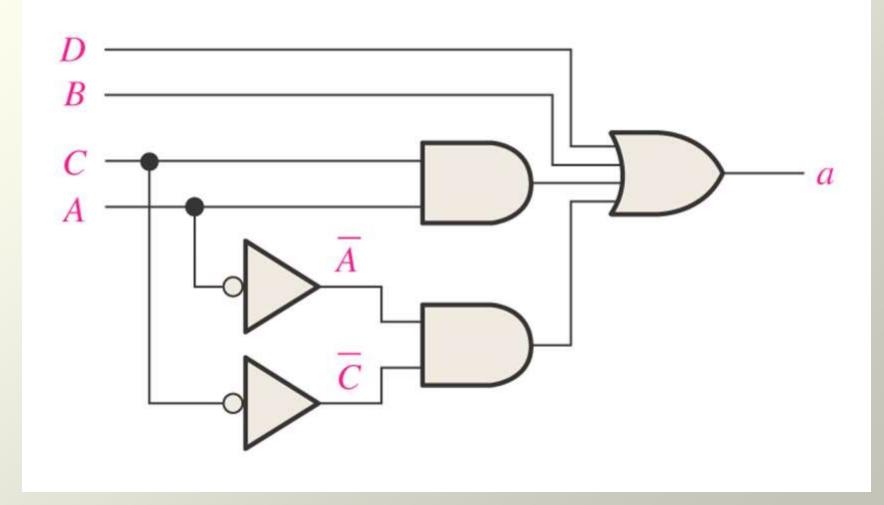
Implementation of the SOP expression AB + BCD + AC.



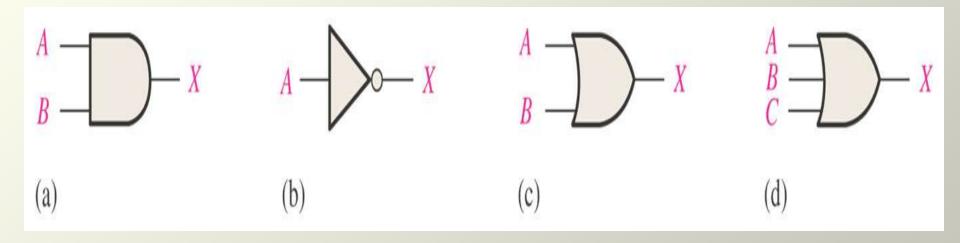
Exercise: The logic implementation for segment X.



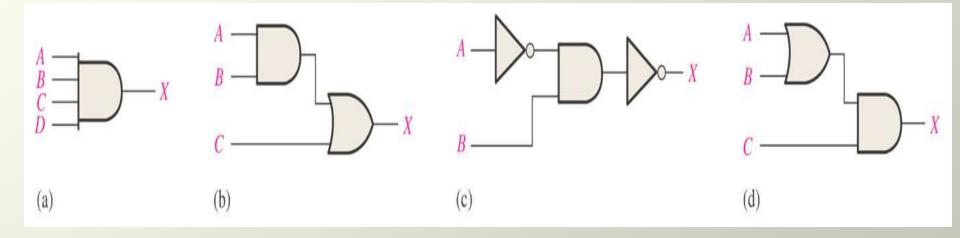
Exercise: The logic implementation for segment a.



Exercise: What is the Boolean expression for each of the logic gates?



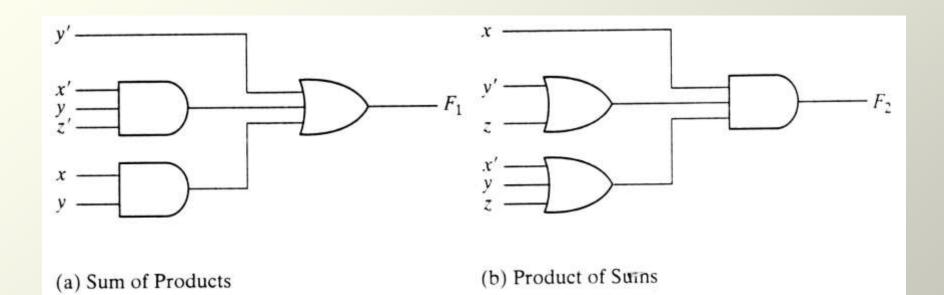
Exercise: What is the Boolean expression for each of the logic gates?



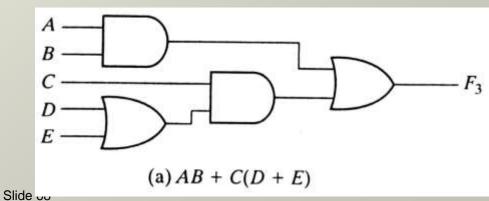
• Example: Prove

x'y'z' + x'yz' + xyz' = x'z' + yz'

Two-level implementation



Multi-level implementation



- Multiple NOR = a complement of OR gate
- Multiple NAND = a complement of AND
- The cascaded NAND operations = sum of products
- The cascaded NOR operations = product of sums

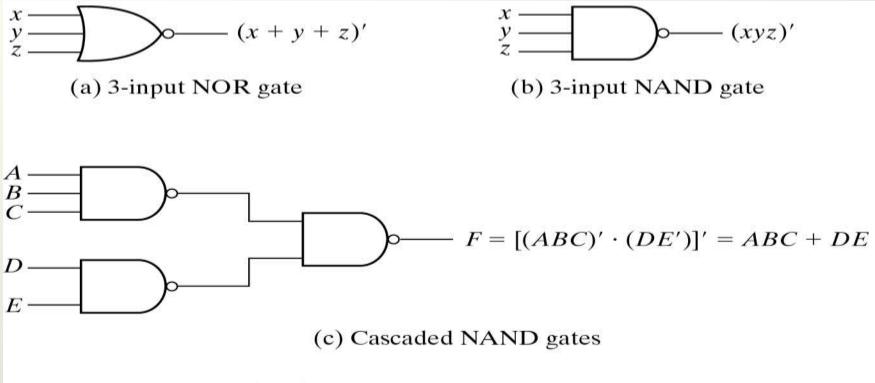


Fig. 2-7 Multiple-input and cascated NOR and NAND gates

- The XOR and XNOR gates are commutative and associative
- Multiple-input XOR gates are uncommon.
- XOR is an odd function: it is equal to 1 if the inputs variables have an odd number of 1's

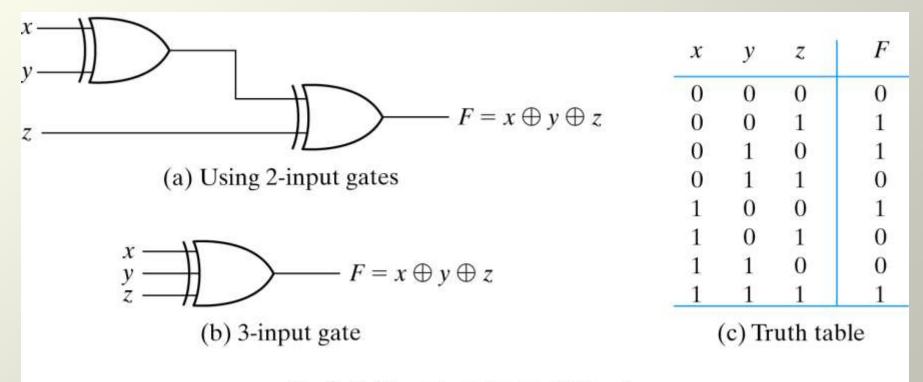
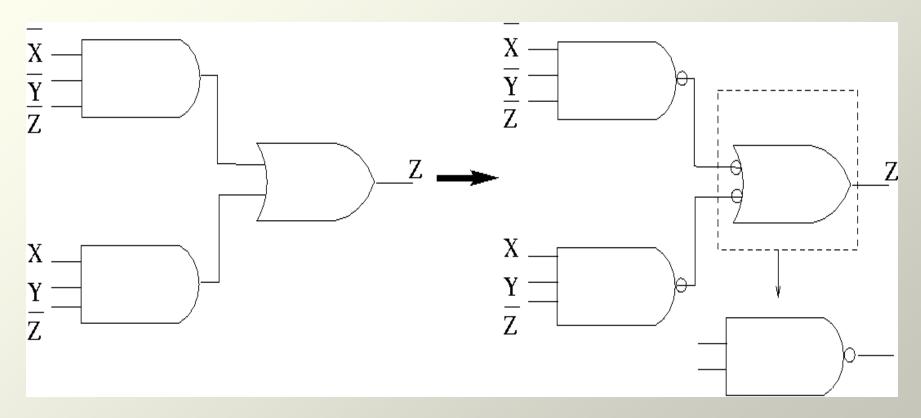


Fig. 2-8 3-input exclusive-OR gate

Two-Level NAND Gate Implementation - Example

- $F(X,Y,Z) = \Sigma m(0,6)$
- 1. Express F in SOP form: F = X'Y'Z' + XYZ'
- 2. Obtain the AND-OR implementation for F.
- 3. Add bubbles and inverters to transform AND-OR to NAND-NAND gates.

Example (cont.)



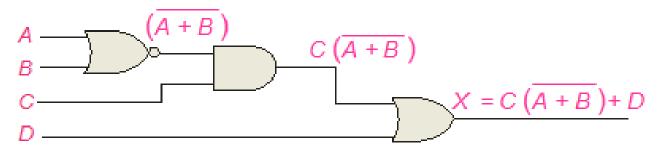
Two-level implementation with NANDs F = X'Y'Z' + XYZ'

Boolean Analysis of Logic Circuits

Combinational logic circuits can be analyzed by writing the expression for each gate and combining the expressions according to the rules for Boolean algebra.

Apply Boolean algebra to derive the expression for X.

Write the expression for each gate:



Applying DeMorgan's theorem and the distribution law:

 $X = C (\overline{A} \ \overline{B}) + D = \overline{A} \overline{B} C + D$

Write an SOP expression for this truth table, and then draw a gate circuit diagram corresponding to that SOP expression:

Α	В	С	Output
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

Finally, simplify this expression using Boolean algebra, and draw a simplified gate circuit based on this new (reduced) Boolean expression.

Examine this truth table and then write both SOP and POS Boolean expressions describing the Output:

A	В	С	Output
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

uiz

1. The associative law for addition is normally written as

a. A + B = B + Ab. (A + B) + C = A + (B + C)c. AB = BAd. A + AB = A

2. The Boolean equation AB + AC = A(B + C) illustrates

a. the distribution law

b. the commutative law

c. the associative law

d. DeMorgan's theorem



3. The Boolean expression $A \cdot 1$ is equal to

- a. A
 b. B
 c. 0
 d. 1
- 4. The Boolean expression A + 1 is equal to
 - a. *A*
 - b. *B*
 - c. 0
 - d. 1



- 5. The Boolean equation AB + AC = A(B + C) illustrates
 - a. the distribution law
 - b. the commutative law
 - c. the associative law
 - d. DeMorgan's theorem
- 6. A Boolean expression that is in standard SOP form is
 - a. the minimum logic expression
 - b. contains only one product term
 - c. has every variable in the domain in every term
 - d. none of the above

Quiz

Answer	Answers:					
1. b	6. c					
2. c						
3. a						
4. d						
5. a						

The end