

Without  $r_d$ ,

$$A_v = \frac{g_m R_S}{1 + g_m R_S} = \frac{(2.28 \text{ mS})(2.2 \text{ k}\Omega)}{1 + (2.28 \text{ mS})(2.2 \text{ k}\Omega)}$$

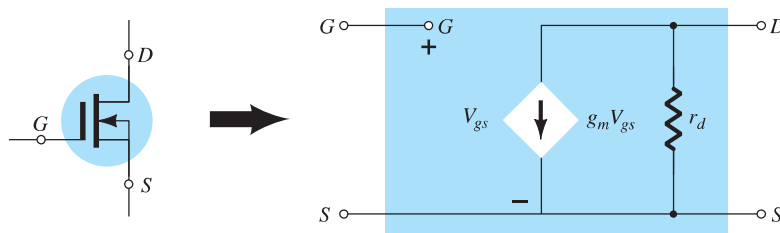
$$= \frac{5.02}{1 + 5.02} = \mathbf{0.83}$$

which shows that  $r_d$  usually has little effect on the gain of the configuration.

## 8.8 DEPLETION-TYPE MOSFETS

The fact that Shockley's equation is also applicable to depletion-type MOSFETs (D-MOSFETs) results in the same equation for  $g_m$ . In fact, the ac equivalent model for D-MOSFETs shown in Fig. 8.33 is exactly the same as that employed for JFETs, as shown in Fig. 8.8.

The only difference offered by D-MOSFETs is that  $V_{GS_Q}$  can be positive for  $n$ -channel devices and negative for  $p$ -channel units. The result is that  $g_m$  can be greater than  $g_{m0}$ , as demonstrated by the example to follow. The range of  $r_d$  is very similar to that encountered for JFETs.

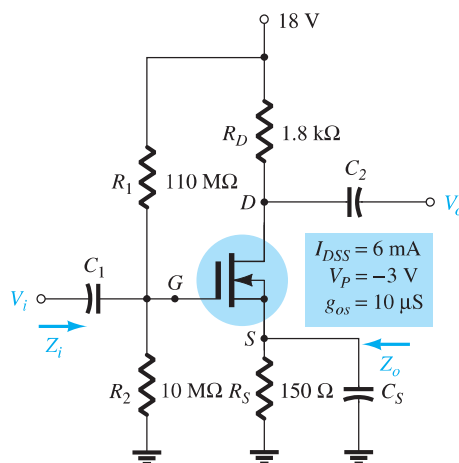


**FIG. 8.33**

*D-MOSFET ac equivalent model.*

**EXAMPLE 8.11** The network of Fig. 8.34 was analyzed as Example 7.7, resulting in  $V_{GS_Q} = 0.35 \text{ V}$  and  $I_{D_Q} = 7.6 \text{ mA}$ .

- Determine  $g_m$  and compare to  $g_{m0}$ .
- Find  $r_d$ .
- Sketch the ac equivalent network for Fig. 8.34.
- Find  $Z_i$ .
- Calculate  $Z_o$ .
- Find  $A_v$ .

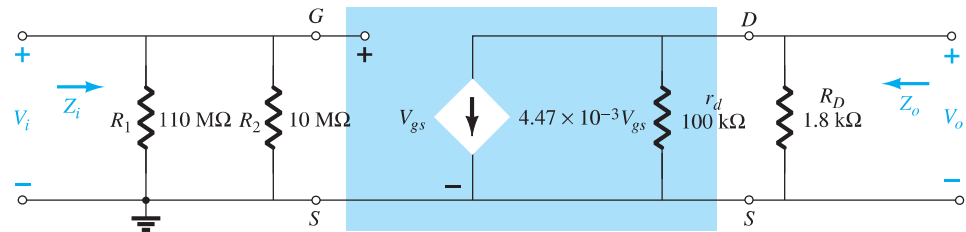


**FIG. 8.34**

*Network for Example 8.11.*

**Solution:**

- a.  $g_{m0} = \frac{2I_{DSS}}{|V_P|} = \frac{2(6 \text{ mA})}{3 \text{ V}} = 4 \text{ mS}$   
 $g_m = g_{m0} \left( 1 - \frac{V_{GSQ}}{V_P} \right) = 4 \text{ mS} \left( 1 - \frac{(+0.35 \text{ V})}{(-3 \text{ V})} \right) = 4 \text{ mS}(1 + 0.117) = \mathbf{4.47 \text{ mS}}$
- b.  $r_d = \frac{1}{y_{os}} = \frac{1}{10 \mu\text{S}} = \mathbf{100 \text{ k}\Omega}$
- c. See Fig. 8.35. Note the similarities with the network of Fig. 8.23. Equations (8.28) through (8.32) are therefore applicable.



**FIG. 8.35**

AC equivalent circuit for Fig. 8.34.

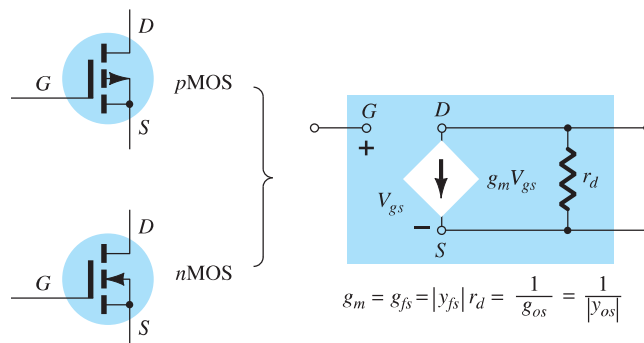
- d. Eq. (8.28):  $Z_i = R_1 \parallel R_2 = 10 \text{ M}\Omega \parallel 110 \text{ M}\Omega = \mathbf{9.17 \text{ M}\Omega}$
- e. Eq. (8.29):  $Z_o = r_d \parallel R_D = 100 \text{ k}\Omega \parallel 1.8 \text{ k}\Omega = \mathbf{1.77 \text{ k}\Omega} \cong R_D = \mathbf{1.8 \text{ k}\Omega}$
- f.  $r_d \geq 10R_D \rightarrow 100 \text{ k}\Omega \geq 18 \text{ k}\Omega$   
 Eq. (8.32):  $A_v = -g_m R_D = -(4.47 \text{ mS})(1.8 \text{ k}\Omega) = \mathbf{8.05}$

**8.9 ENHANCEMENT-TYPE MOSFETS**

The enhancement-type MOSFET (E-MOSFET) can be either an *n*-channel (*n*MOS) or *p*-channel (*p*MOS) device, as shown in Fig. 8.36. The ac small-signal equivalent circuit of either device is shown in Fig. 8.36, revealing an open-circuit between gate and drain–source channel and a current source from drain to source having a magnitude dependent on the gate-to-source voltage. There is an output impedance from drain to source  $r_d$ , which is usually provided on specification sheets as a conductance  $g_{os}$  or admittance  $y_{os}$ . The device transconductance  $g_m$  is provided on specification sheets as the forward transfer admittance  $y_{fs}$ .

In our analysis of JFETs, an equation for  $g_m$  was derived from Shockley’s equation. For E-MOSFETs, the relationship between output current and controlling voltage is defined by

$$I_D = k(V_{GS} - V_{GS(Th)})^2$$



**FIG. 8.36**

Enhancement MOSFET ac small-signal model.

Since  $g_m$  is still defined by

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

we can take the derivative of the transfer equation to determine  $g_m$  as an operating point. That is,

$$\begin{aligned} g_m &= \frac{dI_D}{dV_{GS}} = \frac{d}{dV_{GS}} k(V_{GS} - V_{GS(\text{Th})})^2 = k \frac{d}{dV_{GS}} (V_{GS} - V_{GS(\text{Th})})^2 \\ &= 2k(V_{GS} - V_{GS(\text{Th})}) \frac{d}{dV_{GS}} (V_{GS} - V_{GS(\text{Th})}) = 2k(V_{GS} - V_{GS(\text{Th})})(1 - 0) \end{aligned}$$

and

$$g_m = 2k(V_{GS_Q} - V_{GS(\text{Th})}) \quad (8.45)$$

Recall that the constant  $k$  can be determined from a given typical operating point on a specification sheet. In every other respect, the ac analysis is the same as that employed for JFETs or D-MOSFETs. Be aware, however, that the characteristics of an E-MOSFET are such that the biasing arrangements are somewhat limited.

### 8.10 E-MOSFET DRAIN-FEEDBACK CONFIGURATION

The E-MOSFET drain-feedback configuration appears in Fig. 8.37. Recall from dc calculations that  $R_G$  could be replaced by a short-circuit equivalent since  $I_G = 0$  A and therefore  $V_{R_G} = 0$  V. However, for ac situations it provides an important high impedance between  $V_o$  and  $V_i$ . Otherwise, the input and output terminals would be connected directly and  $V_o = V_i$ .

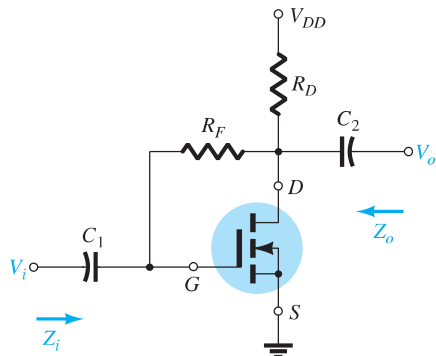


FIG. 8.37

E-MOSFET drain-feedback configuration.

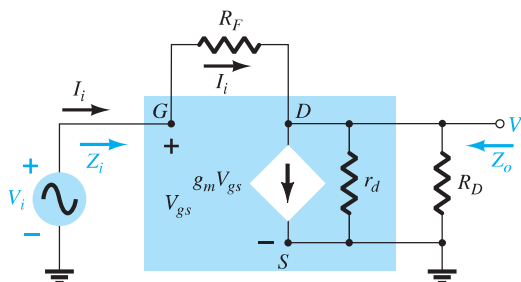


FIG. 8.38

AC equivalent of the network of Fig. 8.37.

Substituting the ac equivalent model for the device results in the network of Fig. 8.38. Note that  $R_F$  is not within the shaded area defining the equivalent model of the device, but does provide a direct connection between input and output circuits.

**Z<sub>i</sub>** Applying Kirchhoff's current law to the output circuit (at node  $D$  in Fig. 8.38) results in

$$I_i = g_m V_{gs} + \frac{V_o}{r_d \parallel R_D}$$

and

$$V_{gs} = V_i$$

so that

$$I_i = g_m V_i + \frac{V_o}{r_d \parallel R_D}$$

or

$$I_i - g_m V_i = \frac{V_o}{r_d \parallel R_D}$$

Therefore,

$$V_o = (r_d \parallel R_D)(I_i - g_m V_i)$$

with

$$I_i = \frac{V_i - V_o}{R_F} = \frac{V_i - (r_d \parallel R_D)(I_i - g_m V_i)}{R_F}$$

and

$$I_i R_F = V_i - (r_d \parallel R_D) I_i + (r_d \parallel R_D) g_m V_i$$

so that

$$V_i [1 + g_m (r_d \parallel R_D)] = I_i [R_F + r_d \parallel R_D]$$

and finally,

$$Z_i = \frac{V_i}{I_i} = \frac{R_F + r_d \parallel R_D}{1 + g_m (r_d \parallel R_D)} \quad (8.46)$$

Typically,  $R_F \gg r_d \parallel R_D$ , so that

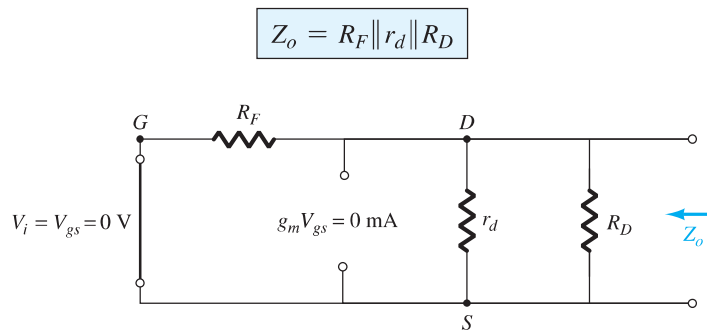
$$Z_i \cong \frac{R_F}{1 + g_m (r_d \parallel R_D)}$$

For  $r_d \geq 10R_D$ ,

$$Z_i \cong \frac{R_F}{1 + g_m R_D} \quad R_F \gg r_d \parallel R_D, r_d \geq 10R_D \quad (8.47)$$

**Z<sub>o</sub>** Substituting  $V_i = 0$  V results in  $V_{gs} = 0$  V and  $g_m V_{gs} = 0$ , with a short-circuit path from gate to ground as shown in Fig. 8.39.  $R_F$ ,  $r_d$ , and  $R_D$  are then in parallel and

$$Z_o = R_F \parallel r_d \parallel R_D \quad (8.48)$$



**FIG. 8.39**

Determining  $Z_o$  for the network of Fig. 8.37.

Normally,  $R_F$  is so much larger than  $r_d \parallel R_D$  that

$$Z_o \cong r_d \parallel R_D$$

and with  $r_d \geq 10R_D$ ,

$$Z_o \cong R_D \quad R_F \gg r_d \parallel R_D, r_d \geq 10R_D \quad (8.49)$$

**A<sub>v</sub>** Applying Kirchhoff's current law at node  $D$  of Fig. 8.38 results in

$$I_i = g_m V_{gs} + \frac{V_o}{r_d \parallel R_D}$$

but

$$V_{gs} = V_i \quad \text{and} \quad I_i = \frac{V_i - V_o}{R_F}$$

so that

$$\frac{V_i - V_o}{R_F} = g_m V_i + \frac{V_o}{r_d \parallel R_D}$$

and

$$\frac{V_i}{R_F} - \frac{V_o}{R_F} = g_m V_i + \frac{V_o}{r_d \parallel R_D}$$

so that

$$V_o \left[ \frac{1}{r_d \parallel R_D} + \frac{1}{R_F} \right] = V_i \left[ \frac{1}{R_F} - g_m \right]$$

and

$$A_v = \frac{V_o}{V_i} = \frac{\left[ \frac{1}{R_F} - g_m \right]}{\left[ \frac{1}{r_d \parallel R_D} + \frac{1}{R_F} \right]}$$

but

$$\frac{1}{r_d \parallel R_D} + \frac{1}{R_F} = \frac{1}{R_F \parallel r_d \parallel R_D}$$

and

$$g_m \gg \frac{1}{R_F}$$

so that

$$A_v = -g_m(R_F \parallel r_d \parallel R_D) \quad (8.50)$$

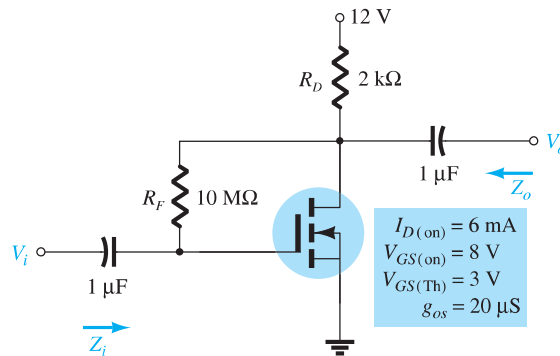
Since  $R_F$  is usually  $\gg r_d \parallel R_D$  and if  $r_d \geq 10R_D$ ,

$$A_v \cong -g_m R_D \quad R_F \gg r_d \parallel R_D, r_d \geq 10R_D \quad (8.51)$$

**Phase Relationship** The negative sign for  $A_v$  reveals that  $V_o$  and  $V_i$  are out of phase by  $180^\circ$ .

**EXAMPLE 8.12** The E-MOSFET of Fig. 8.40 was analyzed in Example 7.10, with the result that  $k = 0.24 \times 10^{-3} \text{ A/V}^2$ ,  $V_{GS_Q} = 6.4 \text{ V}$ , and  $I_{D_Q} = 2.75 \text{ mA}$ .

- Determine  $g_m$ .
- Find  $r_d$ .
- Calculate  $Z_i$  with and without  $r_d$ . Compare results.
- Find  $Z_o$  with and without  $r_d$ . Compare results.
- Find  $A_v$  with and without  $r_d$ . Compare results.



**FIG. 8.40**

Drain-feedback amplifier from Example 8.11.

**Solution:**

a.  $g_m = 2k(V_{GS_Q} - V_{GS(Th)}) = 2(0.24 \times 10^{-3} \text{ A/V}^2)(6.4 \text{ V} - 3 \text{ V})$   
 $= \mathbf{1.63 \text{ mS}}$

b.  $r_d = \frac{1}{g_{os}} = \frac{1}{20 \mu\text{S}} = \mathbf{50 \text{ k}\Omega}$

c. With  $r_d$ ,

$$Z_i = \frac{R_F + r_d \parallel R_D}{1 + g_m(r_d \parallel R_D)} = \frac{10 \text{ M}\Omega + 50 \text{ k}\Omega \parallel 2 \text{ k}\Omega}{1 + (1.63 \text{ mS})(50 \text{ k}\Omega \parallel 2 \text{ k}\Omega)}$$

$$= \frac{10 \text{ M}\Omega + 1.92 \text{ k}\Omega}{1 + 3.13} = \mathbf{2.42 \text{ M}\Omega}$$

Without  $r_d$ ,

$$Z_i \cong \frac{R_F}{1 + g_m R_D} = \frac{10 \text{ M}\Omega}{1 + (1.63 \text{ mS})(2 \text{ k}\Omega)} = \mathbf{2.53 \text{ M}\Omega}$$

which shows that since the condition  $r_d \geq 10R_D = 50 \text{ k}\Omega \geq 40 \text{ k}\Omega$  is satisfied, the results for  $Z_o$  with or without  $r_d$  will be quite close.

d. With  $r_d$ ,

$$Z_o = R_F \parallel r_d \parallel R_D = 10 \text{ M}\Omega \parallel 50 \text{ k}\Omega \parallel 2 \text{ k}\Omega = 49.75 \text{ k}\Omega \parallel 2 \text{ k}\Omega$$

$$= \mathbf{1.92 \text{ k}\Omega}$$

Without  $r_d$ ,

$$Z_o \cong R_D = 2 \text{ k}\Omega$$

again providing very close results.

e. With  $r_d$ ,

$$\begin{aligned} A_v &= -g_m(R_F \parallel r_d \parallel R_D) \\ &= -(1.63 \text{ mS})(10 \text{ M}\Omega \parallel 50 \text{ k}\Omega \parallel 2 \text{ k}\Omega) \\ &= -(1.63 \text{ mS})(1.92 \text{ k}\Omega) \\ &= -3.21 \end{aligned}$$

Without  $r_d$ ,

$$\begin{aligned} A_v &= -g_m R_D = -(1.63 \text{ mS})(2 \text{ k}\Omega) \\ &= -3.26 \end{aligned}$$

which is very close to the above result.

### 8.11 E-MOSFET VOLTAGE-DIVIDER CONFIGURATION

The last E-MOSFET configuration to be examined in detail is the voltage-divider network of Fig. 8.41. The format is exactly the same as appearing in a number of earlier discussions.

Substituting the ac equivalent network for the E-MOSFET results in the configuration of Fig. 8.42, which is exactly the same as Fig. 8.23. The result is that Eqs. (8.28) through (8.32) are applicable, as listed below for the E-MOSFET.

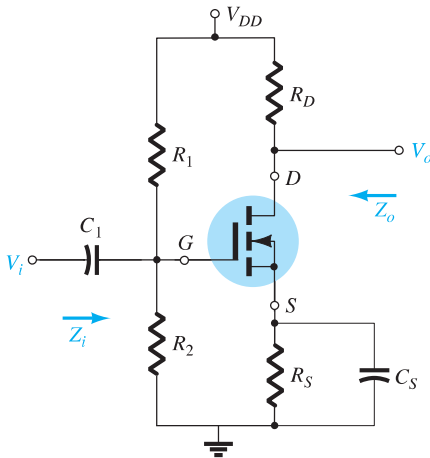


FIG. 8.41

E-MOSFET voltage-divider configuration.

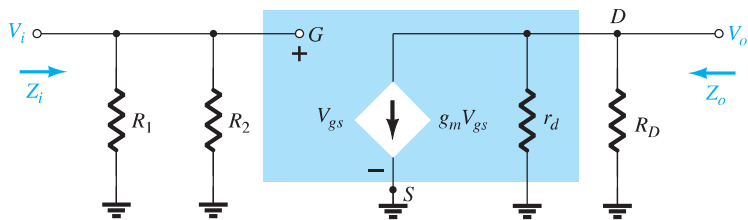


FIG. 8.42

AC equivalent network for the configuration of Fig. 8.41.

$Z_i$

$$Z_i = R_1 \parallel R_2 \tag{8.52}$$

$Z_o$

$$Z_o = r_d \parallel R_D \tag{8.53}$$

For  $r_d \geq 10R_D$ ,

$$Z_o \cong R_D \quad r_d \geq 10R_D \tag{8.54}$$

$A_v$

$$A_v = \frac{V_o}{V_i} = -g_m(r_d \parallel R_D) \tag{8.55}$$

and if  $r_d \geq 10R_D$ ,

$$A_v = \frac{V_o}{V_i} \cong -g_m R_D \quad (8.56)$$

## 8.12 DESIGNING FET AMPLIFIER NETWORKS

Design problems at this stage are limited to obtaining a desired dc bias condition or ac voltage gain. In most cases, the various equations developed are used “in reverse” to define the parameters necessary to obtain the desired gain, input impedance, or output impedance. To avoid unnecessary complexity during the initial stages of the design, the approximate equations are often employed because some variation will occur when calculated resistors are replaced by standard values. Once the initial design is completed, the results can be tested and refinements made using the complete equations.

Throughout the design procedure be aware that although superposition permits a separate analysis and design of the network from a dc and an ac viewpoint, a parameter chosen in the dc environment will often play an important role in the ac response. In particular, recall that the resistance  $R_G$  could be replaced by a short-circuit equivalent in the feedback configuration because  $I_G \cong 0$  A for dc conditions, but for the ac analysis, it presents an important high-impedance path between  $V_o$  and  $V_i$ . In addition, recall that  $g_m$  is larger for operating points closer to the  $I_D$  axis ( $V_{GS} = 0$  V), requiring that  $R_S$  be relatively small. In the unbypassed  $R_S$  network, a small  $R_S$  will also contribute to a higher gain, but for the source-follower, the gain is reduced from its maximum value of 1. In total, simply keep in mind that network parameters can affect the dc and ac levels in different ways. Often a balance must be made between a particular operating point and its effect on the ac response.

In most situations, the available dc supply voltage is known, the FET to be employed has been determined, and the capacitors to be employed at the chosen frequency are defined. It is then necessary to determine the resistive elements necessary to establish the desired gain or impedance level. The next three examples determine the required parameters for a specific gain.

**EXAMPLE 8.13** Design the fixed-bias network of Fig. 8.43 to have an ac gain of 10. That is, determine the value of  $R_D$ .

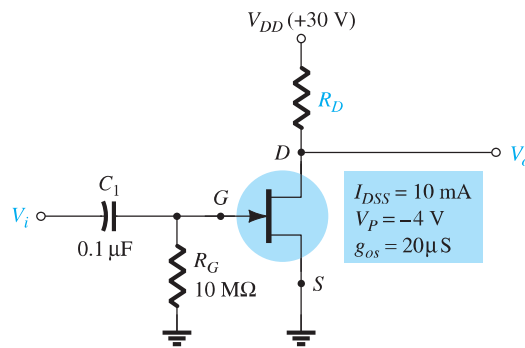


FIG. 8.43

Circuit for desired voltage gain in Example 8.13.

**Solution:** Since  $V_{GS_Q} = 0$  V, the level of  $g_m$  is  $g_{m0}$ . The gain is therefore determined by

$$A_v = -g_m(R_D \parallel r_d) = -g_{m0}(R_D \parallel r_d)$$

with

$$g_{m0} = \frac{2I_{DSS}}{|V_P|} = \frac{2(10 \text{ mA})}{4 \text{ V}} = 5 \text{ mS}$$

The result is

$$-10 = -5 \text{ mS}(R_D \parallel r_d)$$

and

$$R_D \parallel r_d = \frac{10}{5 \text{ mS}} = 2 \text{ k}\Omega$$