8 FET Amplifiers

CHAPTER OBJECTIVES

- Become acquainted with the small-signal ac model for a JFET and MOSFET.
- Be able to perform a small-signal ac analysis of a variety of JFET and MOSFET configurations.
- Begin to appreciate the design sequence applied to FET configurations.
- Understand the effects of a source resistor and load resistor on the input impedance, output impedance and overall gain.
- Be able to analyze cascaded configurations with FETs and/or BJT amplifiers.

8.1 INTRODUCTION

Field-effect transistor amplifiers provide an excellent voltage gain with the added feature of a high input impedance. They are also low-power-consumption configurations with good frequency range and minimal size and weight. JFETs, depletion MOSFETs, and MESFETs can be used to design amplifiers having similar voltage gains. The depletion MOSFET (MESFET) circuit, however, has a much higher input impedance than a similar JFET configuration.

Whereas a BJT device controls a large output (collector) current by means of a relatively small input (base) current, the FET device controls an output (drain) current by means of a small input (gate-voltage) voltage. In general, therefore, the BJT is a *current-controlled* device and the FET is a *voltage-controlled* device. In both cases, however, note that the output current is the controlled variable. Because of the high input characteristic of FETs, the ac equivalent model is somewhat simpler than that employed for BJTs. Whereas the BJT has an amplification factor, β (beta), the FET has a transconductance factor, g_m.

The FET can be used as a linear amplifier or as a digital device in logic circuits. In fact, the enhancement MOSFET is quite popular in digital circuitry, especially in CMOS circuits that require very low power consumption. FET devices are also widely used in high-frequency applications and in buffering (interfacing) applications. Table 8.1 in Section 8.13 provides a summary of FET small-signal amplifier circuits and related formulas.

Although the common-source configuration is the most popular one, providing an inverted, amplified signal, one also finds common-drain (source-follower) circuits providing unity gain with no inversion and common-gate circuits providing gain with no inversion. As with BJT amplifiers, the important circuit features described in this chapter include voltage gain, input impedance, and output impedance. Due to the very high input impedance, the input current is generally assumed to be 0 μA and the current gain is an undefined quantity.

Whereas the voltage gain of an FET amplifier is generally less than that obtained using a BJT amplifier, the FET amplifier provides a much higher input impedance than that of a BJT configuration. Output impedance values are comparable for both BJT and FET circuits.

FET ac amplifier networks can also be analyzed using computer software. Using PSpice or Multisim, one can perform a dc analysis to obtain the circuit bias conditions and an ac analysis to determine the small-signal voltage gain. Using PSpice transistor models, one can analyze the circuit using specific transistor models. On the other hand, one can develop a program using a language such as C++ that can perform both the dc and ac analyses and provide the results in a very special format.

8.2 JFET SMALL-SIGNAL MODEL

The ac analysis of a JFET configuration requires that a small-signal ac model for the JFET be developed. A major component of the ac model will reflect the fact that an ac voltage applied to the input gate-to-source terminals will control the level of current from drain to source.

The gate-to-source voltage controls the drain-to-source (channel) current of a JFET.

Recall from Chapter 7 that a dc gate-to-source voltage controls the level of dc drain current through a relationship known as Shockley's equation: $I_D = I_{DSS}(1 - V_{GS}/V_P)^2$. The *change* in drain current that will result from a *change* in gate-to-source voltage can be determined using the transconductance factor g_m in the following manner:

$$\boxed{\Delta I_D = g_m \, \Delta V_{GS}} \tag{8.1}$$

The prefix *trans-* in the terminology applied to g_m reveals that it establishes a relationship between an output and an input quantity. The root word *conductance* was chosen because g_m is determined by a current-to-voltage ratio similar to the ratio that defines the conductance of a resistor, $G = 1/R = I/V$.

Solving for g_m in Eq. (8.1), we have

$$\boxed{g_m = \frac{\Delta I_D}{\Delta V_{GS}}} \tag{8.2}$$

Graphical Determination of g_m

If we now examine the transfer characteristics of Fig. 8.1, we find that g_m is actually the slope of the characteristics at the point of operation. That is,

$$\boxed{g_m = m = \frac{\Delta y}{\Delta x} = \frac{\Delta I_D}{\Delta V_{GS}}} \tag{8.3}$$

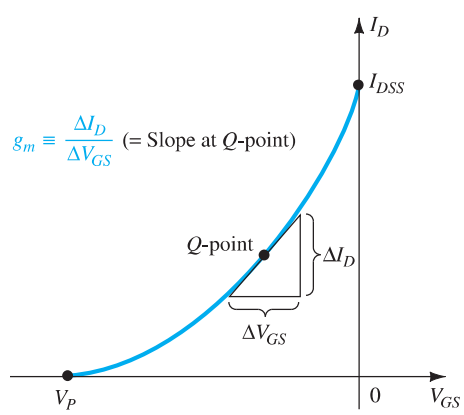

FIG. 8.1
Definition of g_m using transfer characteristic.

Following the curvature of the transfer characteristics, it is reasonably clear that the slope and, therefore, g_m increase as we progress from V_P to I_{DSS}. In other words, as V_{GS} approaches 0 V, the magnitude of g_m increases.

Equation (8.2) reveals that g_m can be determined at any Q-point on the transfer characteristics by simply choosing a finite increment in V_{GS} (or in I_D) about the Q-point and then finding the corresponding change in I_D (or V_{GS}, respectively). The resulting changes in each quantity are then substituted in Eq. (8.2) to determine g_m.

EXAMPLE 8.1 Determine the magnitude of g_m for a JFET with $I_{DSS} = 8$ mA and $V_P = -4$ Vat the following dc bias points:

a. $V_{GS} = -0.5$ V.
b. $V_{GS} = -1.5$ V.
c. $V_{GS} = -2.5$ V.

Solution: The transfer characteristics are generated as Fig. 8.2 using the procedure defined in Chapter 7. Each operating point is then identified and a tangent line is drawn at each point to best reflect the slope of the transfer curve in this region. An appropriate increment is then chosen for V_{GS} to reflect a variation to either side of each Q-point. Equation (8.2) is then applied to determine g_m.

a. $$g_m = \frac{\Delta I_D}{\Delta V_{GS}} \cong \frac{2.1\text{ mA}}{0.6\text{ V}} = \mathbf{3.5\ mS}$$

b. $$g_m = \frac{\Delta I_D}{\Delta V_{GS}} \cong \frac{1.8\text{ mA}}{0.7\text{ V}} \cong \mathbf{2.57\ mS}$$

c. $$g_m = \frac{\Delta I_D}{\Delta V_{GS}} = \frac{1.5\text{ mA}}{1.0\text{ V}} = \mathbf{1.5\ mS}$$

Note the decrease in g_m as V_{GS} approaches V_P.

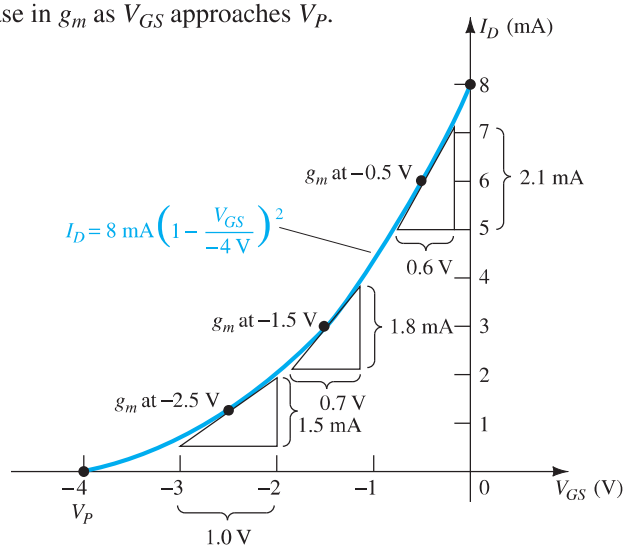

FIG. 8.2
Calculating g_m at various bias points.

Mathematical Definition of g_m

The graphical procedure just described is limited by the accuracy of the transfer plot and the care with which the changes in each quantity can be determined. Naturally, the larger the graph, the better is the accuracy, but this can then become a cumbersome problem. An alternative approach to determining g_m employs the approach used to find the ac resistance of a diode in Chapter 1, where it was stated that:

The derivative of a function at a point is equal to the slope of the tangent line drawn at that point.

If we therefore take the derivative of I_D with respect to V_{GS} (differential calculus) using Shockley's equation, we can derive an equation for g_m as follows:

$$g_m = \left.\frac{dI_D}{dV_{GS}}\right|_{Q\text{-pt.}} = \frac{d}{dV_{GS}}\left[I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2\right]$$

$$= I_{DSS}\frac{d}{dV_{GS}}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = 2I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]\frac{d}{dV_{GS}}\left(1 - \frac{V_{GS}}{V_P}\right)$$

$$= 2I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]\left[\frac{d}{dV_{GS}}(1) - \frac{1}{V_P}\frac{dV_{GS}}{dV_{GS}}\right] = 2I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]\left[0 - \frac{1}{V_P}\right]$$

and

$$\boxed{g_m = \frac{2I_{DSS}}{|V_P|}\left[1 - \frac{V_{GS}}{V_P}\right]} \tag{8.4}$$

where $|V_P|$ denotes magnitude only, to ensure a positive value for g_m.

It was mentioned earlier that the slope of the transfer curve is a maximum at $V_{GS} = 0$ V. Plugging in $V_{GS} = 0$ V into Eq. (8.4) results in the following equation for the maximum value of g_m for a JFET in which I_{DSS} and V_P have been specified:

$$g_m = \frac{2I_{DSS}}{|V_P|}\left[1 - \frac{0}{V_P}\right]$$

and

$$\boxed{g_{m0} = \frac{2I_{DSS}}{|V_P|}} \tag{8.5}$$

where the added subscript 0 reminds us that it is the value of g_m when $V_{GS} = 0$ V. Equation (8.4) then becomes

$$\boxed{g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_P}\right]} \tag{8.6}$$

EXAMPLE 8.2 For the JFET having the transfer characteristics of Example 8.1:

a. Find the maximum value of g_m.
b. Find the value of g_m at each operating point of Example 8.1 using Eq. (8.6) and compare with the graphical results.

Solution:

a. $g_{m0} = \dfrac{2I_{DSS}}{|V_P|} = \dfrac{2(8\text{ mA})}{4\text{ V}} = \mathbf{4\ mS}$ (maximum possible value of g_m)

b. At $V_{GS} = -0.5$ V,

$$g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_P}\right] = 4\text{ mS}\left[1 - \frac{-0.5\text{ V}}{-4\text{ V}}\right] = \mathbf{3.5\ mS}$$ (vs. 3.5 mS graphically)

At $V_{GS} = -1.5$ V,

$$g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_P}\right] = 4\text{ mS}\left[1 - \frac{-1.5\text{ V}}{-4\text{ V}}\right] = \mathbf{2.5\ mS}$$ (vs. 2.57 mS graphically)

At $V_{GS} = -2.5$ V,

$$g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_P}\right] = 4\text{ mS}\left[1 - \frac{-2.5\text{ V}}{-4\text{ V}}\right] = \mathbf{1.5\ mS}$$ (vs. 1.5 mS graphically)

The results of Example 8.2 are certainly sufficiently close to validate Eq. (8.4) through (8.6) for future use when g_m is required.

On specification sheets, g_m is often provided as g_{fs} or y_{fs}, where y indicates it is part of an admittance equivalent circuit. The f signifies *f*orward transfer conductance, and the s indicates that it is connected to the *s*ource terminal.

In equation form,

$$g_m = g_{fs} = y_{fs} \tag{8.7}$$

For the JFET of Fig. 6.20, g_{fs} ranges from 1000 μS to 5000 μS, or 1 mS to 5 mS.

Plotting g_m versus V_{GS}

Since the factor $\left(1 - \frac{V_{GS}}{V_P}\right)$ of Eq. (8.6) is less than 1 for any value of V_{GS} other than 0 V, the magnitude of g_m will decrease as V_{GS} approaches V_P and the ratio $\frac{V_{GS}}{V_P}$ increases in magnitude. At $V_{GS} = V_P$, $g_m = g_{m0}(1 - 1) = 0$. Equation (8.6) defines a straight line with a minimum value of 0 and a maximum value of g_m, as shown by the plot of Fig. 8.3.

In general, therefore

the maximum value of g_m occurs where $V_{GS} = 0$ V and the minimum value at $V_{GS} = V_P$. The more negative the value of V_{GS} the less the value of g_m.

Figure 8.3 also shows that when V_{GS} is one-half the pinch-off value, g_m is one-half the maximum value.

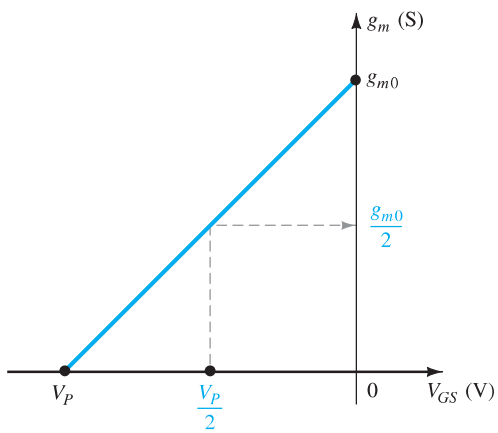

FIG. 8.3
Plot of g_m versus V_{GS}.

EXAMPLE 8.3 Plot g_m versus V_{GS} for the JFET of Examples 8.1 and 8.2.

Solution: Note Fig. 8.4.

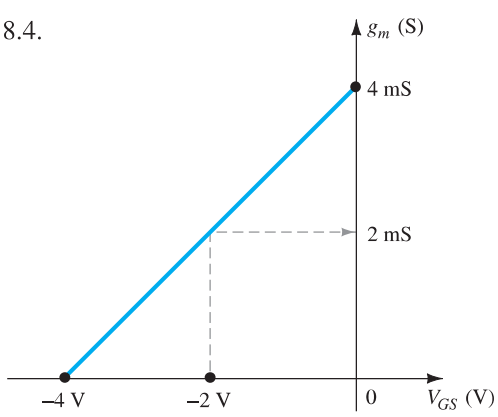

FIG. 8.4
Plot of g_m versus V_{GS} for a JFET with I_{DSS} = 8 mA and $V_P = -4$ V.

Effect of I_D on g_m

A mathematical relationship between g_m and the dc bias current I_D can be derived by noting that Shockley's equation can be written in the following form:

$$\boxed{1 - \frac{V_{GS}}{V_P} = \sqrt{\frac{I_D}{I_{DSS}}}} \tag{8.8}$$

Substituting Eq. (8.8) into Eq. (8.6) results in

$$\boxed{g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_P}\right) = g_{m0}\sqrt{\frac{I_D}{I_{DSS}}}} \tag{8.9}$$

Using Eq. (8.9) to determine g_m for a few specific values of I_D, we obtain the following results:

a. If $I_D = I_{DSS}$,

$$g_m = g_{m0}\sqrt{\frac{I_{DSS}}{I_{DSS}}} = \mathbf{g_{m0}}$$

b. If $I_D = I_{DSS}/2$,

$$g_m = g_{m0}\sqrt{\frac{I_{DSS}/2}{I_{DSS}}} = \mathbf{0.707g_{m0}}$$

c. If $I_D = I_{DSS}/4$,

$$g_m = g_{m0}\sqrt{\frac{I_{DSS}/4}{I_{DSS}}} = \frac{g_{m0}}{2} = \mathbf{0.5g_{m0}}$$

EXAMPLE 8.4 Plot g_m versus I_D for the JFET of Examples 8.1 through 8.3.

Solution: See Fig. 8.5.

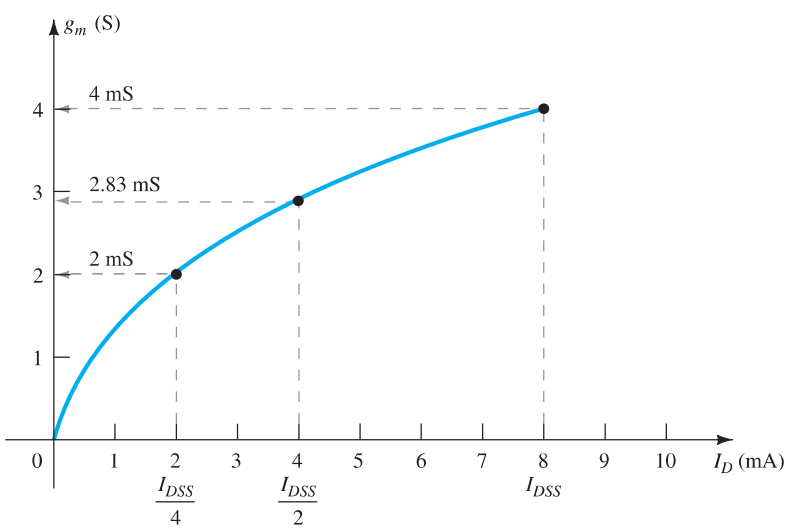

FIG. 8.5
Plot of g_m versus I_D for a JFET with $I_{DSS} = 8$ mA and $V_{GS} = -4$ V.

The plots of Examples 8.3 and 8.4 clearly reveal that

the highest values of g_m are obtained when V_{GS} approaches 0 V and I_D approaches its maximum value of I_{DSS}.

JFET Input Impedance Z_i

The input impedance of all commercially available JFETs is sufficiently large to assume that the input terminals approximate an open circuit. In equation form,

$$Z_i\,(\text{JFET}) = \infty\,\Omega \tag{8.10}$$

For a JFET a practical value of $10^9\ \Omega$ (1000 MΩ) is typical, whereas a value of $10^{12}\ \Omega$ to $10^{15}\ \Omega$ is typical for MOSFETs and MESFETs.

JFET Output Impedance Z_o

The output impedance of JFETs is similar in magnitude to that of conventional BJTs. On JFET specification sheets, the output impedance will typically appear as g_{os} or y_{os} with the units of μS. The parameter y_{os} is a component of an *admittance equivalent circuit*, with the subscript *o* signifying an *o*utput network parameter and *s* the terminal (*s*ource) to which it is attached in the model. For the JFET of Fig. 6.20, g_{os} has a range of 10 μS to 50 μS or 20 kΩ ($R = 1/G = 1/50\ \mu$S) to 100 kΩ ($R = 1/G = 1/10\ \mu$S).

In equation form,

$$Z_o\,(\text{JFET}) = r_d = \frac{1}{g_{os}} = \frac{1}{y_{os}} \tag{8.11}$$

The output impedance is defined on the characteristics of Fig. 8.6 as the slope of the horizontal characteristic curve at the point of operation. The more horizontal the curve, the greater is the output impedance. If it is perfectly horizontal, the ideal situation is on hand with the output impedance being infinite (an open circuit)—an often applied approximation.

In equation form,

$$r_d = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS}=\text{constant}} \tag{8.12}$$

Note the requirement when applying Eq. (8.12) that the voltage V_{GS} remain constant when r_d is determined. This is accomplished by drawing a straight line approximating the V_{GS} line at the point of operation. A ΔV_{DS} or ΔI_D is then chosen and the other quantity measured off for use in the equation.

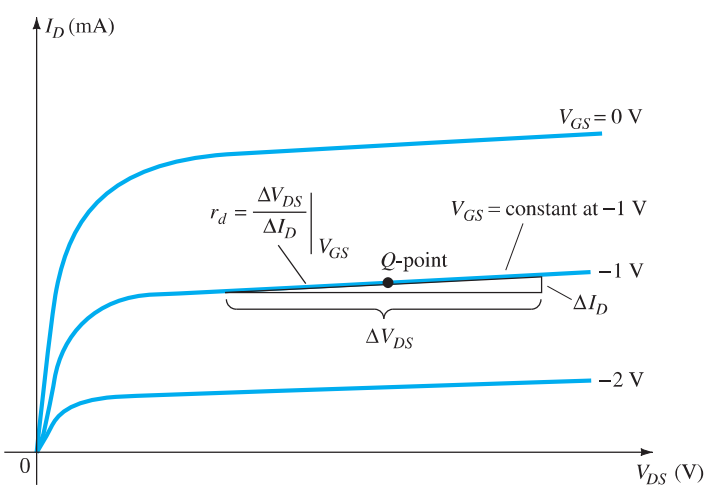

FIG. 8.6
Definition of r_d using JFET drain characteristics.

EXAMPLE 8.5 Determine the output impedance for the JFET of Fig. 8.7 for $V_{GS} = 0$ V and $V_{GS} = -2$ V at $V_{DS} = 8$ V.

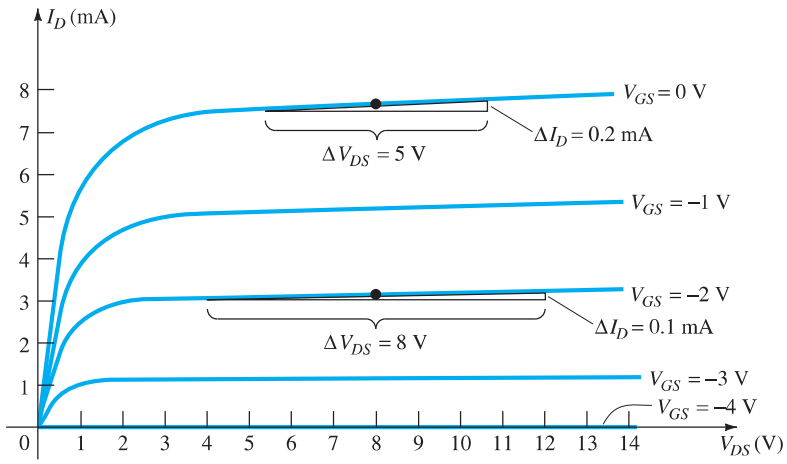

FIG. 8.7
Drain characteristics used to calculate r_d in Example 8.5.

Solution: For $V_{GS} = 0$ V, a tangent line is drawn and ΔV_{DS} is chosen as 5 V, resulting in a ΔI_D of 0.2 mA. Substituting into Eq. (8.12), we find

$$r_d = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS}=0\text{ V}} = \frac{5\text{ V}}{0.2\text{ mA}} = \mathbf{25\ k\Omega}$$

For $V_{GS} = -2$ V, a tangent line is drawn and ΔV_{DS} is chosen as 8 V, resulting in a ΔI_D of 0.1 mA. Substituting into Eq. (8.12), we find

$$r_d = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS}=-2\text{ V}} = \frac{8\text{ V}}{0.1\text{ mA}} = \mathbf{80\ k\Omega}$$

which shows that r_d does change from one operating region to another, with lower values typically occurring at lower levels of V_{GS} (closer to 0 V).

JFET AC Equivalent Circuit

Now that the important parameters of an ac equivalent circuit have been introduced and discussed, a model for the JFET transistor in the ac domain can be constructed. The control of I_d by V_{gs} is included as a current source $g_m V_{gs}$ connected from drain to source as shown in Fig. 8.8. The current source has its arrow pointing from drain to source to establish a 180° phase shift between output and input voltages as will occur in actual operation.

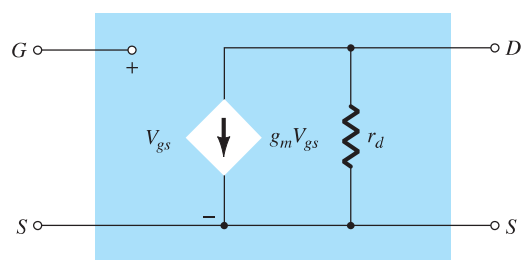

FIG. 8.8
JFET ac equivalent circuit.

The input impedance is represented by the open circuit at the input terminals and the output impedance by the resistor r_d from drain to source. Note that the gate-to-source voltage is now represented by V_{gs} (lowercase subscripts) to distinguish it from dc levels. In addition, note that the source is common to both input and output circuits, whereas the gate and drain terminals are only in "touch" through the controlled current source $g_m V_{gs}$.

In situations where r_d is ignored (assumed sufficiently large in relation to other elements of the network to be approximated by an open circuit), the equivalent circuit is simply a current source whose magnitude is controlled by the signal V_{gs} and parameter g_m—clearly a voltage-controlled current source.

EXAMPLE 8.6 Given $g_{fs} = 3.8$ mS and $g_{os} = 20\ \mu$S, sketch the FET ac equivalent model.

Solution:

$$g_m = g_{fs} = 3.8 \text{ mS} \qquad \text{and} \qquad r_d = \frac{1}{g_{os}} = \frac{1}{20\ \mu\text{S}} = 50\ \text{k}\Omega$$

resulting in the ac equivalent model of Fig. 8.9.

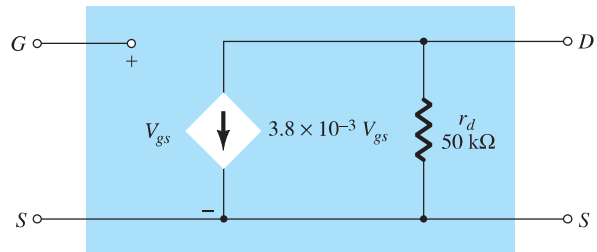

FIG. 8.9
JFET ac equivalent model for Example 8.6.

8.3 FIXED-BIAS CONFIGURATION

Now that the JFET equivalent circuit has been defined, a number of fundamental JFET small-signal configurations are investigated. The approach parallels the ac analysis of BJT amplifiers with a determination of the important parameters of Z_i, Z_o, and A_v for each configuration.

The *fixed-bias* configuration of Fig. 8.10 includes the coupling capacitors C_1 and C_2, which isolate the dc biasing arrangement from the applied signal and load; they act as short-circuit equivalents for the ac analysis.

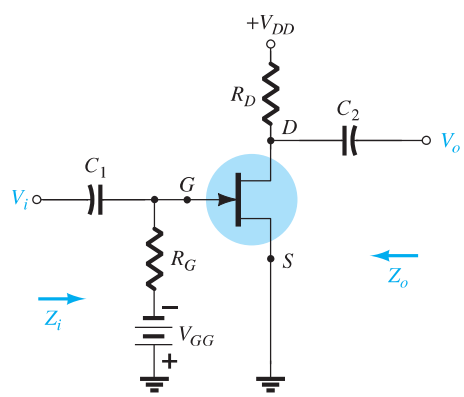

FIG. 8.10
JFET fixed-bias configuration.

Once the levels of g_m and r_d are determined from the dc biasing arrangement, specification sheet, or characteristics, the ac equivalent model can be substituted between the appropriate terminals as shown in Fig. 8.11. Note that both capacitors have the short-circuit equivalent because the reactance $X_C = 1/(2\pi fC)$ is sufficiently small compared to other impedance levels of the network, and the dc batteries V_{GG} and V_{DD} are set to 0 V by a short-circuit equivalent.

The network of Fig. 8.11 is then carefully redrawn as shown in Fig. 8.12. Note the defined polarity of V_{gs}, which defines the direction of $g_m V_{gs}$. If V_{gs} is negative, the direction of the current source reverses. The applied signal is represented by V_i and the output signal across $R_D \| r_d$ by V_o.

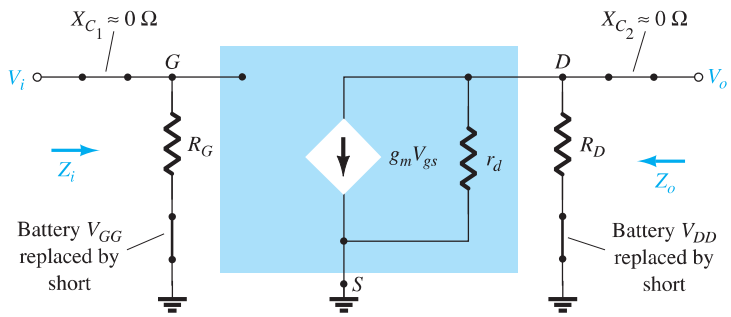

FIG. 8.11
Substituting the JFET ac equivalent circuit unit into the network of Fig. 8.10.

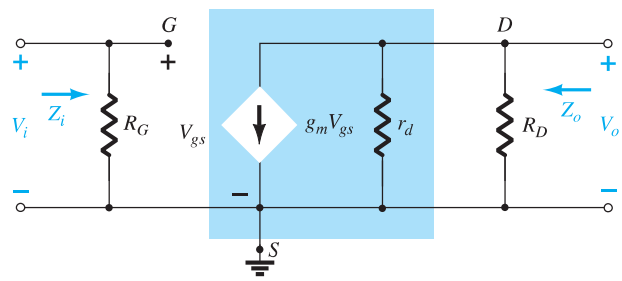

FIG. 8.12
Redrawn network of Fig. 8.11.

Z_i Figure 8.12 clearly reveals that

$$\boxed{Z_i = R_G} \tag{8.13}$$

because of the infinite input impedance at the input terminals of the JFET.

Z_o Setting $V_i = 0$ V as required by the definition of Z_o will establish V_{gs} as 0 V also. The result is $g_m V_{gs} = 0$ mA, and the current source can be replaced by an open-circuit equivalent as shown in Fig. 8.13. The output impedance is

$$\boxed{Z_o = R_D \| r_d} \tag{8.14}$$

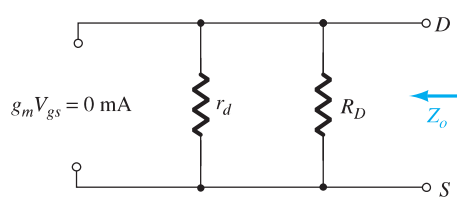

FIG. 8.13
Determining Z_o.

If the resistance r_d is sufficiently large (at least 10:1) compared to R_D, the approximation $r_d \| R_D \cong R_D$ can often be applied and

$$\boxed{Z_o \cong R_D}_{\ r_d \geq 10R_D} \tag{8.15}$$

A_v Solving for V_o in Fig. 8.12, we find

$$V_o = -g_m V_{gs}(r_d \| R_D)$$

but

$$V_{gs} = V_i$$

and

$$V_o = -g_m V_i (r_d \| R_D)$$

so that

$$A_v = \frac{V_o}{V_i} = -g_m(r_d \| R_D) \tag{8.16}$$

If $r_d \geq 10R_D$,

$$A_v = \frac{V_o}{V_i} = -g_m R_D \quad r_d \geq 10R_D \tag{8.17}$$

Phase Relationship The negative sign in the resulting equation for A_v clearly reveals a phase shift of 180° between input and output voltages.

EXAMPLE 8.7 The fixed-bias configuration of Example 7.1 had an operating point defined by $V_{GS_Q} = -2$ V and $I_{D_Q} = 5.625$ mA, with $I_{DSS} = 10$ mA and $V_P = -8$ V. The network is redrawn as Fig. 8.14 with an applied signal V_i. The value of y_{os} is provided as 40 μS.

a. Determine g_m.
b. Find r_d.
c. Determine Z_i.
d. Calculate Z_o.
e. Determine the voltage gain A_v.
f. Determine A_v ignoring the effects of r_d.

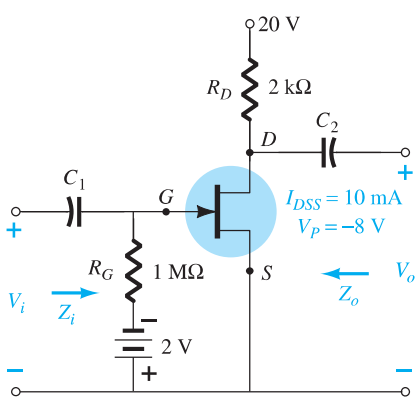

FIG. 8.14
JFET configuration for Example 8.7.

Solution:

a. $g_{m0} = \dfrac{2I_{DSS}}{|V_P|} = \dfrac{2(10\text{ mA})}{8\text{ V}} = 2.5\text{ mS}$

$$g_m = g_{m0}\left(1 - \frac{V_{GS_Q}}{V_P}\right) = 2.5\text{ mS}\left(1 - \frac{(-2\text{ V})}{(-8\text{ V})}\right) = \mathbf{1.88\ mS}$$

b. $r_d = \dfrac{1}{y_{os}} = \dfrac{1}{40\ \mu\text{S}} = \mathbf{25\ k\Omega}$

c. $Z_i = R_G = \mathbf{1\ M\Omega}$

d. $Z_o = R_D \| r_d = 2\text{ k}\Omega \| 25\text{ k}\Omega = \mathbf{1.85\ k\Omega}$

e. $A_v = -g_m(R_D \| r_d) = -(1.88\text{ mS})(1.85\text{ k}\Omega)$
$= \mathbf{-3.48}$

f. $A_v = -g_m R_D = -(1.88\text{ mS})(2\text{ k}\Omega) = \mathbf{-3.76}$

As demonstrated in part (f), a ratio of 25 kΩ:2 kΩ = 12.5:1 between r_d and R_D results in a difference of 8% in the solution.

8.4 SELF-BIAS CONFIGURATION

Bypassed R_S

The fixed-bias configuration has the distinct disadvantage of requiring two dc voltage sources. The *self-bias* configuration of Fig. 8.15 requires only one dc supply to establish the desired operating point.

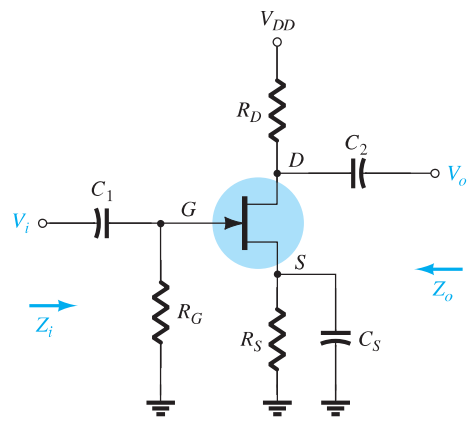

FIG. 8.15
Self-bias JFET configuration.

The capacitor C_S across the source resistance assumes its open-circuit equivalence for dc, allowing R_S to define the operating point. Under ac conditions, the capacitor assumes the short-circuit state and "short circuits" the effects of R_S. If left in the ac, gain will be reduced, as will be shown in the paragraphs to follow.

The JFET equivalent circuit is established in Fig. 8.16 and carefully redrawn in Fig. 8.17.

Since the resulting configuration is the same as appearing in Fig. 8.12, the resulting equations for Z_i, Z_o, and A_v will be the same.

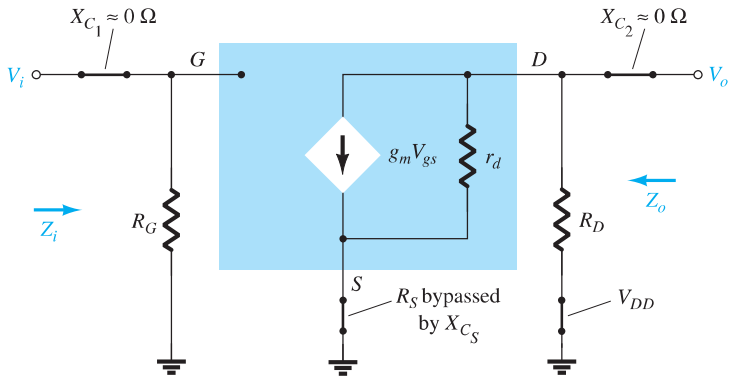

FIG. 8.16
Network of Fig. 8.15 following the substitution of the JFET ac equivalent circuit.

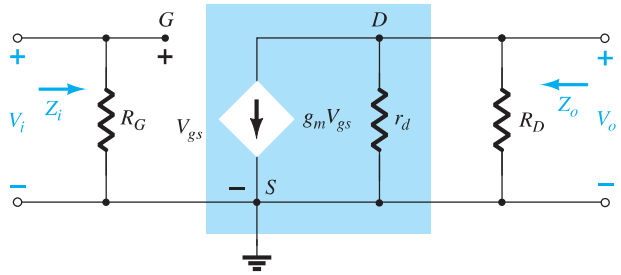

FIG. 8.17
Redrawn network of Fig. 8.16.

Z_i

$$Z_i = R_G \tag{8.18}$$

Z_o

$$Z_o = r_d \| R_D \tag{8.19}$$

If $r_d \geq 10R_D$,

$$Z_o \cong R_D \quad {}_{r_d \geq 10R_D} \tag{8.20}$$

A_v

$$A_v = -g_m(r_d \| R_D) \tag{8.21}$$

If $r_d \geq 10R_D$,

$$A_v = -g_m R_D \quad {}_{r_d \geq 10R_D} \tag{8.22}$$

Phase Relationship The negative sign in the solutions for A_v again indicates a phase shift of 180° between V_i and V_o.

Unbypassed R_S

If C_S is removed from Fig 8.15, the resistor R_S will be part of the ac equivalent circuit as shown in Fig. 8.18. In this case, there is no obvious way to reduce the network to lower its level of complexity. In determining the levels of Z_i, Z_o, and A_v, one must be very careful with notation and defined polarities and direction. Initially, the resistance r_d will be left out of the analysis to form a basis for comparison.

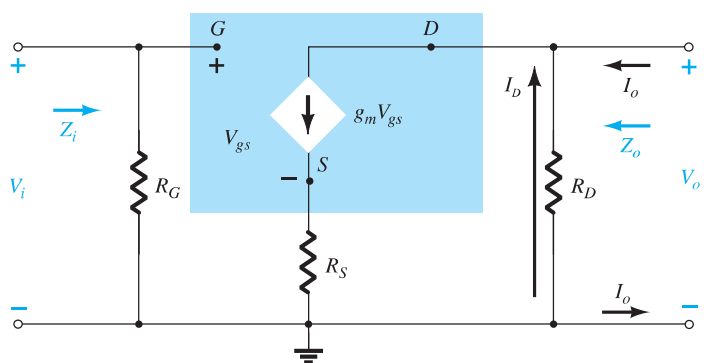

FIG. 8.18
Self-bias JFET configuration including the effects of R_S with $r_d = \infty\Omega$.

Z_i Due to the open-circuit condition between the gate and the output network, the input remains the following:

$$Z_i = R_G \tag{8.23}$$

Z_o The output impedance is defined by

$$Z_o = \left.\frac{V_o}{I_o}\right|_{V_i=0}$$

Setting $V_i = 0$ V in Fig. 8.18 results in the gate terminal being at ground potential (0 V). The voltage across R_G is then 0 V, and R_G has been effectively "shorted out" of the picture.

Applying Kirchhoff's current law results in

$$I_o + I_D = g_m V_{gs}$$

with

$$V_{gs} = -(I_o + I_D)R_S$$

so that $$I_o + I_D = -g_m(I_o + I_D)R_S = -g_m I_o R_S - g_m I_D R_S$$

or $$I_o[1 + g_m R_S] = -I_D[1 + g_m R_S]$$

and $$I_o = -I_D$$ (the controlled current source $g_m V_{gs} = 0$ A for the applied conditions)

Since $$V_o = -I_D R_D$$

then $$V_o = -(-I_o)R_D = I_o R_D$$

and $$\boxed{Z_o = \frac{V_o}{I_o} = R_D}_{r_d = \infty\,\Omega} \qquad \textbf{(8.24)}$$

If r_d is included in the network, the equivalent will appear as shown in Fig. 8.19.

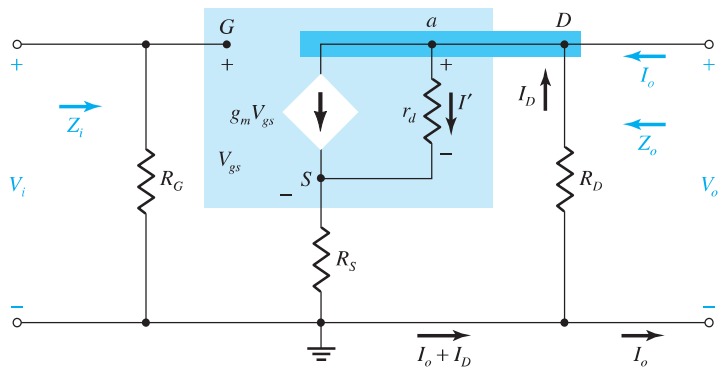

FIG. 8.19
Including the effects of r_d in the self-bias JFET configuration.

Since $$Z_o = \left.\frac{V_o}{I_o}\right|_{V_i = 0\text{ V}} = -\frac{I_D R_D}{I_o}$$

we should try to find an expression for I_o in terms of I_D.

Applying Kirchhoff's current law, we have

$$I_o = g_m V_{gs} + I_{r_d} - I_D$$

but $$V_{r_d} = V_o + V_{gs}$$

and $$I_o = g_m V_{gs} + \frac{V_o + V_{gs}}{r_d} - I_D$$

or $$I_o = \left(g_m + \frac{1}{r_d}\right)V_{gs} - \frac{I_D R_D}{r_d} - I_D \text{ using } V_o = -I_D R_D$$

Now, $$V_{gs} = -(I_D + I_o)R_S$$

so that $$I_o = -\left(g_m + \frac{1}{r_d}\right)(I_D + I_o)R_S - \frac{I_D R_D}{r_d} - I_D$$

with the result that $$I_o\left[1 + g_m R_S + \frac{R_S}{r_d}\right] = -I_D\left[1 + g_m R_S + \frac{R_S}{r_d} + \frac{R_D}{r_d}\right]$$

or $$I_o = \frac{-I_D\left[1 + g_m R_S + \dfrac{R_S}{r_d} + \dfrac{R_D}{r_d}\right]}{1 + g_m R_S + \dfrac{R_S}{r_d}}$$

and $$Z_o = \frac{V_o}{I_o} = \frac{-I_D R_D}{\dfrac{-I_D\left(1 + g_m R_S + \dfrac{R_S}{r_d} + \dfrac{R_D}{r_d}\right)}{1 + g_m R_S + \dfrac{R_S}{r_d}}}$$

and finally,

$$\boxed{Z_o = \frac{\left[1 + g_m R_S + \dfrac{R_S}{r_d}\right]}{\left[1 + g_m R_S + \dfrac{R_S}{r_d} + \dfrac{R_D}{r_d}\right]} R_D} \tag{8.25a}$$

For $r_d \geq 10R_D$,

$$\left(1 + g_m R_S + \frac{R_S}{r_d}\right) \gg \frac{R_D}{r_d}$$

and

$$1 + g_m R_S + \frac{R_S}{r_d} + \frac{R_D}{r_d} \cong 1 + g_m R_S + \frac{R_S}{r_d}$$

resulting in

$$\boxed{Z_o \cong R_D}_{\;r_d \geq 10R_D} \tag{8.25b}$$

A_v For the network of Fig. 8.19, application of Kirchhoff's voltage law to the input circuit results in

$$V_i - V_{gs} - V_{R_S} = 0$$
$$V_{gs} = V_i - I_D R_S$$

The voltage across r_d using Kirchhoff's voltage law is

$$V_{r_d} = V_o - V_{R_S}$$

and

$$I' = \frac{V_{r_d}}{r_d} = \frac{V_o - V_{R_S}}{r_d}$$

so that application of Kirchhoff's current law results in

$$I_D = g_m V_{gs} + \frac{V_o - V_{R_S}}{r_d}$$

Substituting for V_{gs} from above and substituting for V_o and V_{R_S}, we have

$$I_D = g_m[V_i - I_D R_S] + \frac{(-I_D R_D) - (I_D R_S)}{r_d}$$

so that

$$I_D\left[1 + g_m R_S + \frac{R_D + R_S}{r_d}\right] = g_m V_i$$

or

$$I_D = \frac{g_m V_i}{1 + g_m R_S + \dfrac{R_D + R_S}{r_d}}$$

The output voltage is then

$$V_o = -I_D R_D = -\frac{g_m R_D V_i}{1 + g_m R_S + \dfrac{R_D + R_S}{r_d}}$$

and

$$\boxed{A_v = \frac{V_o}{V_i} = -\frac{g_m R_D}{1 + g_m R_S + \dfrac{R_D + R_S}{r_d}}} \tag{8.26}$$

Again, if $r_d \geq 10(R_D + R_S)$,

$$\boxed{A_v = \frac{V_o}{V_i} \cong -\frac{g_m R_D}{1 + g_m R_S}}_{\;r_d \geq 10(R_D + R_S)} \tag{8.27}$$

Phase Relationship The negative sign in Eq. (8.26) again reveals that a 180° phase shift will exist between V_i and V_o.

EXAMPLE 8.8 The self-bias configuration of Example 7.2 has an operating point defined by $V_{GS_Q} = -2.6$ V and $I_{D_Q} = 2.6$ mA, with $I_{DSS} = 8$ mA and $V_P = -6$ V. The network is redrawn as Fig. 8.20 with an applied signal V_i. The value of g_{os} is given as 20 μS.

a. Determine g_m.
b. Find r_d.
c. Find Z_i.
d. Calculate Z_o with and without the effects of r_d. Compare the results.
e. Calculate A_v with and without the effects of r_d. Compare the results.

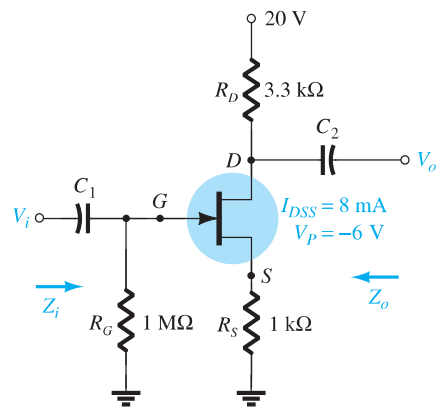

FIG. 8.20
Network for Example 8.8.

Solution:

a. $$g_{m0} = \frac{2I_{DSS}}{|V_P|} = \frac{2(8\text{ mA})}{6\text{ V}} = 2.67\text{ mS}$$

$$g_m = g_{m0}\left(1 - \frac{V_{GS_Q}}{V_P}\right) = 2.67\text{ mS}\left(1 - \frac{(-2.6\text{ V})}{(-6\text{ V})}\right) = \mathbf{1.51\ mS}$$

b. $$r_d = \frac{1}{y_{os}} = \frac{1}{20\ \mu\text{S}} = \mathbf{50\ k\Omega}$$

c. $Z_i = R_G = \mathbf{1\ M\Omega}$

d. With r_d,

$$r_d = 50\text{ k}\Omega > 10R_D = 33\text{ k}\Omega$$

Therefore,

$$Z_o = R_D = \mathbf{3.3\ k\Omega}$$

If $r_d = \infty\,\Omega$,

$$Z_o = R_D = \mathbf{3.3\ k\Omega}$$

e. With r_d,

$$A_v = \frac{-g_mR_D}{1 + g_mR_S + \dfrac{R_D + R_S}{r_d}} = \frac{-(1.51\text{ mS})(3.3\text{ k}\Omega)}{1 + (1.51\text{ mS})(1\text{ k}\Omega) + \dfrac{3.3\text{ k}\Omega + 1\text{ k}\Omega}{50\text{ k}\Omega}}$$

$$= \mathbf{-1.92}$$

With $r_d = \infty\,\Omega$ (open-circuit equivalence),

$$A_v = \frac{-g_mR_D}{1 + g_mR_S} = \frac{-(1.51\text{ mS})(3.3\text{ k}\Omega)}{1 + (1.51\text{ mS})(1\text{ k}\Omega)} = \mathbf{-1.98}$$

As above, the effect of r_d is minimal because the condition $r_d \geq 10(R_D + R_S)$ is satisfied.

Note also that the typical gain of a JFET amplifier is less than that generally encountered for BJTs of similar configurations. Keep in mind, however, that Z_i is magnitudes greater than the typical Z_i of a BJT, which will have a very positive effect on the overall gain of a system.

8.5 VOLTAGE-DIVIDER CONFIGURATION

The popular voltage-divider configuration for BJTs can also be applied to JFETs as demonstrated in Fig. 8.21.

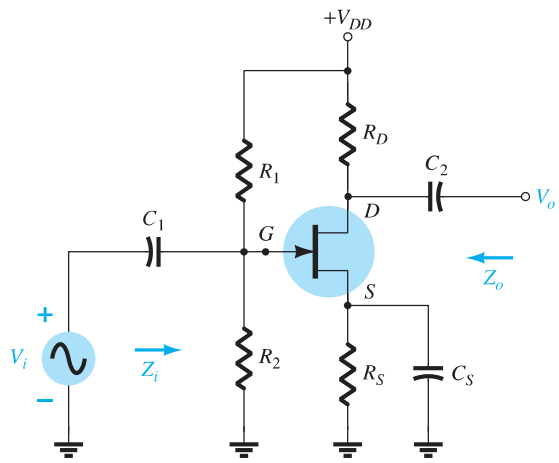

FIG. 8.21
JFET voltage-divider configuration.

Substituting the ac equivalent model for the JFET results in the configuration of Fig. 8.22. Replacing the dc supply V_{DD} by a short-circuit equivalent has grounded one end of R_1 and R_D. Since each network has a common ground, R_1 can be brought down in parallel with R_2 as shown in Fig. 8.23. R_D can also be brought down to ground, but in the output circuit across r_d. The resulting ac equivalent network now has the basic format of some of the networks already analyzed.

Z_i R_1 and R_2 are in parallel with the open-circuit equivalence of the JFET, resulting in

$$\boxed{Z_i = R_1 \| R_2} \tag{8.28}$$

Z_o Setting $V_i = 0$ V sets V_{gs} and $g_m V_{gs}$ to zero, and

$$\boxed{Z_o = r_d \| R_D} \tag{8.29}$$

For $r_d \geq 10R_D$,

$$\boxed{Z_o \cong R_D}_{\,r_d \geq 10R_D} \tag{8.30}$$

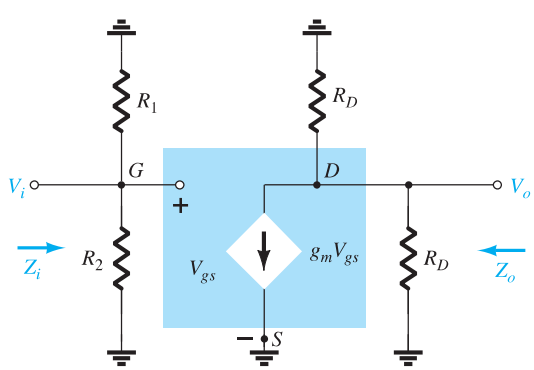

FIG. 8.22
Network of Fig. 8.21 under ac conditions.

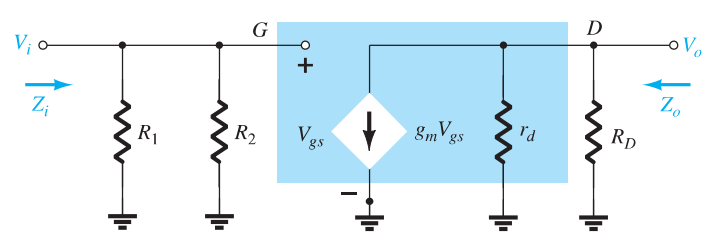

FIG. 8.23
Redrawn network of Fig. 8.22.

A_v

$$V_{gs} = V_i$$

and
$$V_o = -g_m V_{gs}(r_d \| R_D)$$

so that
$$A_v = \frac{V_o}{V_i} = \frac{-g_m V_{gs}(r_d \| R_D)}{V_{gs}}$$

and
$$\boxed{A_v = \frac{V_o}{V_i} = -g_m(r_d \| R_D)} \qquad \textbf{(8.31)}$$

If $r_d \geq 10R_D$,
$$\boxed{A_v = \frac{V_o}{V_i} \cong -g_m R_D}_{\,r_d \geq 10R_D} \qquad \textbf{(8.32)}$$

Note that the equations for Z_o and A_v are the same as obtained for the fixed-bias and self-bias (with bypassed R_S) configurations. The only difference is the equation for Z_i, which is now sensitive to the parallel combination of R_1 and R_2.

8.6 COMMON-GATE CONFIGURATION

The last JFET configuration to be analyzed in detail is the common-gate configuration of Fig. 8.24, which parallels the common-base configuration employed with BJT transistors.

Substituting the JFET equivalent circuit results in Fig. 8.25. Note the continuing requirement that the controlled source $g_m V_{gs}$ be connected from drain to source with r_d in parallel. The isolation between input and output circuits has obviously been lost since the gate terminal is now connected to the common ground of the network and the controlled current source is connected directly from drain to source. In addition, the resistor connected between input terminals is no longer R_G, but the resistor R_S connected from source to ground. Note also the location of the controlling voltage V_{gs} and the fact that it appears directly across the resistor R_S.

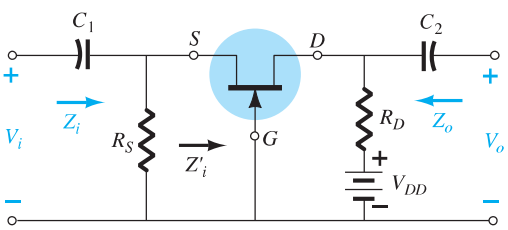

FIG. 8.24
JFET common-gate configuration.

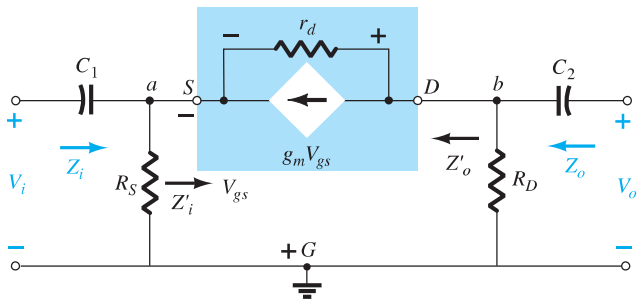

FIG. 8.25
Network of Fig. 8.24 following substitution of JFET ac equivalent model.

Z_i The resistor R_S is directly across the terminals defining Z_i. Let us therefore find the impedance Z_i' of Fig. 8.24, which will simply be in parallel with R_S when Z_i is defined.

The network of interest is redrawn as Fig. 8.26. The voltage $V' = -V_{gs}$. Applying Kirchhoff's voltage law around the output perimeter of the network results in

$$V' - V_{r_d} - V_{R_D} = 0$$

and
$$V_{r_d} = V' - V_{R_D} = V' - I'R_D$$

Applying Kirchhoff's current law at node a results in

$$I' + g_m V_{gs} = I_{r_d}$$

and
$$I' = I_{r_d} - g_m V_{gs} = \frac{(V' - I'R_D)}{r_d} - g_m V_{gs}$$

or
$$I' = \frac{V'}{r_d} - \frac{I'R_D}{r_d} - g_m[-V']$$

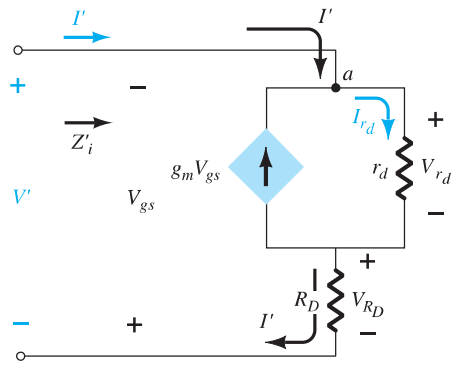

FIG. 8.26
Determining Z_i' for the network of Fig. 8.24.

so that
$$I'\left[1 + \frac{R_D}{r_d}\right] = V'\left[\frac{1}{r_d} + g_m\right]$$

and
$$\boxed{Z_i' = \frac{V'}{I'} = \frac{\left[1 + \dfrac{R_D}{r_d}\right]}{\left[g_m + \dfrac{1}{r_d}\right]}} \qquad \textbf{(8.33)}$$

or
$$Z_i' = \frac{V'}{I'} = \frac{r_d + R_D}{1 + g_m r_d}$$

and
$$Z_i = R_S \| Z_i'$$

which results in
$$\boxed{Z_i = R_S \left\| \left[\frac{r_d + R_D}{1 + g_m r_d}\right]\right.} \qquad \textbf{(8.34)}$$

If $r_d \geq 10R_D$, Eq. (8.33) permits the following approximation since $R_D/r_d \ll 1$ and $1/r_d \ll g_m$:

$$Z_i' = \frac{\left[1 + \dfrac{R_D}{r_d}\right]}{\left[g_m + \dfrac{1}{r_d}\right]} \cong \frac{1}{g_m}$$

and
$$\boxed{Z_i \cong R_S \| 1/g_m}_{\;r_d \geq 10R_D} \qquad \textbf{(8.35)}$$

Z_o Substituting $V_i = 0$ V in Fig. 8.25 will "short-out" the effects of R_S and set V_{gs} to 0 V. The result is $g_mV_{gs} = 0$, and r_d will be in parallel with R_D. Therefore,

$$\boxed{Z_o = R_D \| r_d} \qquad \textbf{(8.36)}$$

For $r_d \geq 10R_D$,

$$\boxed{Z_o \cong R_D}_{\;r_d \geq 10R_D} \qquad \textbf{(8.37)}$$

A_v Figure 8.25 reveals that

$$V_i = -V_{gs}$$

and
$$V_o = I_D R_D$$

The voltage across r_d is

$$V_{r_d} = V_o - V_i$$

and
$$I_{r_d} = \frac{V_o - V_i}{r_d}$$

Applying Kirchhoff's current law at node b in Fig. 8.25 results in

$$I_{r_d} + I_D + g_m V_{gs} = 0$$

and
$$I_D = -I_{r_d} - g_m V_{gs}$$
$$= -\left[\frac{V_o - V_i}{r_d}\right] - g_m[-V_i]$$
$$I_D = \frac{V_i - V_o}{r_d} + g_m V_i$$

so that
$$V_o = I_D R_D = \left[\frac{V_i - V_o}{r_d} + g_m V_i\right] R_D$$
$$= \frac{V_i R_D}{r_d} - \frac{V_o R_D}{r_d} + g_m$$

and
$$V_o\left[1 + \frac{R_D}{r_d}\right] = V_i\left[\frac{R_D}{r_d} + g_m R_D\right]$$

with
$$\boxed{A_v = \frac{V_o}{V_i} = \frac{\left[g_m R_D + \dfrac{R_D}{r_d}\right]}{\left[1 + \dfrac{R_D}{r_d}\right]}} \qquad \textbf{(8.38)}$$

For $r_d \geq 10R_D$, the factor R_D/r_d of Eq. (8.38) can be dropped as a good approximation, and

$$\boxed{A_v \cong g_m R_D}_{\,r_d \geq 10R_D} \qquad \textbf{(8.39)}$$

Phase Relationship The fact that A_v is a positive number will result in an *in-phase* relationship between V_o and V_i for the common-gate configuration.

EXAMPLE 8.9 Although the network of Fig. 8.27 may not initially appear to be of the common-gate variety, a close examination will reveal that it has all the characteristics of Fig. 8.24. If $V_{GS_Q} = -2.2$ V and $I_{D_Q} = 2.03$ mA:

a. Determine g_m.
b. Find r_d.
c. Calculate Z_i with and without r_d. Compare results.
d. Find Z_o with and without r_d. Compare results.
e. Determine V_o with and without r_d. Compare results.

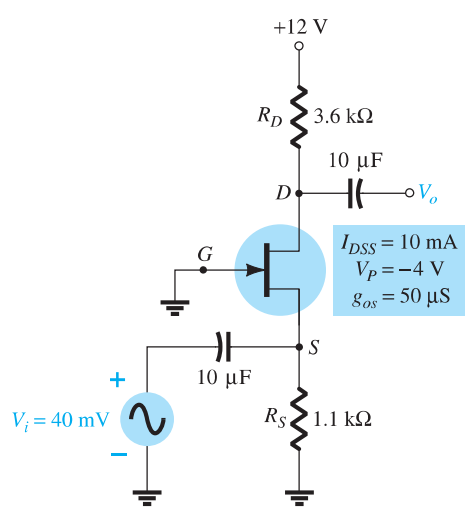

FIG. 8.27
Network for Example 8.9.

Solution:

a. $g_{m0} = \dfrac{2I_{DSS}}{|V_P|} = \dfrac{2(10\text{ mA})}{4\text{ V}} = 5\text{ mS}$

$$g_m = g_{m0}\left(1 - \frac{V_{GS_Q}}{V_P}\right) = 5\text{ mS}\left(1 - \frac{(-2.2\text{ V})}{(-4\text{ V})}\right) = \mathbf{2.25\text{ mS}}$$

b. $r_d = \dfrac{1}{g_{os}} = \dfrac{1}{50\ \mu\text{S}} = \mathbf{20\text{ k}\Omega}$

c. With r_d,

$$Z_i = R_S \| \left[\frac{r_d + R_D}{1 + g_m r_d}\right] = 1.1\text{ k}\Omega \| \left[\frac{20\text{ k}\Omega + 3.6\text{ k}\Omega}{1 + (2.25\text{ mS})(20\text{ k}\Omega)}\right]$$
$$= 1.1\text{ k}\Omega \| 0.51\text{ k}\Omega = \mathbf{0.35\text{ k}\Omega}$$

Without r_d,

$$Z_i = R_S \| 1/g_m = 1.1\text{ k}\Omega \| 1/2.25\text{ ms} = 1.1\text{ k}\Omega \| 0.44\text{ k}\Omega$$
$$= \mathbf{0.31\text{ k}\Omega}$$

Even though the condition $r_d \geq 10R_D$ is not satisfied with $r_d = 20\text{ k}\Omega$ and $10R_D = 36\text{ k}\Omega$, both equations result in essentially the same level of impedance. In this case, $1/g_m$ was the predominant factor.

d. With r_d,

$$Z_o = R_D \| r_d = 3.6\text{ k}\Omega \| 20\text{ k}\Omega = \mathbf{3.05\text{ k}\Omega}$$

Without r_d,

$$Z_o = R_D = \mathbf{3.6\text{ k}\Omega}$$

Again the condition $r_d \geq 10R_D$ is *not* satisfied, but both results are reasonably close. R_D is certainly the predominant factor in this example.

e. With r_d,

$$A_v = \frac{\left[g_m R_D + \dfrac{R_D}{r_d}\right]}{\left[1 + \dfrac{R_D}{r_d}\right]} = \frac{\left[(2.25\text{ mS})(3.6\text{ k}\Omega) + \dfrac{3.6\text{ k}\Omega}{20\text{ k}\Omega}\right]}{\left[1 + \dfrac{3.6\text{ k}\Omega}{20\text{ k}\Omega}\right]}$$
$$= \frac{8.1 + 0.18}{1 + 0.18} = \mathbf{7.02}$$

and $\quad A_v = \dfrac{V_o}{V_i} \Rightarrow V_o = A_v V_i = (7.02)(40\text{ mV}) = \mathbf{280.8\text{ mV}}$

Without r_d,

$$A_v = g_m R_D = (2.25\text{ mS})(3.6\text{ k}\Omega) = \mathbf{8.1}$$

with $\quad V_o = A_v V_i = (8.1)(40\text{ mV}) = \mathbf{324\text{ mV}}$

In this case, the difference is a little more noticeable, but not dramatically so.

Example 8.9 demonstrates that even though the condition $r_d \geq 10R_D$ was not satisfied, the results for the parameters given were not significantly different using the exact and approximate equations. In fact, in most cases, the approximate equations can be used to find a reasonable idea of particular levels with a reduced amount of effort.

8.7 SOURCE-FOLLOWER (COMMON-DRAIN) CONFIGURATION

The JFET equivalent of the BJT emitter-follower configuration is the source-follower configuration of Fig. 8.28. Note that the output is taken off the source terminal and, when the dc supply is replaced by its short-circuit equivalent, the drain is grounded (hence, the terminology *common-drain*).

Substituting the JFET equivalent circuit results in the configuration of Fig. 8.29. The controlled source and the internal output impedance of the JFET are tied to ground at one end and R_S on the other, with V_o across R_S. Since $g_m V_{gs}$, r_d, and R_S are connected to

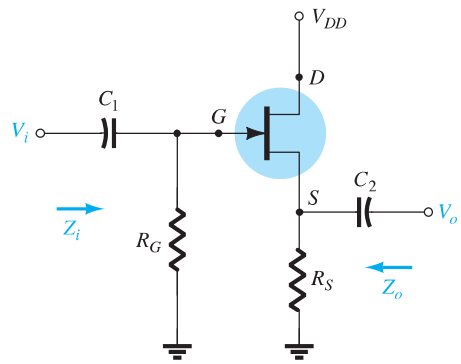

FIG. 8.28
JFET source-follower configuration.

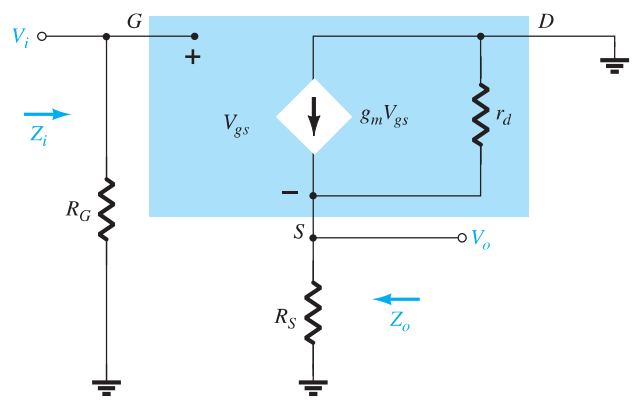

FIG. 8.29
Network of Fig. 8.28 following the substitution of the JFET ac equivalent model.

the same terminal and ground, they can all be placed in parallel as shown in Fig. 8.30. The current source reversed direction, but V_{gs} is still defined between the gate and source terminals.

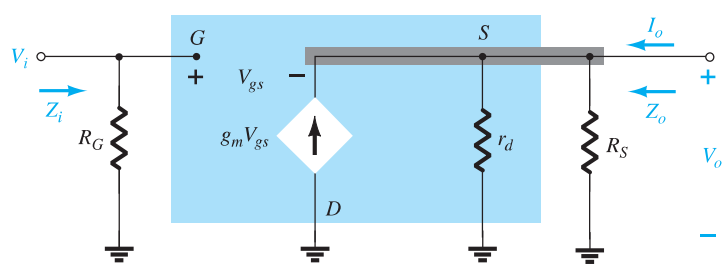

FIG. 8.30
Network of Fig. 8.29 redrawn.

Z_i Figure 8.30 clearly reveals that Z_i is defined by

$$\boxed{Z_i = R_G} \tag{8.40}$$

Z_o Setting $V_i = 0$ V results in the gate terminal being connected directly to the ground as shown in Fig. 8.31.

The fact that V_{gs} and V_o are across the same parallel network results in $V_o = -V_{gs}$.

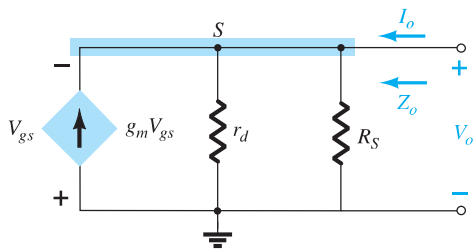

FIG. 8.31
Determining Z_o for the network of Fig. 8.30.

Applying Kirchhoff's current law at node S, we obtain

$$I_o + g_mV_{gs} = I_{r_d} + I_{R_s} = \frac{V_o}{r_d} + \frac{V_o}{R_S}$$

The result is

$$I_o = V_o\left[\frac{1}{r_d} + \frac{1}{R_S}\right] - g_mV_{gs} = V_o\left[\frac{1}{r_d} + \frac{1}{R_S}\right] - g_m[-V_o] = V_o\left[\frac{1}{r_d} + \frac{1}{R_S} + g_m\right]$$

and

$$Z_o = \frac{V_o}{I_o} = \frac{V_o}{V_o\left[\frac{1}{r_d} + \frac{1}{R_S} + g_m\right]} = \frac{1}{\frac{1}{r_d} + \frac{1}{R_S} + g_m} = \frac{1}{\frac{1}{r_d} + \frac{1}{R_S} + \frac{1}{1/g_m}}$$

which has the same format as the total resistance of three parallel resistors. Therefore,

$$\boxed{Z_o = r_d \| R_S \| 1/g_m} \tag{8.41}$$

For $r_d \geq 10\,R_S$,

$$\boxed{Z_o \cong R_S \| 1/g_m}_{\;r_d \geq 10R_S} \tag{8.42}$$

***A*$_v$** The output voltage V_o is determined by

$$V_o = g_mV_{gs}(r_d \| R_S)$$

and applying Kirchhoff's voltage law around the perimeter of the network of Fig. 8.30 results in

$$V_i = V_{gs} + V_o$$

and

$$V_{gs} = V_i - V_o$$

so that

$$V_o = g_m(V_i - V_o)(r_d \| R_S)$$

or

$$V_o = g_mV_i(r_d \| R_S) - g_mV_o(r_d \| R_S)$$

and

$$V_o[1 + g_m(r_d \| R_S)] = g_mV_i(r_d \| R_S)$$

so that

$$\boxed{A_v = \frac{V_o}{V_i} = \frac{g_m(r_d \| R_S)}{1 + g_m(r_d \| R_S)}} \tag{8.43}$$

In the absence of r_d or if $r_d \geq 10\,R_S$,

$$\boxed{A_v = \frac{V_o}{V_i} \cong \frac{g_mR_S}{1 + g_mR_S}}_{\;r_d \geq 10R_S} \tag{8.44}$$

Since the denominator of Eq. (8.43) is larger than the numerator by a factor of one, the gain can never be equal to or greater than one (as encountered for the emitter-follower BJT network).