▶ TABLE 10–2

Power in terms of dBm.

POWER	dBm
32 mW	15 dBm
16 mW	12 dBm
8 mW	9 dBm
4 mW	6 dBm
2 mW	3 dBm
1 mW	0 dBm
0.5 mW	−3 dBm
0.25 mW	−6 dBm
0.125 mW	−9 dBm
0.0625 mW	−12 dBm
0.03125 mW	−15 dBm

power, the dBm can be used. For example, 3 dBm is equivalent to 2 mW because 2 mW is twice the 1 mW reference. 6 dBm is equivalent to 4 mW, and so on. Likewise, −3 dBm is the same as 0.5 mW. Table 10–2 shows several values of power in terms of dBm.

SECTION 10–2 CHECKUP

1. How much increase in actual voltage gain corresponds to +12 dB?
2. Convert a power gain of 25 to decibels.
3. What power corresponds to 0 dBm?

10–3 LOW-FREQUENCY AMPLIFIER RESPONSE

The voltage gain and phase shift of capacitively coupled amplifiers are affected when the signal frequency is below a critical value. At low frequencies, the reactance of the coupling capacitors becomes significant, resulting in a reduction in voltage gain and an increase in phase shift. Frequency responses of both BJT and FET capacitively coupled amplifiers are discussed.

After completing this section, you should be able to

- **Analyze the low-frequency response of an amplifier**
- Analyze a BJT amplifier
  ◆ Calculate the midrange voltage gain ◆ Identify the parts of the amplifier that affect low-frequency response
- Identify and analyze the BJT amplifier's input *RC* circuit
  ◆ Calculate the lower critical frequency and gain roll-off ◆ Sketch a Bode plot ◆ Define *decade* and *octave* ◆ Determine the phase shift
- Identify and analyze the BJT amplifier's output *RC* circuit
  ◆ Calculate the lower critical frequency ◆ Determine the phase shift
- Identify and analyze the BJT amplifier's bypass *RC* circuit
  ◆ Calculate the lower critical frequency ◆ Explain the effect of a swamping resistor
- Analyze a FET amplifier
- Identify and analyze the D-MOSFET amplifier's input *RC* circuit
  ◆ Calculate the lower critical frequency ◆ Determine the phase shift
- Identify and analyze the D-MOSFET amplifier's output *RC* circuit
  ◆ Calculate the lower critical frequency ◆ Determine the phase shift

- Explain the total low-frequency response of an amplifier
  - Illustrate the response with Bode plots
- Simulate the frequency response using Multisim
  - Calculate the lower critical frequency
  - Determine the phase shift

BJT Amplifiers

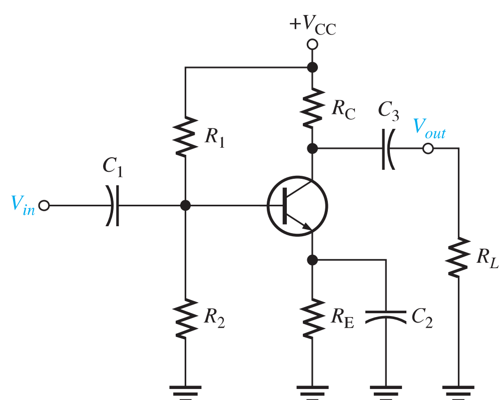
A typical capacitively coupled common-emitter amplifier is shown in Figure 10–8. Assuming that the coupling and bypass capacitors are ideal shorts at the midrange signal frequency, you can determine the midrange voltage gain using Equation 10–5, where $R_c = R_C \| R_L$.

$$\mathbf{A_{v(mid)} = \frac{R_c}{r'_e}}$$

Equation 10–5

If a swamping resistor (R_{E1}) is used, it appears in series with r'_e and the equation becomes

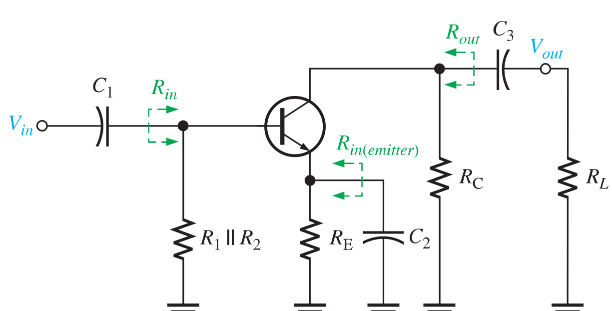
$$A_{v(mid)} = \frac{R_c}{r'_e + R_{E1}}$$



◄ **FIGURE 10–8**

A capacitively coupled BJT amplifier.

The BJT amplifier in Figure 10–8 has three high-pass *RC* circuits that affect its gain as the frequency is reduced below midrange. These are shown in the low-frequency ac equivalent circuit in Figure 10–9. Unlike the ac equivalent circuit used in previous chapters, which represented midrange response ($X_C \cong 0\ \Omega$), the low-frequency equivalent circuit retains the coupling and bypass capacitors because X_C is not small enough to neglect when the signal frequency is sufficiently low.



◄ **FIGURE 10–9**

The low-frequency ac equivalent circuit of the amplifier in Figure 10–8 consists of three high-pass *RC* circuits.

One *RC* circuit is formed by the input coupling capacitor C_1 and the input resistance of the amplifier. The second *RC* circuit is formed by the output coupling capacitor C_3, the resistance looking in at the collector (R_{out}), and the load resistance. The third *RC* circuit that affects the low-frequency response is formed by the emitter-bypass capacitor C_2 and the resistance looking in at the emitter.

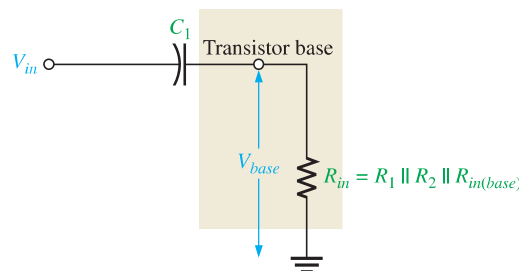
The Input *RC* Circuit

The input *RC* circuit for the BJT amplifier in Figure 10–8 is formed by C_1 and the amplifier's input resistance and is shown in Figure 10–10. (Input resistance was discussed in Chapter 6.) As the signal frequency decreases, X_{C1} increases. This causes less voltage across the input resistance of the amplifier at the base because more voltage is dropped across C_1 and because of this, the overall voltage gain of the amplifier is reduced. The base voltage for the input *RC* circuit in Figure 10–10 (neglecting the internal resistance of the input signal source) can be stated as

$$V_{base} = \left(\frac{R_{in}}{\sqrt{R_{in}^2 + X_{C1}^2}}\right)V_{in}$$

▶ FIGURE 10–10

Input *RC* circuit formed by the input coupling capacitor and the amplifier's input resistance.



As previously mentioned, a critical point in the amplifier's response occurs when the output voltage is 70.7% of its midrange value. This condition occurs in the input *RC* circuit when $X_{C1} = R_{in}$.

$$V_{base} = \left(\frac{R_{in}}{\sqrt{R_{in}^2 + R_{in}^2}}\right)V_{in} = \left(\frac{R_{in}}{\sqrt{2R_{in}^2}}\right)V_{in} = \left(\frac{R_{in}}{\sqrt{2}R_{in}}\right)V_{in} = \left(\frac{1}{\sqrt{2}}\right)V_{in} = 0.707V_{in}$$

In terms of measurement in decibels,

$$20\log\left(\frac{V_{base}}{V_{in}}\right) = 20\log(0.707) = -3\text{ dB}$$

Lower Critical Frequency The condition where the gain is down 3 dB is logically called the −3 *dB point* of the amplifier response; the overall gain is 3 dB less than at midrange frequencies because of the attenuation (gain less than 1) of the input *RC* circuit. The frequency, f_{cl}, at which this condition occurs is called the *lower critical frequency* (also known as the *lower cutoff frequency, lower corner frequency,* or *lower break frequency*) and can be calculated as follows:

$$X_{C1} = \frac{1}{2\pi f_{cl(input)}C_1} = R_{in}$$

Equation 10–6

$$\mathbf{f_{cl(input)} = \frac{1}{2\pi R_{in}C_1}}$$

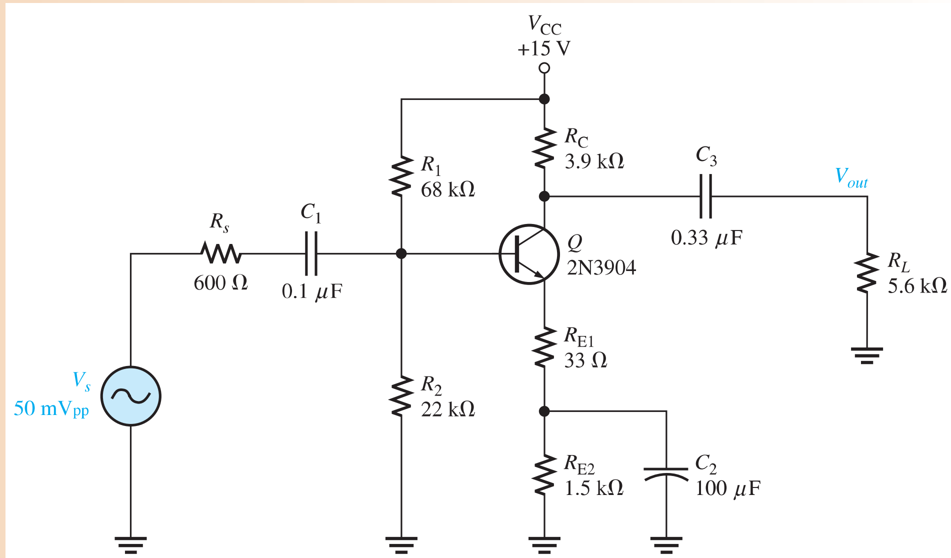
If the resistance of the input source is taken into account, Equation 10–6 becomes

$$f_{cl(input)} = \frac{1}{2\pi(R_s + R_{in})C_1}$$

EXAMPLE 10–3

For the circuit in Figure 10–11, calculate the lower critical frequency due to the input *RC* circuit. Assumed $r'_e = 9.6\ \Omega$ and $\beta = 200$. Notice that a swamping resistor, R_{E1}, is used.

▶ **FIGURE 10–11**



Solution The input resistance is

$$R_{in} = R_1 \| R_2 \| (\beta(r'_e + R_{E1})) = 68\ \text{k}\Omega \| 22\ \text{k}\Omega \| (200(9.6\ \Omega + 33\ \Omega)) = 5.63\ \text{k}\Omega$$

The lower critical frequency is

$$f_{cl(input)} = \frac{1}{2\pi R_{in} C_1} = \frac{1}{2\pi(5.63\ \text{k}\Omega)(0.1\ \mu\text{F})} = \mathbf{282\ Hz}$$

Related Problem What value of input capacitor will move the lower cutoff frequency to 130 Hz?

Open the Multisim file E10-03 in the Examples folder on the companion website and read the critical frequency on the Bode plotter. The Bode plotter is not an actual instrument available, but allows the user to see the response of a circuit in the frequency domain (frequency is the independent variable). Notice that C_2 and C_3 are taken out of the calculation by making their value huge (1 F!). While this is unrealistic, it works nicely for the computer simulation to isolate the input response.

Voltage Gain Roll-Off at Low Frequencies As you have seen, the input *RC* circuit reduces the overall voltage gain of an amplifier by 3 dB when the frequency is reduced to the critical value f_c. As the frequency continues to decrease below f_c, the overall voltage gain also continues to decrease. The rate of decrease in voltage gain with frequency is called **roll-off**. For each ten times reduction in frequency below f_c, *there is a 20 dB reduction in voltage gain.*

Let's consider a frequency that is one-tenth of the critical frequency ($f = 0.1f_c$). Since $X_{C1} = R_{in}$ at f_c, then $X_{C1} = 10R_{in}$ at $0.1f_c$ because of the inverse relationship of X_{C1} and f. The attenuation of the input *RC* circuit is, therefore,

$$\text{Attenuation} = \frac{V_{base}}{V_{in}} = \frac{R_{in}}{\sqrt{R_{in}^2 + X_{C1}^2}} = \frac{R_{in}}{\sqrt{R_{in}^2 + (10R_{in})^2}} = \frac{R_{in}}{\sqrt{R_{in}^2 + 100R_{in}^2}}$$

$$= \frac{R_{in}}{\sqrt{R_{in}^2(1 + 100)}} = \frac{R_{in}}{R_{in}\sqrt{101}} = \frac{1}{\sqrt{101}} \cong \frac{1}{10} = 0.1$$

HISTORY NOTE

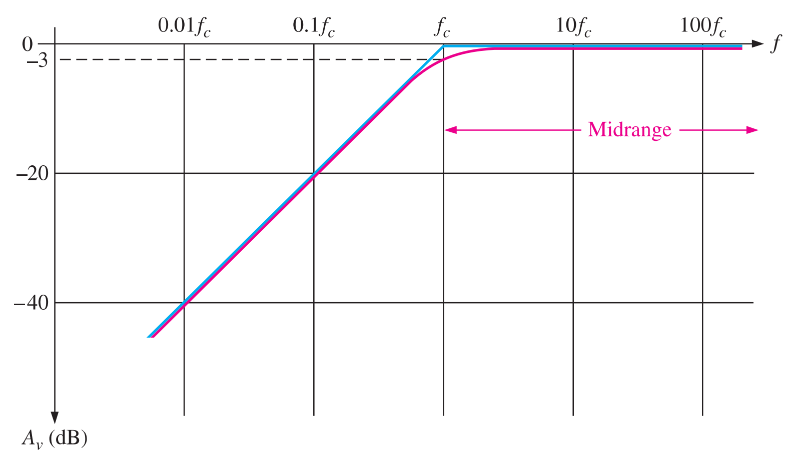
Hendrik Wade Bode pronounced *Boh-dee* (1905–1982) was born in Madison, Wisconsin. He received his B.A. degree in 1924, at the age of 19, from Ohio State University and his M.A. degree in 1926, both in Mathematics. He was hired by Bell Labs and completed his Ph.D. in Physics in 1935. In 1938 he developed his now well-known magnitude and phase plots. His work on automatic control systems introduced innovative methods to the study of system stability.

The dB attenuation is

$$20 \log \left(\frac{V_{base}}{V_{in}} \right) = 20 \log (0.1) = -20 \text{ dB}$$

The Bode Plot A ten-times change in frequency is called a **decade**. So, for the input *RC* circuit, the attenuation is reduced by 20 dB for each decade that the frequency decreases below the critical frequency. This causes the overall voltage gain to drop 20 dB per decade.

A plot of dB voltage gain versus frequency on semilog graph paper (logarithmic horizontal axis scale and a linear vertical axis scale) is called a **Bode plot**. A generalized Bode plot for an input *RC* circuit appears in Figure 10–12. The ideal response curve is shown in blue. Notice that it is flat (0 dB) down to the critical frequency, at which point the gain drops at −20 dB/decade as shown. Above f_c are the midrange frequencies. The actual response curve is shown in red. Notice that it decreases gradually beginning in midrange and is down to −3 dB at the critical frequency. Often, the ideal response is used to simplify amplifier analysis. As previously mentioned, the critical frequency at which the curve "breaks" into a −20 dB/decade drop is sometimes called the *lower break frequency*.



▲ **FIGURE 10–12**

Bode plot. (Blue is ideal; red is actual.)

Sometimes, the voltage gain roll-off of an amplifier is expressed in dB/octave rather than dB/decade. An **octave** corresponds to a doubling or halving of the frequency. For example, an increase in frequency from 100 Hz to 200 Hz is an octave. Likewise, a decrease in frequency from 100 kHz to 50 kHz is also an octave. A rate of −20 dB/decade is approximately equivalent to −6 dB/octave, a rate of −40 dB/decade is approximately equivalent to −12 dB/octave, and so on.

EXAMPLE 10–4

The midrange voltage gain of a certain amplifier is 100. The input *RC* circuit has a lower critical frequency of 1 kHz. Determine the actual voltage gain at $f = 1$ kHz, $f = 100$ Hz, and $f = 10$ Hz.

Solution

When $f = 1$ kHz, the voltage gain is 3 dB less than at midrange. At −3 dB, the voltage gain is reduced by a factor of 0.707.

$$A_v = (0.707)(100) = \mathbf{70.7}$$

When $f = 100 \text{ Hz} = 0.1f_c$, the voltage gain is 20 dB less than at f_c. The voltage gain at −20 dB is one-tenth of that at the midrange frequencies.

$$A_v = (0.1)(100) = \mathbf{10}$$

When $f = 10 \text{ Hz} = 0.01f_c$, the voltage gain is 20 dB less than at $f = 0.1f_c$ or -40 dB. The voltage gain at -40 dB is one-tenth of that at -20 dB or one-hundredth that at the midrange frequencies.

$$A_v = (0.01)(100) = \mathbf{1}$$

Related Problem The midrange voltage gain of an amplifier is 300. The lower critical frequency of the input RC circuit is 400 Hz. Determine the actual voltage gain at 400 Hz, 40 Hz, and 4 Hz.

Phase Shift in the Input RC Circuit In addition to reducing the voltage gain, the input RC circuit also causes an increasing phase shift through an amplifier as the frequency decreases. At midrange frequencies, the phase shift through the input RC circuit is approximately zero because the capacitive reactance, X_{C1}, is approximately 0 Ω. At lower frequencies, higher values of X_{C1} cause a phase shift to be introduced, and the output voltage of the RC circuit leads the input voltage. As you learned in ac circuit theory, the phase angle in an input RC circuit is expressed as

$$\boldsymbol{\theta = \tan^{-1}\left(\frac{X_{C1}}{R_{in}}\right)}$$

Equation 10–7

For midrange frequencies, $X_{C1} \cong 0\ \Omega$, so

$$\theta = \tan^{-1}\left(\frac{0\ \Omega}{R_{in}}\right) = \tan^{-1}(0) = 0°$$

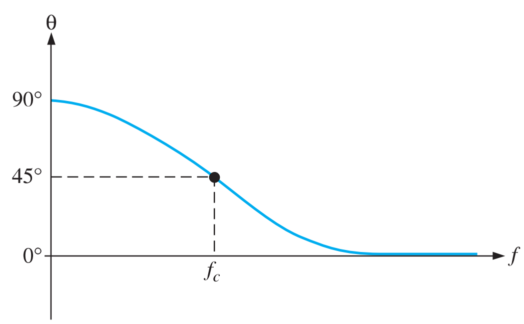
At the critical frequency, $X_{C1} = R_{in}$, so

$$\theta = \tan^{-1}\left(\frac{R_{in}}{R_{in}}\right) = \tan^{-1}(1) = 45°$$

At a decade below the critical frequency, $X_{C1} = 10R_{in}$, so

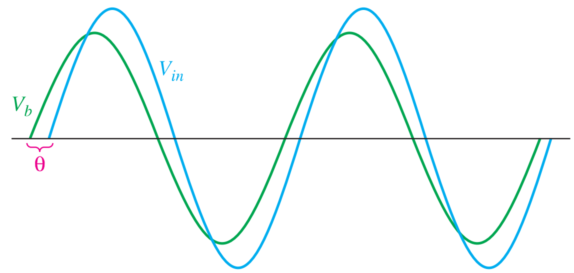
$$\theta = \tan^{-1}\left(\frac{10R_{in}}{R_{in}}\right) = \tan^{-1}(10) = 84.3°$$

A continuation of this analysis will show that the phase shift through the input RC circuit approaches 90° as the frequency approaches zero. A plot of phase angle versus frequency is shown in Figure 10–13. The result is that the voltage at the base of the transistor *leads* the input signal voltage in phase below midrange, as shown in Figure 10–14.



▲ FIGURE 10–13

Phase angle versus frequency for the input RC circuit.



▲ FIGURE 10–14

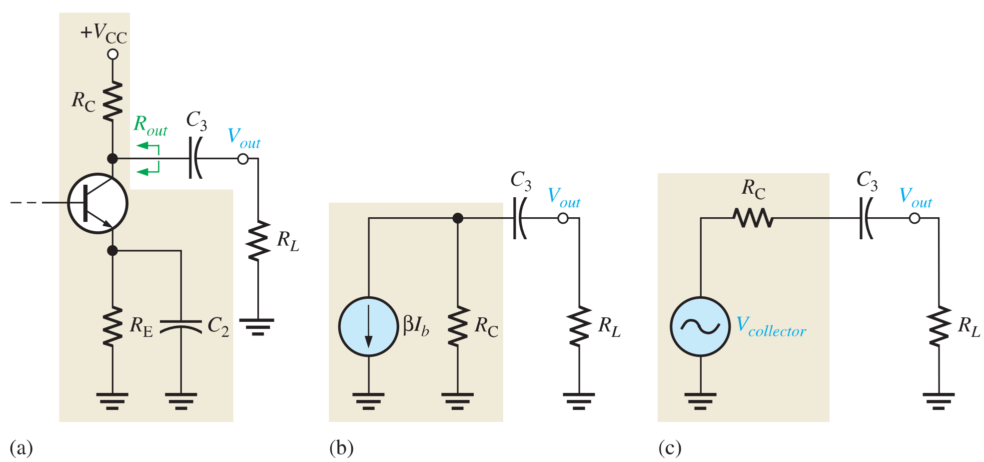
The input *RC* circuit causes the base voltage to lead the input voltage below midrange by an amount equal to the circuit phase angle, θ.

The Output *RC* Circuit

The second high-pass *RC* circuit in the BJT amplifier of Figure 10–8 is formed by the coupling capacitor C_3, the resistance looking in at the collector, and the load resistance R_L, as shown in Figure 10–15(a). In determining the output resistance, looking in at the collector, the transistor is treated as an ideal current source (with infinite internal resistance), and the upper end of R_C is effectively at ac ground, as shown in Figure 10–15(b). Therefore, thevenizing the circuit to the left of capacitor C_3 produces an equivalent voltage source equal to the collector voltage and a series resistance equal to R_C, as shown in Figure 10–15(c). The lower critical frequency of this output *RC* circuit is

Equation 10–8

$$f_{cl(output)} = \frac{1}{2\pi(R_C + R_L)C_3}$$



▲ FIGURE 10–15

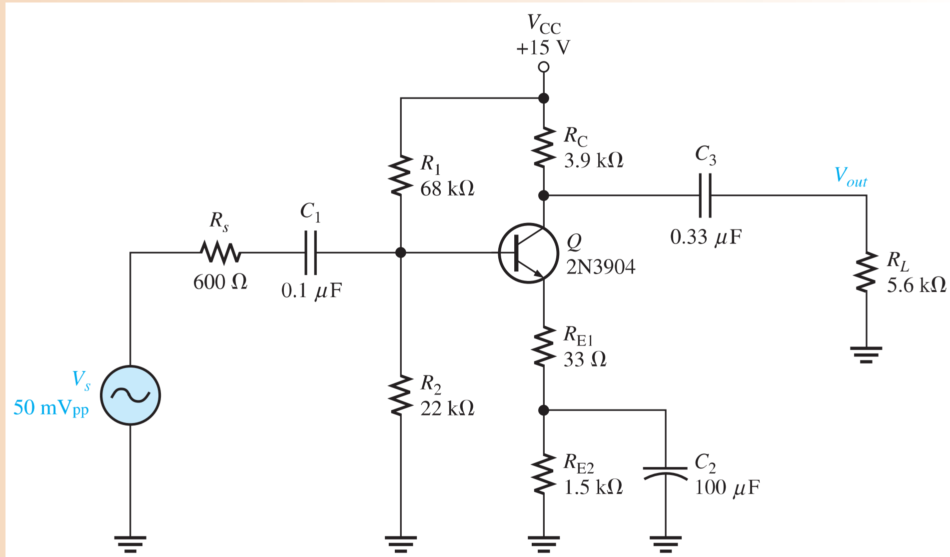
Development of the equivalent low-frequency output *RC* circuit.

The effect of the output *RC* circuit on the amplifier voltage gain is similar to that of the input *RC* circuit. As the signal frequency decreases, X_{C3} increases. This causes less voltage across the load resistance because more voltage is dropped across C_3. The signal voltage is reduced by a factor of 0.707 when frequency is reduced to the lower critical value, f_{cl}, for the circuit. This corresponds to a 3 dB reduction in voltage gain.

EXAMPLE 10–5

For the circuit from Example 10–3 and shown in Figure 10–16, calculate the lower critical frequency due to the output *RC* circuit.

▶ **FIGURE 10–16**



Solution The resistance in the output *RC* circuit is

$$R_C + R_L = 3.9\text{ k}\Omega + 5.6\text{ k}\Omega = 9.5\text{ k}\Omega$$

The lower critical frequency is

$$f_{cl(output)} = \frac{1}{2\pi(R_C + R_L)C_3} = \frac{1}{2\pi(9.5\text{ k}\Omega)(0.33\ \mu\text{F})} = \mathbf{50.8\ Hz}$$

Related Problem What effect does a larger load resistor have on the gain and the lower cutoff frequency?

Open the Multisim file E10-05 in the Examples folder on the companion website and read the critical frequency on the Bode plotter. Notice that C_1 and C_2 are taken out of the calculation by making their value huge as explained in Example 10–3.

Phase Shift in the Output RC Circuit The phase angle in the output *RC* circuit is

$$\theta = \tan^{-1}\left(\frac{X_{C3}}{R_C + R_L}\right)$$

Equation 10–9

$\theta \cong 0°$ for the midrange frequencies and approaches 90° as the frequency approaches zero (X_{C3} approaches infinity). At the critical frequency f_c, the phase shift is 45°.

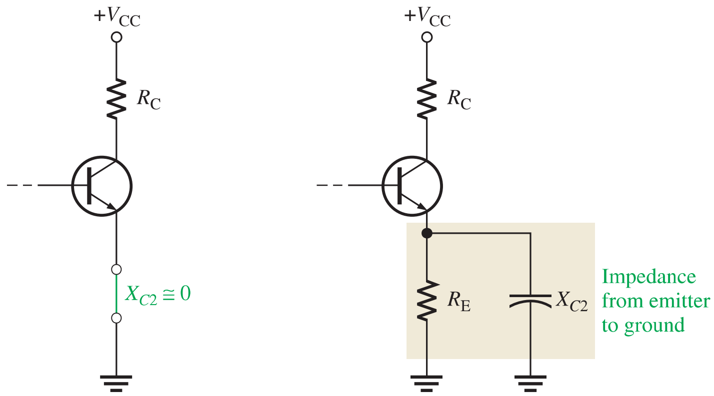
The Bypass *RC* Circuit

The third *RC* circuit that affects the low-frequency gain of the BJT amplifier in Figure 10–8 includes the bypass capacitor C_2. As illustrated in Figure 10–17(a) for midrange frequencies, it is assumed that $X_{C2} \cong 0\ \Omega$, effectively shorting the emitter to ground so that the amplifier gain is R_c/r'_e, as you already know. As the frequency is reduced, X_{C2} increases and no longer provides a sufficiently low reactance to effectively place the emitter at ac ground, as shown in part (b). Because the impedance from emitter to ground increases, the gain decreases. In this case, R_e in the formula, $A_v = R_c/(r'_e + R_e)$, is replaced by an impedance formed by R_E in parallel with X_{C2}.

The bypass *RC* circuit is formed by C_2 and the resistance looking in at the emitter, $R_{in(emitter)}$, as shown in Figure 10–18(a). The resistance looking in at the emitter is derived

FIGURE 10–17

At low frequencies, X_{C2} in parallel with R_E creates an impedance that reduces the voltage gain.



(a) For midrange frequencies, C_2 effectively shorts the emitter to ground.

(b) Below f_c, X_{C2} and R_E form an impedance between the emitter and ground.

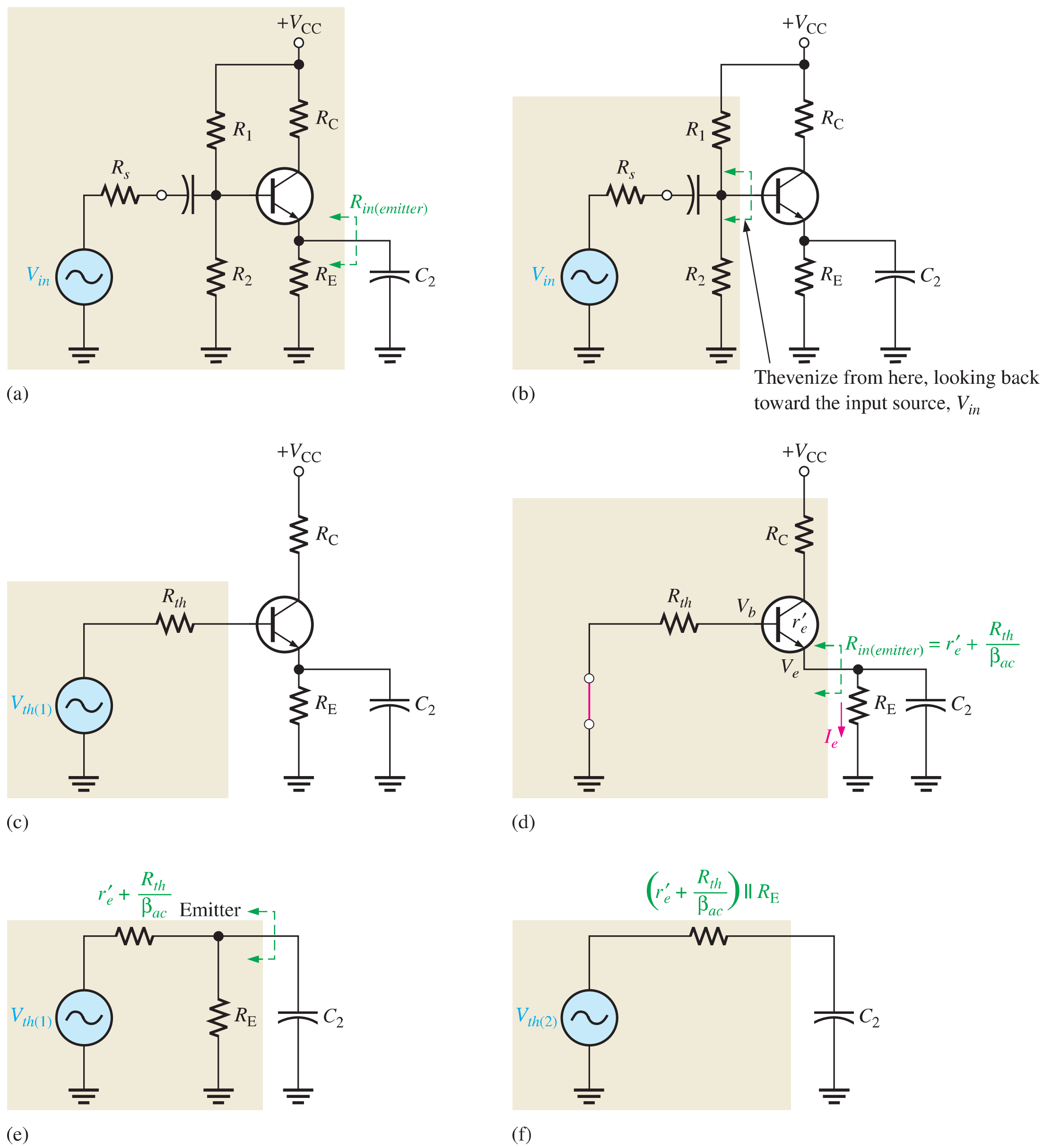


FIGURE 10–18

Development of the equivalent bypass *RC* circuit.

as follows. First, Thevenin's theorem is applied looking from the base of the transistor toward the input source V_{in}, as shown in Figure 10–18(b). This results in an equivalent resistance (R_{th}) and an equivalent voltage source ($V_{th(1)}$) in series with the base, as shown in Figure 10–18(c). The resistance looking in at the emitter is determined with the equivalent input source shorted, as shown in Figure 10–18(d), and is expressed as follows:

$$R_{in(emitter)} = r'_e + \frac{V_e}{I_e} \cong r'_e + \frac{V_b}{\beta_{ac} I_b} = r'_e + \frac{I_b R_{th}}{\beta_{ac} I_b}$$

$$\boldsymbol{R_{in(emitter)} = r'_e + \frac{R_{th}}{\beta_{ac}}}$$

Equation 10–10

Looking from the capacitor C_2, $r'_e + R_{th}/\beta_{ac}$ is in parallel with R_E, as shown in Figure 10–18(e). Thevenizing again, we get the equivalent *RC* circuit shown in Figure 10–18(f). The lower critical frequency for this equivalent bypass *RC* circuit is

$$\boldsymbol{f_{cl(bypass)} = \frac{1}{2\pi[(r'_e + R_{th}/\beta_{ac}) \parallel R_E]C_2}}$$

Equation 10–11

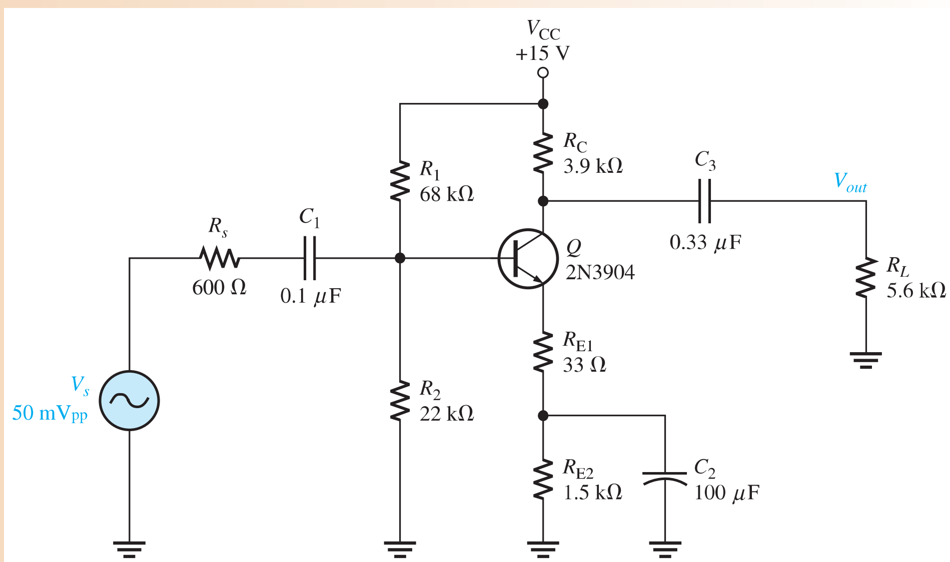
If a swamping resistor is used, the equation for $R_{in(emitter)}$ becomes

$$R_{in(emitter)} = r'_e + R_{E1} + \frac{R_{th}}{\beta_{ac}}$$

EXAMPLE 10–6

For the circuit from Example 10–3 and shown in Figure 10–19, calculate the lower critical frequency due to the bypass *RC* circuit. Assume $r'_e = 9.6\ \Omega$ and $\beta = 200$.

▶ FIGURE 10–19



Solution The resistance in the emitter bypass circuit is

$$R_{in(emitter)} = r'_e + R_{E1} + \frac{R_{th}}{\beta_{ac}} = 9.6\ \Omega + 33\ \Omega + \frac{68\ \text{k}\Omega \parallel 22\ \text{k}\Omega \parallel 600\ \Omega}{200} = 45.5\ \Omega$$

The lower critical frequency is

$$f_{cl(bypass)} = \frac{1}{2\pi(R_{in(emitter)} \parallel R_{E2})C_2} = \frac{1}{2\pi(45.5\ \Omega \parallel 1.5\ \text{k}\Omega)(100\ \mu\text{F})} = \mathbf{36.0\ Hz}$$

Related Problem Explain why C_2 is larger than C_1 or C_3.

Open the Multisim file E10-06 in the Examples folder on the companion website and read the critical frequency on the Bode plotter. Notice that C_1 and C_3 are taken out of the calculation by making their value huge as before (1 F!).

FET Amplifiers

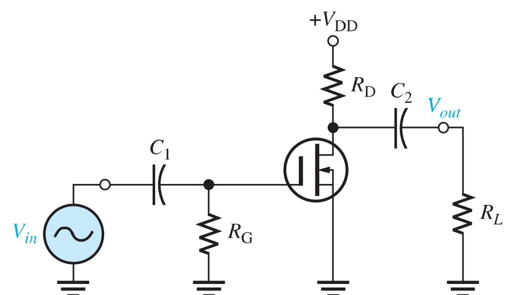
A zero-biased D-MOSFET amplifier with capacitive coupling on the input and output is shown in Figure 10–20. As you learned in Chapter 9, the midrange voltage gain of a zero-biased amplifier is

$$A_{v(mid)} = g_m R_d$$

This is the gain at frequencies high enough so that the capacitive reactances are approximately zero.

▶ FIGURE 10–20

Zero-biased D-MOSFET amplifier.



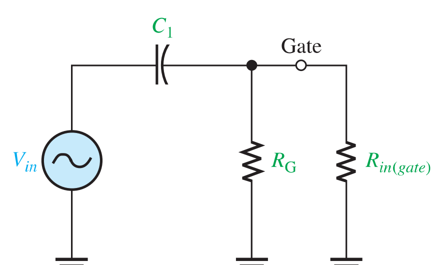
The amplifier in Figure 10–20 has only two high-pass *RC* circuits that influence its low-frequency response. One *RC* circuit is formed by the input coupling capacitor C_1 and the input resistance. The other circuit is formed by the output coupling capacitor C_2 and the output resistance looking in at the drain.

The Input *RC* Circuit

The input *RC* circuit for the FET amplifier in Figure 10–20 is shown in Figure 10–21. As in the case for the BJT amplifier, the reactance of the input coupling capacitor increases as the frequency decreases. When $X_{C1} = R_{in}$, the gain is down 3 dB below its midrange value.

▶ FIGURE 10–21

Input *RC* circuit.



The lower critical frequency is

$$f_{cl(input)} = \frac{1}{2\pi R_{in} C_1}$$

The input resistance is

$$R_{in} = R_G \| R_{in(gate)}$$

where $R_{in(gate)}$ is determined from datasheet information as

$$R_{in(gate)} = \left|\frac{V_{GS}}{I_{GSS}}\right|$$

Therefore, the lower critical frequency is

$$f_{cl(input)} = \frac{1}{2\pi(R_G \| R_{in(gate)})C_1}$$

Equation 10–12

For practical work, the value of $R_{in(gate)}$ is so large it can be ignored, as will be illustrated in Example 10–7.

The gain rolls off below f_c at 20 dB/decade, as previously shown. The phase angle in the low-frequency input *RC* circuit is

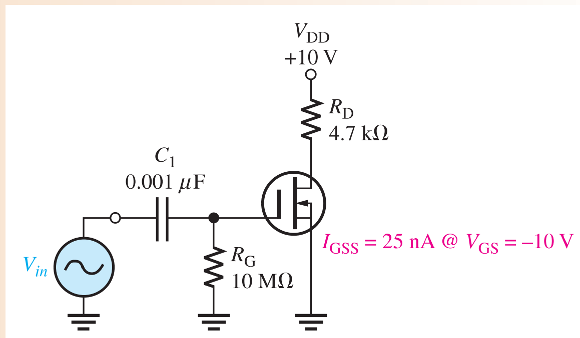
$$\theta = \tan^{-1}\left(\frac{X_{C1}}{R_{in}}\right)$$

Equation 10–13

EXAMPLE 10–7

What is the lower critical frequency of the input *RC* circuit in the FET amplifier of Figure 10–22?

▶ FIGURE 10–22



Solution First determine R_{in} and then calculate f_c.

$$R_{in(gate)} = \left|\frac{V_{GS}}{I_{GSS}}\right| = \frac{10\text{ V}}{25\text{ nA}} = 400\text{ M}\Omega$$

$$R_{in} = R_G \| R_{in(gate)} = 10\text{ M}\Omega \| 400\text{ M}\Omega = 9.8\text{ M}\Omega$$

$$f_{cl(input)} = \frac{1}{2\pi R_{in}C_1} = \frac{1}{2\pi(9.8\text{ M}\Omega)(0.001\text{ }\mu\text{F})} = \mathbf{16.2\text{ Hz}}$$

For all practical purposes,

$$R_{in} \cong R_G = 10\text{ M}\Omega$$

and

$$f_{cl(input)} = \frac{1}{2\pi R_G C_1} = \frac{1}{2\pi(10\text{ M}\Omega)(0.001\text{ }\mu\text{F})} \cong 15.9\text{ Hz}$$

There is very little difference in the two results.

The critical frequency of the input *RC* circuit of a FET amplifier is usually very low because of the very high input resistance and the high value of R_G.

Related Problem How much does the lower critical frequency of the input *RC* circuit change if the FET in Figure 10–22 is replaced by one with $I_{GSS} = 10$ nA @ $V_{GS} = -8$ V?

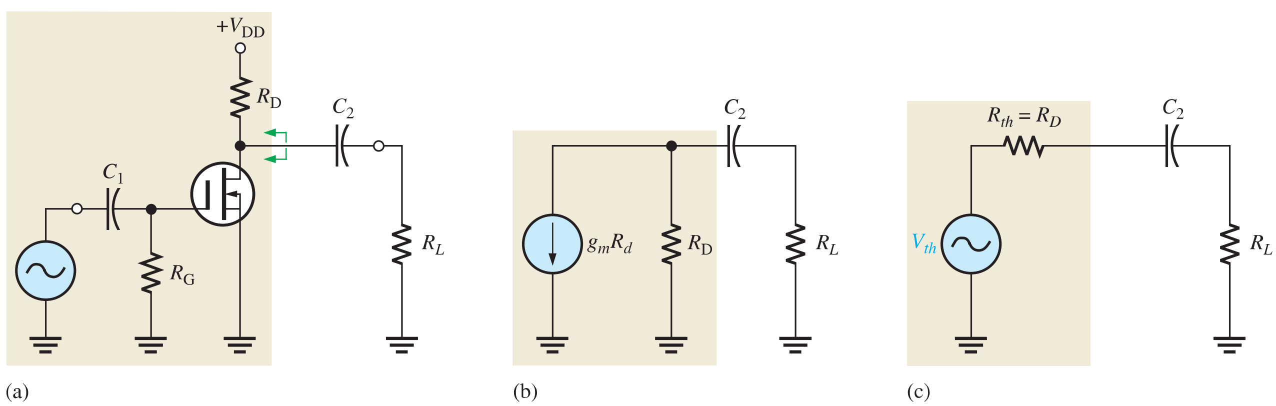
Open the Multisim file E10-07 in the Examples folder on the companion website and measure the low critical frequency for the input circuit. Compare to the calculated results.

The Output *RC* Circuit

The second *RC* circuit that affects the low-frequency response of the FET amplifier in Figure 10–20 is formed by a coupling capacitor C_2 and the output resistance looking in at the drain, as shown in Figure 10–23(a). The load resistor, R_L, is also included. As in the case of the BJT, the FET is treated as a current source, and the upper end of R_D is effectively ac ground, as shown in Figure 10–23(b). The Thevenin equivalent of the circuit to the left of C_2 is shown in Figure 10–23(c). The lower critical frequency for this *RC* circuit is

Equation 10–14

$$f_{cl(output)} = \frac{1}{2\pi(R_D + R_L)C_2}$$



▲ FIGURE 10–23

Development of the equivalent low-frequency output *RC* circuit.

The effect of the output *RC* circuit on the amplifier's voltage gain below the midrange is similar to that of the input *RC* circuit. The circuit with the highest critical frequency dominates because it is the one that first causes the gain to roll off as the frequency drops below its midrange values. The phase angle in the low-frequency output *RC* circuit is

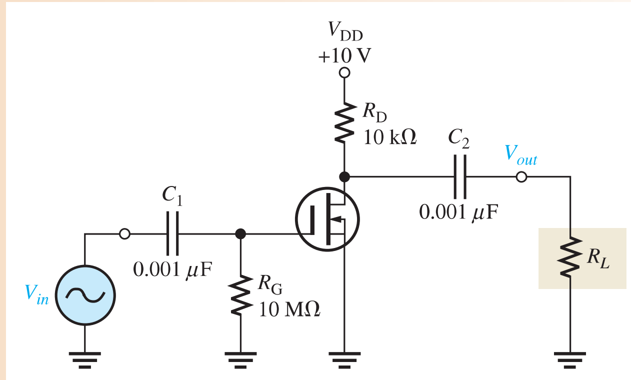
Equation 10–15

$$\theta = \tan^{-1}\left(\frac{X_{C2}}{R_D + R_L}\right)$$

Again, at the critical frequency, the phase angle is 45° and approaches 90° as the frequency approaches zero. However, starting at the critical frequency, the phase angle decreases from 45° and becomes very small as the frequency goes higher.

EXAMPLE 10–8

Determine the lower critical frequencies for the FET amplifier in Figure 10–24. Assume that the load is another identical amplifier with the same R_{in}. The datasheet shows $I_{GSS} = 100$ nA at $V_{GS} = -12$ V.



▲ FIGURE 10–24

Solution First, find the lower critical frequency for the input *RC* circuit.

$$R_{in(gate)} = \left|\frac{V_{GS}}{I_{GSS}}\right| = \frac{12\text{ V}}{100\text{ nA}} = 120\text{ M}\Omega$$

$$R_{in} = R_G \| R_{in(gate)} = 10\text{ M}\Omega \| 120\text{ M}\Omega = 9.2\text{ M}\Omega$$

$$f_{cl(input)} = \frac{1}{2\pi R_{in}C_1} = \frac{1}{2\pi(9.2\text{ M}\Omega)(0.001\ \mu\text{F})} = \mathbf{17.3\ Hz}$$

The output *RC* circuit has a lower critical frequency of

$$f_{cl(output)} = \frac{1}{2\pi(R_D + R_L)C_2} = \frac{1}{2\pi(9.21\text{ M}\Omega)(0.001\ \mu\text{F})} \cong \mathbf{17.3\ Hz}$$

Related Problem If the circuit in Figure 10–24 were operated with no load, how is the low-frequency response affected?

Open the Multisim file E10-08 in the Examples folder on the companion website. Determine the total low-frequency response of the amplifier.

Total Low-Frequency Response of an Amplifier

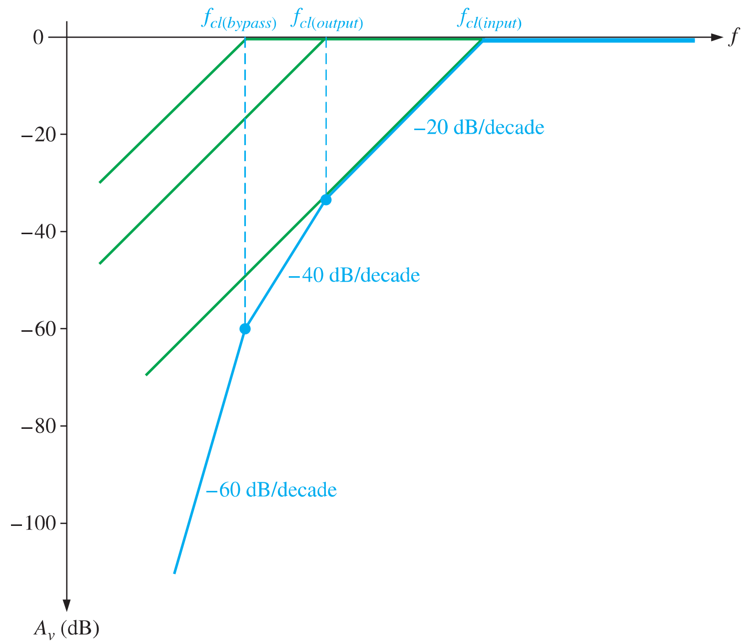
Now that we have individually examined the high-pass *RC* circuits that affect a BJT or FET amplifier's voltage gain at low frequencies, let's look at the combined effect of the three *RC* circuits in a BJT amplifier. Each circuit has a critical frequency determined by the *R* and *C* values. The critical frequencies of the three *RC* circuits are not necessarily all equal. If one of the *RC* circuits has a critical (break) frequency higher than the other two, then it is the *dominant RC* circuit. The dominant circuit determines the frequency at which the overall voltage gain of the amplifier begins to drop at −20 dB/decade. The other circuits each cause an additional −20 dB/decade roll-off below their respective critical (break) frequencies.

To get a better picture of what happens at low frequencies, refer to the Bode plot in Figure 10–25, which shows the superimposed ideal responses for the three *RC* circuits (green lines) of a BJT amplifier. In this example, each *RC* circuit has a different critical frequency. The input *RC* circuit is dominant (highest f_c) in this case, and the bypass *RC* circuit has the lowest f_c. The ideal overall response is shown as the blue line.

Here is what happens. As the frequency is reduced from midrange, the first "break point" occurs at the critical frequency of the input *RC* circuit, $f_{cl(input)}$, and the gain begins to drop at −20 dB/decade. This constant roll-off rate continues until the critical frequency of the output *RC* circuit, $f_{cl(output)}$, is reached. At this break point, the output *RC* circuit adds another −20 dB/decade to make a total roll-off of −40 dB/decade. This constant

▶ **FIGURE 10–25**

Composite Bode plot of a BJT amplifier response for three low-frequency *RC* circuits with different critical frequencies. Total response is shown by the blue curve.

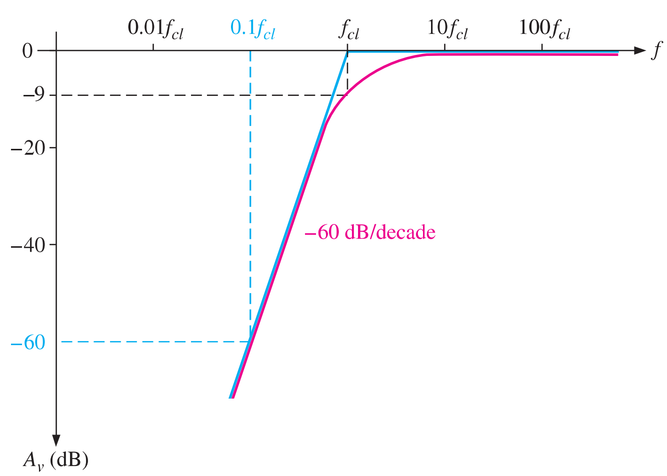


−40 dB/decade roll-off continues until the critical frequency of the bypass *RC* circuit, $f_{cl(bypass)}$, is reached. The bypass *RC* circuit adds still another −20 dB/decade at this break point, making the gain roll-off at −60 dB/decade.

If all *RC* circuits have the same critical frequency, the response curve has one break point at that value of f_{cl}, and the voltage gain rolls off at −60 dB/decade below that value, as shown by the ideal curve (blue) in Figure 10–26. Actually, the midrange voltage gain does not extend down to the dominant critical frequency but is really at −9 dB below the midrange voltage gain at that point (−3 dB for each *RC* circuit), as shown by the red curve.

▶ **FIGURE 10–26**

Composite Bode plot of an amplifier response where all *RC* circuits have the same f_{cl}. (Blue is ideal; red is actual.)

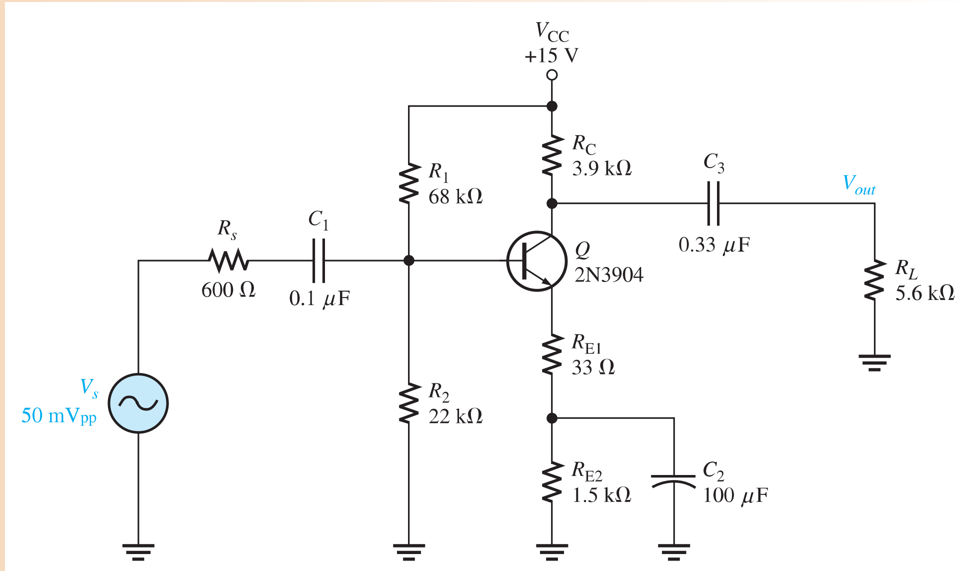


EXAMPLE 10–9

For the circuit from Example 10–3 and shown in Figure 10–27, determine the midband gain in decibels and draw the Bode plot, showing each of the lower critical frequencies. Assume $r'_e = 9.6\ \Omega$.

Solution The midband gain is

$$A_v = \frac{R_C R_L}{r'_e + R_{E1}} = \frac{(3.9\ \text{k}\Omega)(5.6\ \text{k}\Omega)}{9.6\ \Omega + 33\ \Omega} = 54.0$$



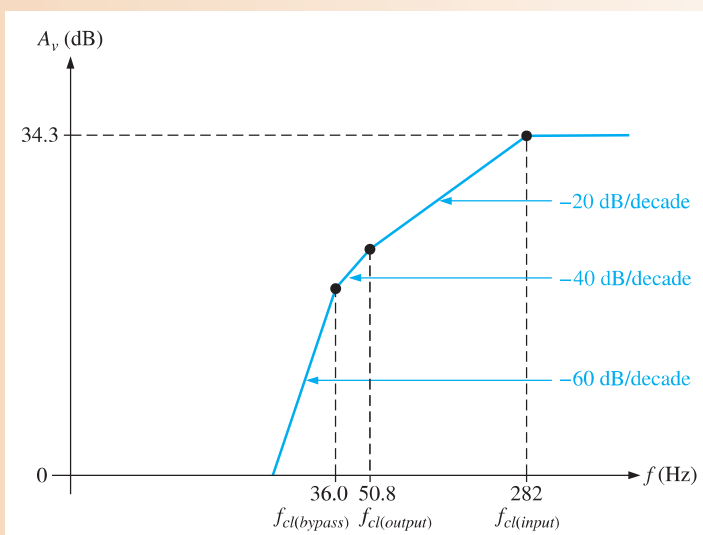
▲ FIGURE 10–27

In decibels,

$$A_v = 20 \log (54.0) = \mathbf{34.3\ dB}$$

The critical frequency for the input circuit was found in Example 10–3 and is 282 Hz. The critical frequency for the output circuit was found in Example 10–5 and is 50.8 Hz. The critical frequency for the emitter bypass circuit was found in Example 10–6 and is 36.0 Hz.

The overall response is shown in the Bode plot of Figure 10–28. The lower critical frequency of the input circuit has the highest value and is therefore the overall or dominant critical frequency because the response first begins to roll off at this frequency.



▶ FIGURE 10–28

Ideal Bode plot for the overall low-frequency response of the amplifier in Figure 10–27.

Related Problem If the overall gain of the amplifier is reduced by increasing R_{E1}, how will the lower critical frequency be affected?

FYI

SPICE was one of the first computer programs that could simulate electronic circuits. Its origins can be traced to a program called CANCER (Computer Analysis of Nonlinear Circuits, Excluding Radiation) at the University of California. It was developed as a computer aid for designing integrated circuits in the 1960s. SPICE is an acronym for Simulation Program with Integrated Circuit Emphasis. Over the years, SPICE has been revised many times but is still the underlying software for many of today's simulations.

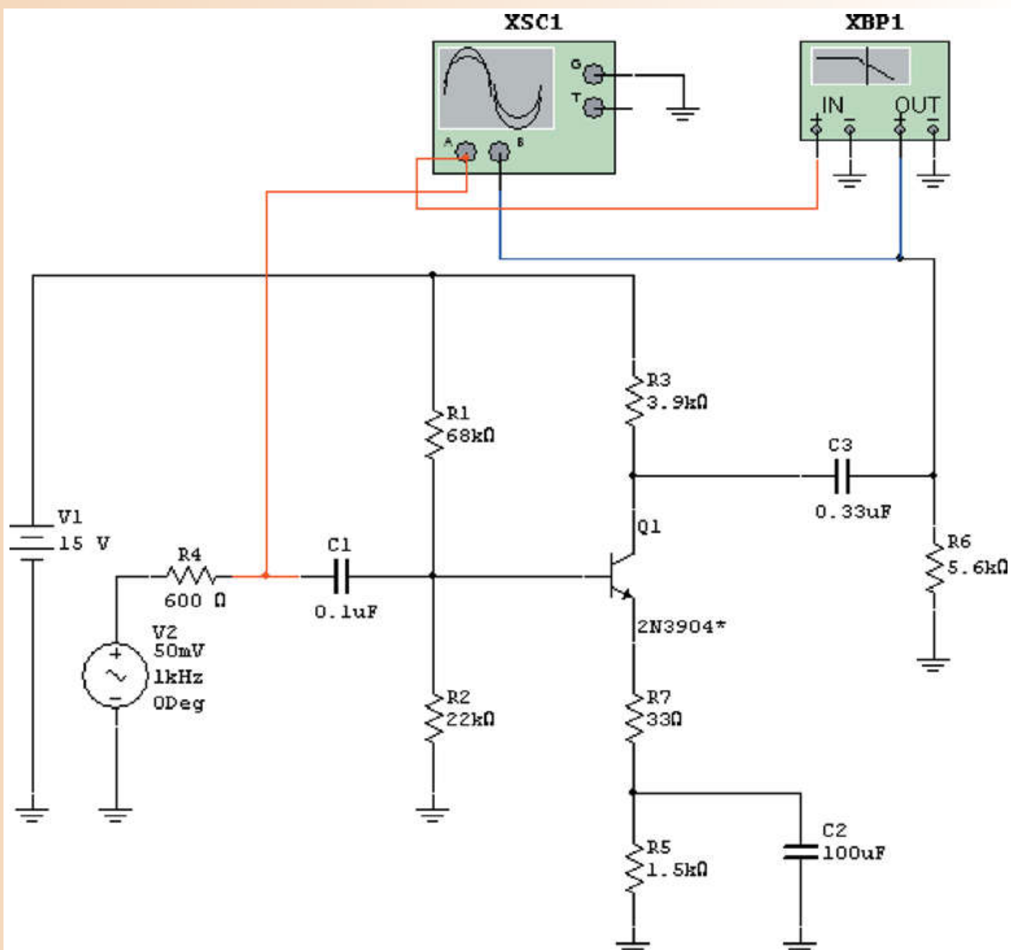
Computer Simulation of Frequency Response

As you saw in the previous example, the calculation of multiple critical frequencies is involved and each critical frequency contributes to the overall response. The ideal response shown in Example 10–9 is an excellent first approximation, but when more accuracy is required, a computer simulation is used. The computer takes into account all of the parameters for the particular device including effects such as internal capacitances that are usually ignored in manual calculations, and it can calculate in detail the interactions that occur when there are multiple breakpoints as in Example 10–9.

Multisim is based on SPICE models that can show the frequency response of circuits on the Bode plotter. As mentioned earlier, the Bode plotter is not a real instrument. It performs the same function as an instrument called the spectrum analyzer, which can also plot the frequency response of a circuit. Example 10–10 illustrates the application of computer analysis to the circuit in the previous example.

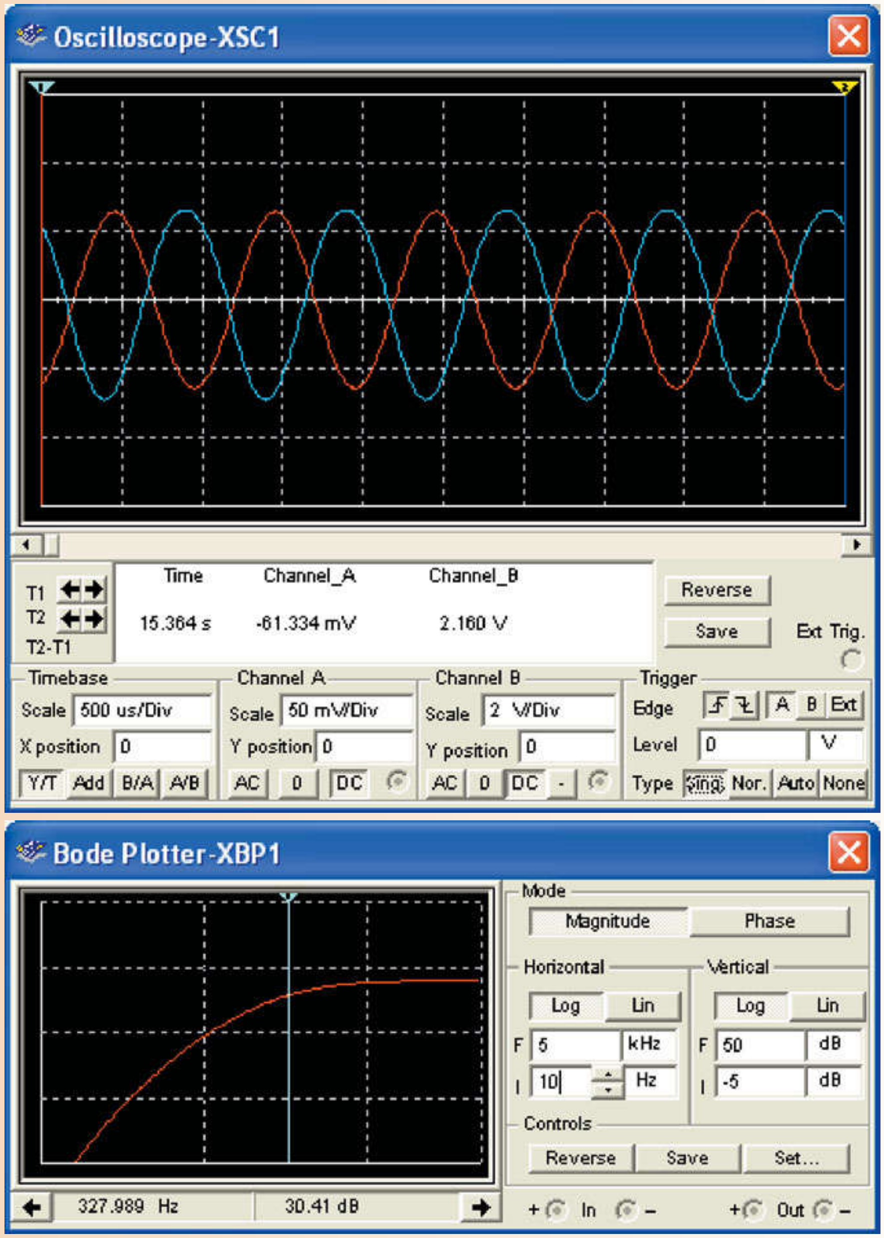
EXAMPLE 10–10 Use Multisim to show the overall low-frequency response of the circuit in Example 10–9.

Solution Figure 10–29 shows the circuit in Multisim with an oscilloscope display and Bode plotter. The cursor is set to the critical frequency on the Bode plotter so that the



▲ FIGURE 10–29

frequency can be read directly. The result in Figure 10–30 indicates the overall critical frequency is 328 Hz.



▲ FIGURE 10–30

Related Problem What change would you make to reduce the lower critical frequency to 100 Hz?

SECTION 10–3 CHECKUP

1. A certain BJT amplifier exhibits three critical frequencies in its low-frequency response: $f_{cl1} = 130$ Hz, $f_{cl2} = 167$ Hz, and $f_{cl3} = 75$ Hz. Which is the dominant critical frequency?
2. If the midrange voltage gain of the amplifier in Question 1 is 50 dB, what is the gain at the dominant f_{cl}?

3. A certain *RC* circuit has an $f_{cl} = 235$ Hz, above which the attenuation is 0 dB. What is the dB attenuation at 23.5 Hz?
4. What is the amount of phase shift contributed by an input circuit when $X_C = 0.5R_{in}$ at a certain frequency below f_{cl1}?
5. What is the critical frequency when $R_D = 1.5\ \text{k}\Omega$, $R_L = 5\ \text{k}\Omega$, and $C_2 = 0.0022\ \mu\text{F}$ in a circuit like Figure 10–24?

10–4 HIGH-FREQUENCY AMPLIFIER RESPONSE

You have seen how the coupling and bypass capacitors affect the voltage gain of an amplifier at lower frequencies where the reactances of the coupling and bypass capacitors are significant. In the midrange of an amplifier, the effects of the capacitors are minimal and can be neglected. If the frequency is increased sufficiently, a point is reached where the transistor's internal capacitances begin to have a significant effect on the gain. The basic differences between BJTs and FETs are the specifications of the internal capacitances and the input resistance.

After completing this section, you should be able to

- **Analyze the high-frequency response of an amplifier**
- Analyze a BJT amplifier
  - Apply Miller's theorem
- Identify and analyze the BJT amplifier's input *RC* circuit
  - Calculate the upper critical frequency and gain roll-off ◆ Determine the phase shift
- Identify and analyze the BJT amplifier's output *RC* circuit
  - Calculate the upper critical frequency ◆ Determine the phase shift
- Analyze a FET amplifier
- Identify and analyze a JFET amplifier
  - Determine internal capacitances on a datasheet ◆ Apply Miller's theorem
- Identify and analyze the JFET amplifier's input *RC* circuit
  - Calculate the upper critical frequency ◆ Determine the phase shift
- Identify and analyze the JFET amplifier's output *RC* circuit
  - Calculate the upper critical frequency ◆ Determine the phase shift
- Discuss the total high-frequency response of an amplifier
  - Use Bode plots to illustrate the high-frequency response

BJT Amplifiers

A high-frequency ac equivalent circuit for the BJT amplifier in Figure 10–31(a) is shown in Figure 10–31(b). Notice that the coupling and bypass capacitors are treated as effective shorts and do not appear in the equivalent circuit. The internal capacitances, C_{be} and C_{bc}, which are significant only at high frequencies, do appear in the diagram. As previously mentioned. C_{be} is sometimes called the input capacitance C_{ib}, and C_{bc} is sometimes called the output capacitance C_{ob}. C_{be} is specified on datasheets at a certain value of V_{BE}. Often, a datasheet will list C_{ib} as C_{ibo} and C_{ob} as C_{obo}. The *o* as the last letter in the subscript indicates the capacitance is measured with the base open. For example, a 2N2222A transistor has a C_{be} of 25 pF at $V_{BE} = 0.5$ V dc, $I_C = 0$, and $f = 1$ MHz. Also, C_{bc} is specified at a certain value of V_{BC}. The 2N2222A has a maximum C_{bc} of 8 pF at $V_{BC} = 10$ V dc.

Miller's Theorem in High-Frequency Analysis By applying Miller's theorem to the inverting amplifier in Figure 10–31(b) and using the midrange voltage gain, you have a circuit