

EXPERIMENT NO 07

IMPLEMENTATION OF HALF ADDER AND FULL ADDER

OBJECTIVE

To study Half and Full adder operations.

THEORY

Digital computers perform a variety of information-processing tasks. Among the basic functions encountered are various arithmetic operations. The most basic arithmetic operations are, no doubt, the addition and subtraction of binary digits (bit).

HALF ADDER

The possible operations, when we want to add only two bits, would be the followings:

$$0 + 0 = 0 \quad 0 + 1 = 1$$

$$1 + 0 = 1$$

$$1 + 1 = 0 \quad \& \quad \text{Carry } 1$$

Above mentioned operation could be performed by a **Half Adder** circuit.

FULL ADDER

We know that in practice, all addition operations must take into account the Carry bit (or digit) from the previous operation. Adders in digital computers also take into account the Carry bit from last operation and add it with the Augend and Addend bits of the present operation to complete the addition operation. The possible operations are:

$$0 + 0 + 0 \text{ (carry)} = 0$$

$$0 + 0 + 1 \text{ (carry)} = 1 \quad 0 + 1 + 0 \text{ (carry)} = 1$$

$$0 + 1 + 1 \text{ (carry)} = 0 \quad \& \quad \text{carry } 1 \text{ (to be added to next higher digit)}$$

$$1 + 1 + 0 \text{ (carry)} = 0 \quad \& \quad \text{carry } 1 \text{ (to be added to next higher digit)}$$

$$1 + 1 + 1 \text{ (carry)} = 1 \quad \& \quad \text{carry } 1 \text{ (to be added to next higher digit)}$$

The adder that performs the addition of three bits (two significant bits and a previous carry) is called a **Full Adder**.

TASK 1: HALF ADDER

We arbitrarily assign symbols **A** and **B** to the two inputs and **S** (for sum) and **Cout** (for Carry) to the two outputs. Truth table for Half Adder as shown below:-

Table 1: Truth Table for Half Adder operation

Input		Output Desired		Observed	
A	B	S	Cout	S	Cout
0	0	0	0		
0	1	1	0		
1	0	1	0		
1	1	0	1		

The simplified Boolean function for the two outputs can be written from this truth table as:-

$$S = A'.B + A.B'$$

$$Cout = A.B$$

The circuit diagram for the Half Adder to implement above mentioned Boolean function could be quite a few. We will however verify only one.

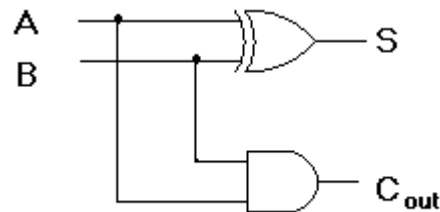


Figure 1: Half Adder using AND and XOR gates.

PROCEDURE

1. Wire the circuit as per figure 2 above.
2. Use any two Logic Switches of the trainer (S2 to S9) for the input and any two of the LEDs of the trainer (L0 to L15) as output indication.
3. Connect +5V to pin 14 (Vcc) and Ground to pin 7 (GND) of the ICs.
4. By setting various combinations of the two switches verify that the output of the circuit is in accordance with the Truth Table shown above. Record your observation.

TASK 2: FULL ADDER

As mentioned in the beginning, a full-adder is a combinational circuit that forms the arithmetic sum of three input bits (two significant bits and a previous carry bit) and two output bits. We arbitrarily assign symbols **A** and **B** to the two significant bit inputs and **C_{in}** for the Carry from the previous lower significant position, and **S** (for sum) and **C_{out}** (for Carry) to the two outputs.

Truth table for the Full Adder is shown below:

Input			Output Desired		Output Observed	
A	B	Cin	S	Cout	S	Cout
0	0	0	0	0		
0	0	1	1	0		
0	1	0	1	0		
0	1	1	0	1		
1	0	0	1	0		
1	0	1	0	1		
1	1	0	0	1		
1	1	1	1	1		

Simplified Boolean function for the two outputs can be written from this truth table as:-

$$S = A \oplus B \oplus C_{in}$$

$$C_{out} = (A \oplus B) C_{in} + A.B$$

The circuit diagram for the Full Adder is as under:

EXPERIMENT NO 3

IMPLEMENTATION OF HALF ADDER AND FULL ADDER

OBJECTIVE

To study Half and Full adder operations.

THEORY

Digital computers perform a variety of information-processing tasks. Among the basic functions encountered are various arithmetic operations. The most basic arithmetic operations are, no doubt, the addition and subtraction of binary digits (bit).

HALF ADDER

The possible operations, when we want to add only two bits, would be the followings:

$$0 + 0 = 0 \quad 0 + 1 = 1$$

$$1 + 0 = 1$$

$$1 + 1 = 0 \quad \& \quad \text{Carry } 1$$

Above mentioned operation could be performed by a **Half Adder** circuit.

FULL ADDER

We know that in practice, all addition operations must take into account the Carry bit (or digit) from the previous operation.

computers also account the last operation the Augend and the present

Input		Output Desired		Observed	
A	B	S	Cout	S	Cout
0	0	0	0		
0	1	1	0		
1	0	1	0		
1	1	0	1		

Adders in digital take into Carry bit from and add it with Addend bits of operation to

complete the addition operation. The possible operations are:

$$0 + 0 + 0 \text{ (carry)} = 0$$

$$0 + 0 + 1 \text{ (carry)} = 1 \quad 0 + 1 + 0 \text{ (carry)} = 1$$

$$0 + 1 + 1 \text{ (carry)} = 0 \quad \& \text{ carry } 1 \text{ (to be added to next higher digit)}$$

$$1 + 1 + 0 \text{ (carry)} = 0 \quad \& \text{ carry } 1 \text{ (to be added to next higher digit)}$$

$$1 + 1 + 1 \text{ (carry)} = 1 \quad \& \text{ carry } 1 \text{ (to be added to next higher digit)}$$

The adder that performs the addition of three bits (two significant bits and a previous carry) is called a **Full Adder**.

TASK 1: HALF ADDER

We arbitrarily assign symbols **A** and **B** to the two inputs and **S** (for sum) and **Cout** (for Carry) to the two outputs. Truth table for Half Adder as shown below:-

Table 1: Truth Table for Half Adder operation

The simplified Boolean function for the two outputs can be written from this truth table as:-

$$\mathbf{S = A'.B + A.B'}$$

$$\mathbf{Cout = A.B}$$

The circuit diagram for the Half Adder to implement above mentioned Boolean function

could be quite a few. We will however verify only one.

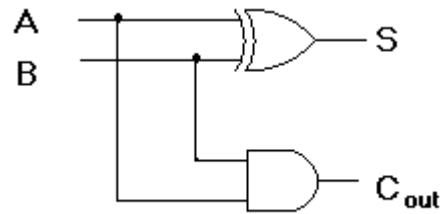


Figure 1: Half Adder using AND and XOR gates.

PROCEDURE

1. Wire the circuit as per figure 2 above.
2. Use any two Logic Switches of the trainer (S2 to S9) for the input and any two of the LEDs of the trainer (L0 to L15) as output indication.
3. Connect +5V to pin 14 (Vcc) and Ground to pin 7 (GND) of the ICs.
4. By setting various combinations of the two switches verify that the output of the circuit is in accordance with the Truth Table shown above. Record your observation.

TASK 2: FULL ADDER

As mentioned in the beginning, a full-adder is a combinational circuit that forms the arithmetic sum of three input bits (two significant bits and a previous carry bit) and two output bits. We arbitrarily assign symbols **A** and **B** to the two significant bit inputs and **C_{in}** for the Carry from the previous lower significant position, and **S** (for sum) and **C_{out}** (for Carry) to the two outputs. Truth table for the Full Adder is shown below:

Input			Output Desired		Output Observed	
A	B	C _{in}	S	C _{out}	S	C _{out}
0	0	0	0	0		
0	0	1	1	0		
0	1	0	1	0		
0	1	1	0	1		
1	0	0	1	0		
1	0	1	0	1		
1	1	0	0	1		
1	1	1	1	1		

Simplified Boolean function for the two outputs can be written from this truth table as:-

$\oplus \oplus$

$$S = A \oplus B \oplus C_{in}$$

$$C_{out} = (A \oplus B) C_{in} + A \cdot B$$

The circuit diagram for the Full Adder is as under:

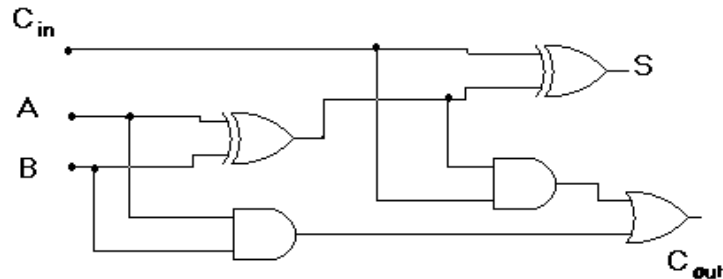


Figure 2: Full Adder comprising of two Half Adders and an OR gate.

PROCEDURE

1. Wire the circuit as per figure 2 above.
2. Use any three Logic Switches of the trainer (S2 to S9) for the input and any two of the LEDs of the trainer (L0 to L15) as output indication.
3. Connect +5V to pin 14 (Vcc) and Ground to pin 7 (GND) of the ICs.
4. By setting various combinations of the two switches verify that the output of the circuit is in accordance with the Truth Table shown above. Record your observation.

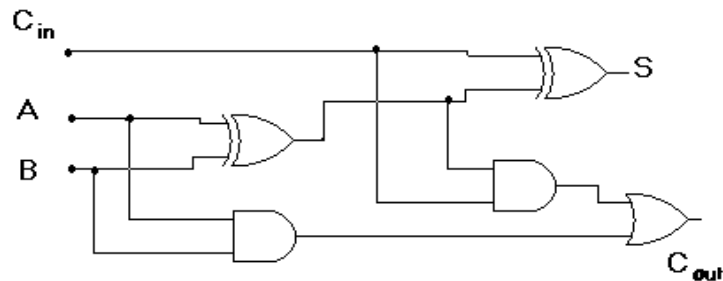


Figure 2: Full Adder comprising of two Half Adders and an OR gate.

PROCEDURE

1. Wire the circuit as per figure 2 above.
2. Use any three Logic Switches of the trainer (S2 to S9) for the input and any two of the LEDs of the trainer (L0 to L15) as output indication.

3. Connect +5V to pin 14 (Vcc) and Ground to pin 7 (GND) of the ICs.
4. By setting various combinations of the two switches verify that the output of the circuit is in accordance with the Truth Table shown above. Record your observation.