

EXPERIMENT NO 5

TO STUDY BASIC LOGIC GATE INTEGRATED CIRCUITS AND VERIFICATION OF THEIR TRUTH TABLES

OBJECTIVES

To understand the different options, facilities and provisions provided on the Digital Logic Trainer

To recognize the different logic gates ICs

To verify the truth tables of basic logic gates

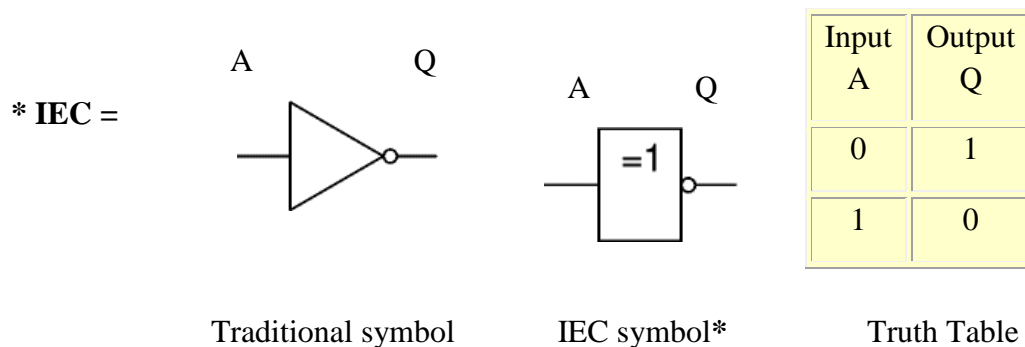
INTRODUCTION

A logic gate is an elementary building block of a digital circuit. Most logic gates have two inputs and one output. At any given moment, every terminal is in one of the two logic states, i.e. LOW/FALSE/ (0) or HIGH/TRUE/ (1), represented by different voltage levels. The logic state of a terminal changes as the circuit processes data. In most logic gates, the LOW state corresponds to zero volts (0 V), while the HIGH state corresponds to positive five volts (+5 V). There are three basic logic gates, i.e. NOT-gate, AND-gate and OR-gate. A combination on these basic gates has given birth to some advanced gates which are widely used, e.g. NAND-gate, NOR-gate, EX-OR (Exclusive OR) gate and EX-NOR (Exclusive NOR) gate.

LOGIC GATE SYMBOLS AND TRUTH-TABLES

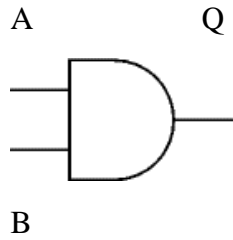
NOT GATE

NOT gate has only one input and one output. The output Q is true when the input A is NOT true, i.e. the output is the inverse of the input, mathematically we write it as $Q = \text{NOT} (A)$. A NOT gate is also called an inverter.

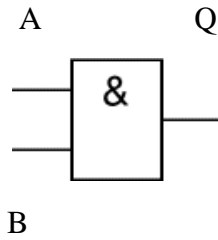


AND GATE

A basic AND gate has two inputs and one output. The output Q is true if **both** the inputs A **AND** B are simultaneously true, mathematically this is stated as $Q = A \text{ AND } B$. Some AND gates can have more than two inputs, in that case the output is true when **ALL** the inputs are true.



Traditional
symbol



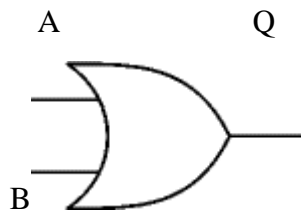
IEC symbol

Input A	Input B	Output Q
0	0	0
0	1	0
1	0	0
1	1	1

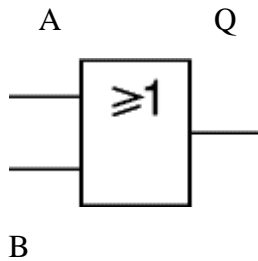
Truth Table

OR GATE

A basic OR gate also has two inputs and one output. The output Q is true if either of the two inputs A OR B is true (or when both of them are true), i.e. $Q = A \text{ OR } B$. Some OR gates can have more than two inputs, in that case, the output is true if at least one input is true.



Traditional symbol



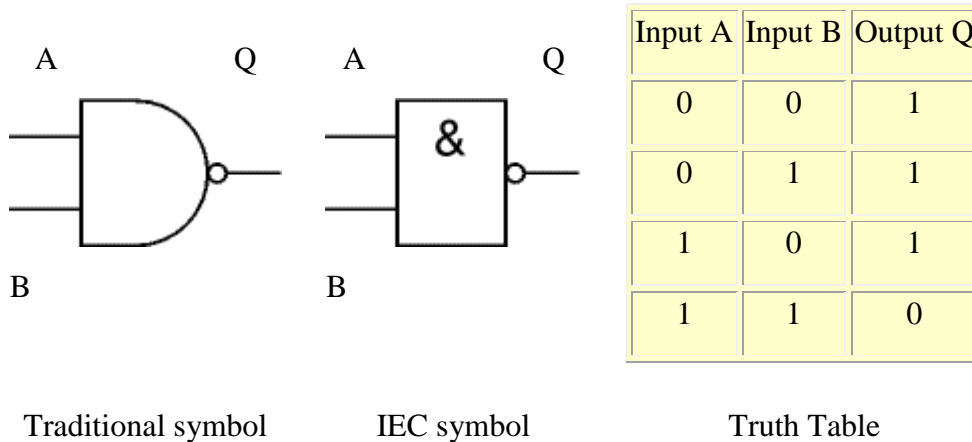
IEC symbol

Input A	Input B	Output Q
0	0	0
0	1	1
1	0	1
1	1	1

Truth Table

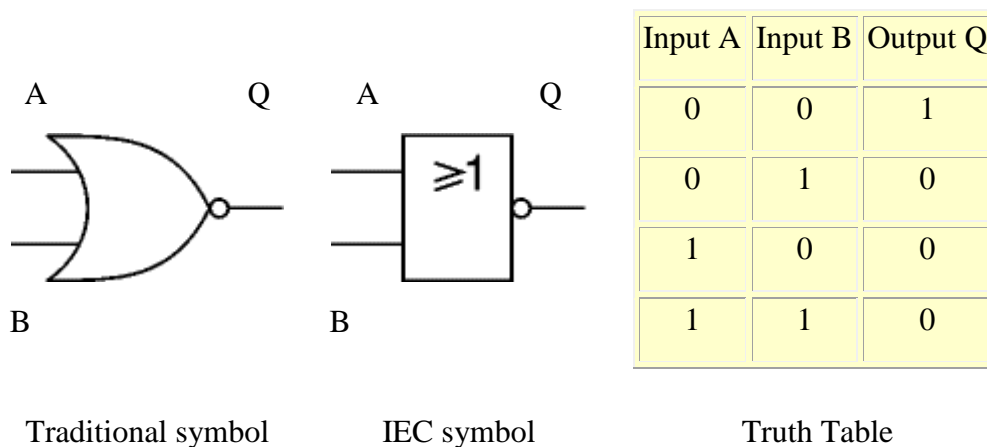
NAND GATE

NAND gate is basically an AND gate but with the output inverted, as shown by the 'o' on the output of the AND gate symbol. Thus the output is true if both the inputs A AND B are NOT true simultaneously, in equation form we can write it as $Q = \text{NOT} (A \text{ AND } B)$. Like AND gates, some NAND gates can have more than two inputs, in that case, the output is true if NOT ALL the inputs are true.



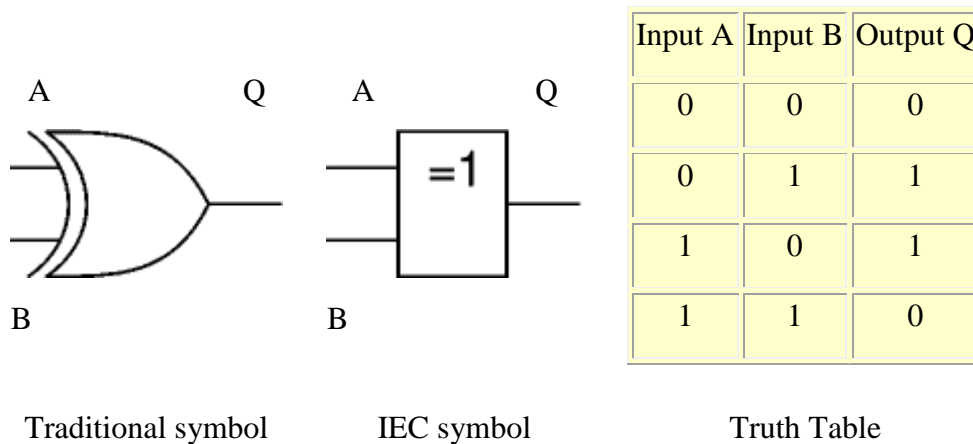
NOR GATE

NOR gate is basically an OR gate but with the output inverted, as shown by the 'o' on the output of the OR gate symbol. Thus the output is true if neither of the inputs A OR B is true, in equation form we can write it as $Q = \text{NOT} (A \text{ OR } B)$. Like OR gates, some NOR gates can have more than two inputs, in that case, the output is true if NONE of the inputs is true.



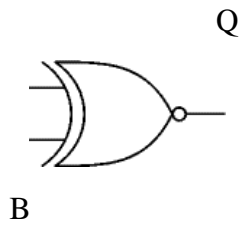
X-OR (EXCLUSIVE-OR) GATE

A basic X-OR gate also has two inputs and one output. The output Q is true if either of the two inputs A OR B (but not both) is true, mathematically it is written as $Q = (A \text{ AND NOT}(B)) \text{ OR } (B \text{ AND NOT}(A))$. Hence it is like an OR gate but excluding the case when both the inputs are true simultaneously, in other words the output is true if the inputs are DIFFERENT. Advanced X-OR gates can have more than two inputs, in that case, the output is true only when an ODD number of inputs are true.

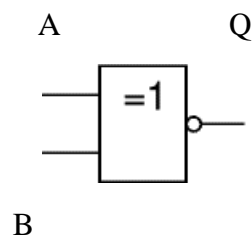


X-NOR (EXCLUSIVE-NOR) GATE

This is equivalent to an X-OR gate with the output inverted, as shown by the 'o' on the output of the X-OR gate symbol. Thus the output Q is true if both the inputs A and B are the same, i.e. either both are true or both are false, in equation form this is described as $Q = (A \text{ AND } B) \text{ OR } (\text{NOT}(A) \text{ AND } \text{NOT}(B))$. Like X-OR, X-NOR gates have more than two inputs, in that case, the output is true when an EVEN number of inputs are true.



Traditional symbol



IEC symbol

Input A	Input B	Output Q
0	0	1
0	1	0
1	0	0
1	1	1

Truth Table

UNIVERSAL GATES

The NAND and NOR gates can be said to be universal gates, since combinations of them can be used to accomplish any of the basic operations and can, thus produce an inverter, an OR gate or an AND gate. The non-inverting gates do not have this versatility since they can't produce an inversion.

COMPONENTS

1. Power supply

2. Components (ICs):

74LS00 (NAND Gate)	-----	1
74LS02 (AND Gate)	-----	1
74LS04 (NOT Gate)	-----	1
74LS08 (AND Gate)	-----	1
74LS32 (OR Gate)	-----	1
74LS86 (EX-OR Gate)	-----	1

3. Connecting wires

4. Bread board

5. LED

PROCEDURE

1. Connect the DC power supply to 220V Ac power supply.
2. Turn on the DC power supply and verify the DC voltage by using voltmeter, it should be almost 5.0 volts (specifically between 4.75V – 5.25V). If not consult the Lab Supervisor.

3. Install the IC chip under experiment, on breadboard.
4. Connect the +Vcc (pin # 14) and Ground (pin # 7) pins of the IC to +5V and Ground supply of the trainer board. (Consult Fig 1.2 for the pin diagrams of the IC under test)
5. Make the appropriate circuit connections as shown in Fig 1.1(a, b, c,e,f) for the particular IC under test. Use logic switches to provide “0” and “1” at the inputs and use the trainer’s LEDs to display the output. Note that there is more than one gate in each IC chip, so you can use any one of these gates to make your connections (Consult Fig 1.2 for the pin numbers corresponding to each gate in that particular chip).
6. Record your observations according to Table 2.1 and verify whether the output conform to the truth tables of each gate.
7. Repeat steps 3-6 for each of the IC chips.
8. Write down your observations & comments at the end, as per your concept developed during this experimental work.

CIRCUIT DIAGRAMS

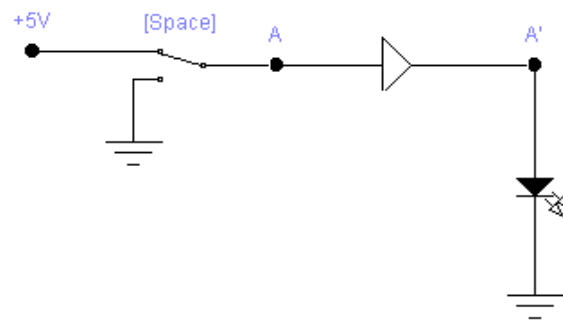


Fig 1.1 (a) NOT Gate (7404)

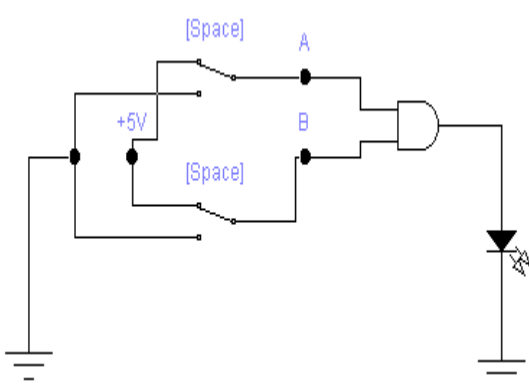


Fig 1.1 (b) AND Gate (74LS08)

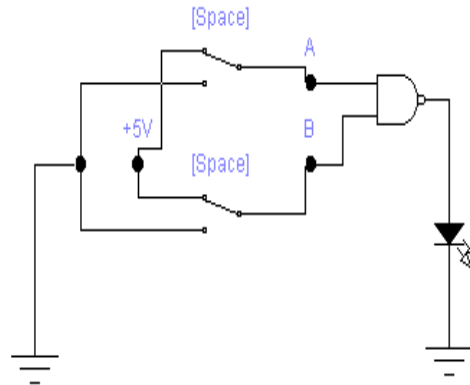


Fig 1.1 (c) NAND Gate (74LS00)

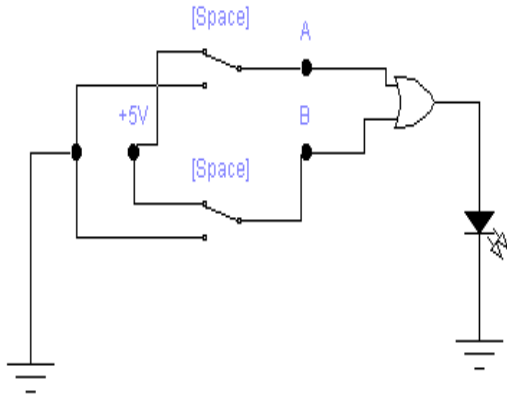


Fig 1.1 (d) OR neither Gate (74LS32)

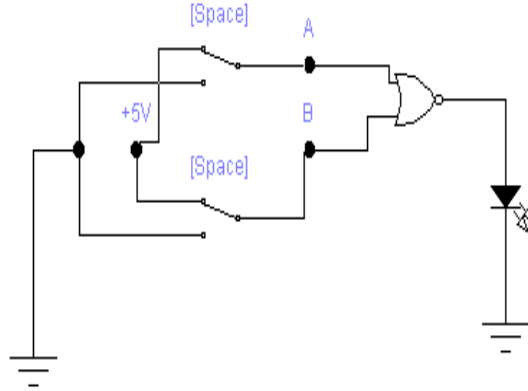
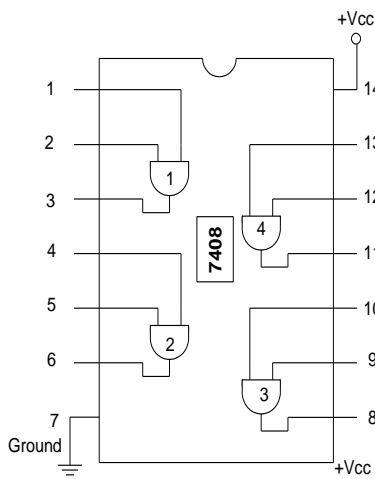
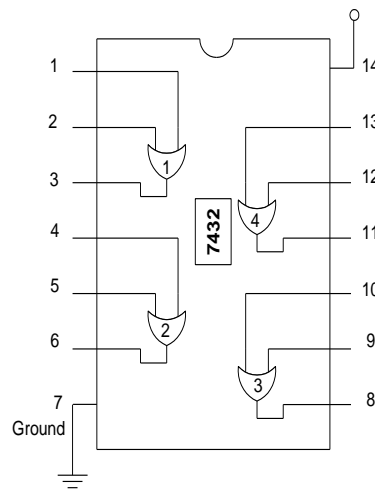


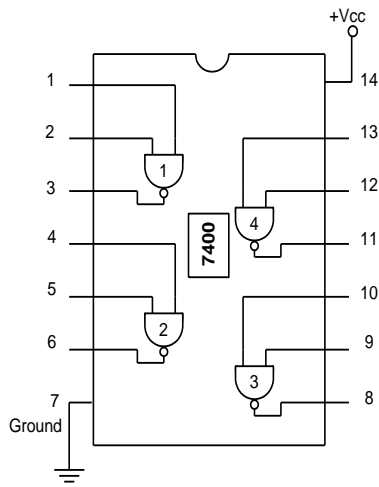
Fig 1.1 (e) NOR Gate (74LS02)



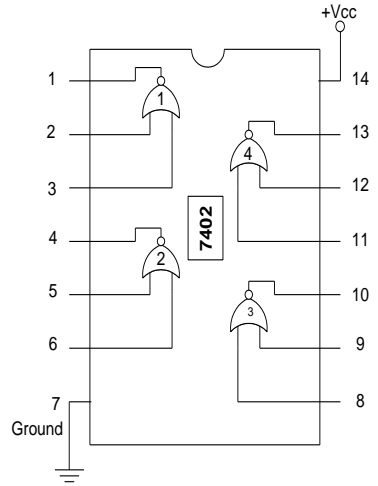
AND GATE



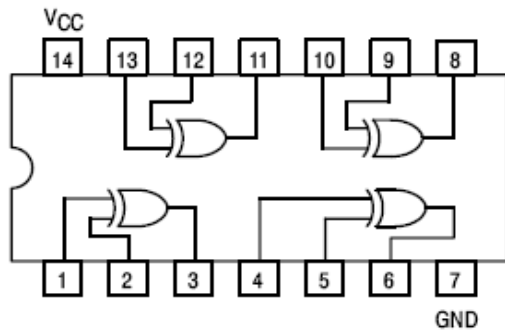
OR GATE



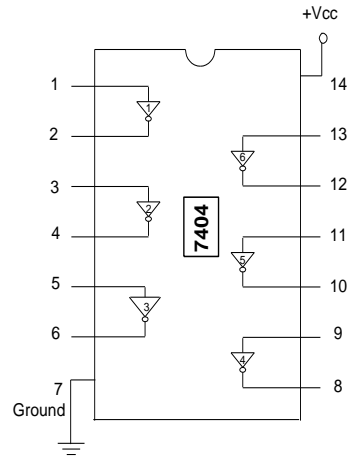
NAND GATE



NOR GATE



EX-OR GATE



NOT GATE

Fig 1.2: Pin Diagrams of IC's

EXPERIMENTAL RESULTS

Table 1.3 Truth Tables of Different Logic Gates

Input A	Output Q
0	
1	

NOT GATE

Input A	Input B	Output Q
0	0	
0	1	
1	0	
1	1	

OR GATE

Input A	Input B	Output Q
	0	
0	1	
1	0	
1	1	

AND GATE

Input A	Input B	Output Q
0	0	
0	1	
1	0	
1	1	

NOR GATE

Input A	Input B	Output Q
0	0	
0	1	
1	0	
1	1	

NAND GATE

Input A	Input B	Output Q
0	0	
0	1	
1	0	
1	1	

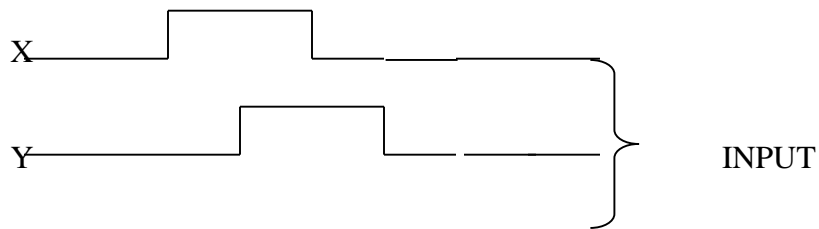
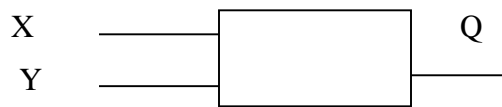
EX-OR GATE

PRECAUTIONS

- Check the power supply for correct voltage.
- Check the Vcc (pin # 14) and Ground (pin # 7) connections of the IC under test.
- Check all the wire connections and remove any possible breaks.
- Check the IC under test using truth table.

QUESTIONS

The input/output signals are shown by means of the following diagram. Corresponding to the Input X and Y given below; Draw waveform for given gates.



AND

OR

NOT