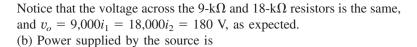


**Figure 2.44** For Example 2.13: (a) original circuit, (b) its equivalent circuit.



$$p_o = v_o i_o = 180(30) \text{ mW} = 5.4 \text{ W}$$

(c) Power absorbed by the 12-k $\Omega$  resistor is

$$p = iv = i_2(i_2R) = i_2^2R = (10 \times 10^{-3})^2 (12,000) = 1.2 \text{ W}$$

Power absorbed by the 6-k $\Omega$  resistor is

$$p = i_2^2 R = (10 \times 10^{-3})^2 (6,000) = 0.6 \text{ W}$$

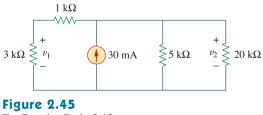
Power absorbed by the 9-k $\Omega$  resistor is

$$p = \frac{v_o^2}{R} = \frac{(180)^2}{9.000} = 3.6 \text{ W}$$

$$p = v_o i_1 = 180(20) \text{ mW} = 3.6 \text{ W}$$

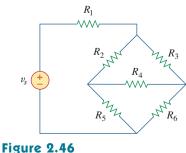
Notice that the power supplied (5.4 W) equals the power absorbed (1.2 + 0.6 + 3.6 = 5.4 W). This is one way of checking results.

**Practice Problem 2.13** For the circuit shown in Fig. 2.45, find: (a)  $v_1$  and  $v_2$ , (b) the power dissipated in the 3-k $\Omega$  and 20-k $\Omega$  resistors, and (c) the power supplied by the current source.



For Practice Prob. 2.13.

Answer: (a) 45 V, 60 V, (b) 675 mW, 180 mW, (c) 1.8 W.



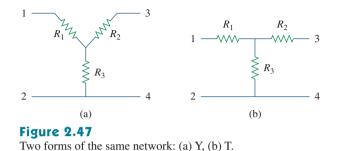
The bridge network.

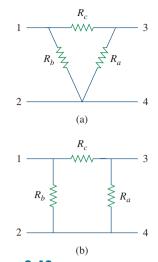
# 2.7 <sup>†</sup>Wye-Delta Transformations

Situations often arise in circuit analysis when the resistors are neither in parallel nor in series. For example, consider the bridge circuit in Fig. 2.46. How do we combine resistors  $R_1$  through  $R_6$  when the resistors are neither in series nor in parallel? Many circuits of the type shown in Fig. 2.46 can be simplified by using three-terminal equivalent networks. These are

or

the wye (Y) or tee (T) network shown in Fig. 2.47 and the delta ( $\Delta$ ) or pi ( $\Pi$ ) network shown in Fig. 2.48. These networks occur by themselves or as part of a larger network. They are used in three-phase networks, electrical filters, and matching networks. Our main interest here is in how to identify them when they occur as part of a network and how to apply wye-delta transformation in the analysis of that network.





**Figure 2.48** Two forms of the same network: (a)  $\Delta$ , (b)  $\Pi$ .

## Delta to Wye Conversion

Suppose it is more convenient to work with a wye network in a place where the circuit contains a delta configuration. We superimpose a wye network on the existing delta network and find the equivalent resistances in the wye network. To obtain the equivalent resistances in the wye network, we compare the two networks and make sure that the resistance between each pair of nodes in the  $\Delta$  (or  $\Pi$ ) network is the same as the resistance between the same pair of nodes in the Y (or T) network. For terminals 1 and 2 in Figs. 2.47 and 2.48, for example,

$$R_{12}(Y) = R_1 + R_3$$

$$R_{12}(\Delta) = R_b \parallel (R_a + R_c)$$
(2.46)

Setting  $R_{12}(Y) = R_{12}(\Delta)$  gives

$$R_{12} = R_1 + R_3 = \frac{R_b(R_a + R_c)}{R_a + R_b + R_c}$$
 (2.47a)

Similarly,

$$R_{13} = R_1 + R_2 = \frac{R_c(R_a + R_b)}{R_a + R_b + R_c}$$
 (2.47b)

$$R_{34} = R_2 + R_3 = \frac{R_a(R_b + R_c)}{R_a + R_b + R_c}$$
(2.47c)

Subtracting Eq. (2.47c) from Eq. (2.47a), we get

$$R_1 - R_2 = \frac{R_c(R_b - R_a)}{R_a + R_b + R_c}$$
(2.48)

Adding Eqs. (2.47b) and (2.48) gives

$$R_1 = \frac{R_b R_c}{R_a + R_b + R_c}$$
(2.49)

and subtracting Eq. (2.48) from Eq. (2.47b) yields

$$R_2 = \frac{R_c R_a}{R_a + R_b + R_c}$$
(2.50)

Subtracting Eq. (2.49) from Eq. (2.47a), we obtain

$$R_3 = \frac{R_a R_b}{R_a + R_b + R_c}$$
(2.51)

We do not need to memorize Eqs. (2.49) to (2.51). To transform a  $\Delta$  network to Y, we create an extra node *n* as shown in Fig. 2.49 and follow this conversion rule:

Each resistor in the Y network is the product of the resistors in the two adjacent  $\Delta$  branches, divided by the sum of the three  $\Delta$  resistors.

One can follow this rule and obtain Eqs. (2.49) to (2.51) from Fig. 2.49.

## Wye to Delta Conversion

To obtain the conversion formulas for transforming a wye network to an equivalent delta network, we note from Eqs. (2.49) to (2.51) that

$$R_{1}R_{2} + R_{2}R_{3} + R_{3}R_{1} = \frac{R_{a}R_{b}R_{c}(R_{a} + R_{b} + R_{c})}{(R_{a} + R_{b} + R_{c})^{2}}$$

$$= \frac{R_{a}R_{b}R_{c}}{R_{a} + R_{b} + R_{c}}$$
(2.52)

Dividing Eq. (2.52) by each of Eqs. (2.49) to (2.51) leads to the following equations:

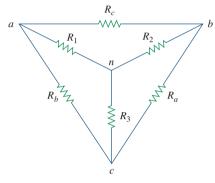
$$R_a = \frac{R_1 R_2 + R_2 R_3 + R_3 R_1}{R_1}$$
(2.53)

$$R_b = \frac{R_1 R_2 + R_2 R_3 + R_3 R_1}{R_2}$$
(2.54)

$$R_c = \frac{R_1 R_2 + R_2 R_3 + R_3 R_1}{R_3}$$
(2.55)

From Eqs. (2.53) to (2.55) and Fig. 2.49, the conversion rule for Y to  $\Delta$  is as follows:

Each resistor in the  $\Delta$  network is the sum of all possible products of Y resistors taken two at a time, divided by the opposite Y resistor.



### Figure 2.49

Superposition of Y and  $\Delta$  networks as an aid in transforming one to the other.

The Y and  $\Delta$  networks are said to be *balanced* when

$$R_1 = R_2 = R_3 = R_Y, \qquad R_a = R_b = R_c = R_\Delta$$
 (2.56)

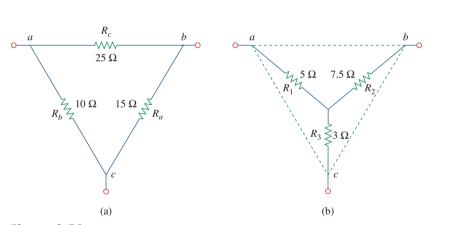
Under these conditions, conversion formulas become

$$R_{\rm Y} = \frac{R_{\Delta}}{3}$$
 or  $R_{\Delta} = 3R_{\rm Y}$  (2.57)

One may wonder why  $R_Y$  is less than  $R_\Delta$ . Well, we notice that the Y-connection is like a "series" connection while the  $\Delta$ -connection is like a "parallel" connection.

Note that in making the transformation, we do not take anything out of the circuit or put in anything new. We are merely substituting different but mathematically equivalent three-terminal network patterns to create a circuit in which resistors are either in series or in parallel, allowing us to calculate  $R_{eq}$  if necessary.

Convert the  $\Delta$  network in Fig. 2.50(a) to an equivalent Y network.



**Figure 2.50** For Example 2.14: (a) original  $\Delta$  network, (b) Y equivalent network.

### Solution:

Using Eqs. (2.49) to (2.51), we obtain

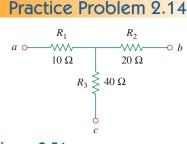
$$R_{1} = \frac{R_{b}R_{c}}{R_{a} + R_{b} + R_{c}} = \frac{10 \times 25}{15 + 10 + 25} = \frac{250}{50} = 5 \Omega$$

$$R_{2} = \frac{R_{c}R_{a}}{R_{a} + R_{b} + R_{c}} = \frac{25 \times 15}{50} = 7.5 \Omega$$

$$R_{3} = \frac{R_{a}R_{b}}{R_{a} + R_{b} + R_{c}} = \frac{15 \times 10}{50} = 3 \Omega$$

The equivalent Y network is shown in Fig. 2.50(b).

Example 2.14



Transform the wye network in Fig. 2.51 to a delta network.

Answer:  $R_a = 140 \Omega$ ,  $R_b = 70 \Omega$ ,  $R_c = 35 \Omega$ .

Figure 2.51 For Practice Prob. 2.14.

## Example 2.15

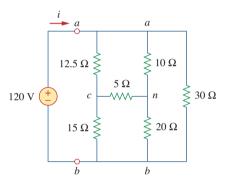


Figure 2.52 For Example 2.15.

Obtain the equivalent resistance  $R_{ab}$  for the circuit in Fig. 2.52 and use it to find current *i*.

### Solution:

- 1. **Define.** The problem is clearly defined. Please note, this part normally will deservedly take much more time.
- 2. **Present.** Clearly, when we remove the voltage source, we end up with a purely resistive circuit. Since it is composed of deltas and wyes, we have a more complex process of combining the elements together. We can use wye-delta transformations as one approach to find a solution. It is useful to locate the wyes (there are two of them, one at *n* and the other at *c*) and the deltas (there are three: *can, abn, cnb*).
- 3. Alternative. There are different approaches that can be used to solve this problem. Since the focus of Sec. 2.7 is the wye-delta transformation, this should be the technique to use. Another approach would be to solve for the equivalent resistance by injecting one amp into the circuit and finding the voltage between *a* and *b*; we will learn about this approach in Chap. 4.

The approach we can apply here as a check would be to use a wye-delta transformation as the first solution to the problem. Later we can check the solution by starting with a delta-wye transformation.

4. Attempt. In this circuit, there are two Y networks and three  $\Delta$  networks. Transforming just one of these will simplify the circuit. If we convert the Y network comprising the 5- $\Omega$ , 10- $\Omega$ , and 20- $\Omega$  resistors, we may select

$$R_1 = 10 \,\Omega, \qquad R_2 = 20 \,\Omega, \qquad R_3 = 5 \,\Omega$$

Thus from Eqs. (2.53) to (2.55) we have

$$R_{a} = \frac{R_{1}R_{2} + R_{2}R_{3} + R_{3}R_{1}}{R_{1}} = \frac{10 \times 20 + 20 \times 5 + 5 \times 10}{10}$$
$$= \frac{350}{10} = 35 \Omega$$
$$R_{b} = \frac{R_{1}R_{2} + R_{2}R_{3} + R_{3}R_{1}}{R_{2}} = \frac{350}{20} = 17.5 \Omega$$
$$R_{c} = \frac{R_{1}R_{2} + R_{2}R_{3} + R_{3}R_{1}}{R_{3}} = \frac{350}{5} = 70 \Omega$$

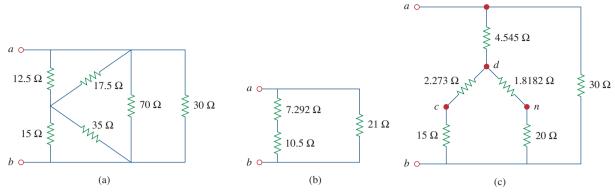


Figure 2.53 Equivalent circuits to Fig. 2.52, with the voltage source removed.

With the Y converted to  $\Delta$ , the equivalent circuit (with the voltage source removed for now) is shown in Fig. 2.53(a). Combining the three pairs of resistors in parallel, we obtain

$$70 \parallel 30 = \frac{70 \times 30}{70 + 30} = 21 \ \Omega$$
$$12.5 \parallel 17.5 = \frac{12.5 \times 17.5}{12.5 + 17.5} = 7.292 \ \Omega$$
$$15 \parallel 35 = \frac{15 \times 35}{15 + 35} = 10.5 \ \Omega$$

so that the equivalent circuit is shown in Fig. 2.53(b). Hence, we find

$$R_{ab} = (7.292 + 10.5) \| 21 = \frac{17.792 \times 21}{17.792 + 21} = 9.632 \Omega$$

Then

$$i = \frac{v_s}{R_{ab}} = \frac{120}{9.632} = 12.458 \,\mathrm{A}$$

We observe that we have successfully solved the problem. Now we must evaluate the solution.

5. Evaluate. Now we must determine if the answer is correct and then evaluate the final solution.

It is relatively easy to check the answer; we do this by solving the problem starting with a delta-wye transformation. Let us transform the delta, *can*, into a wye.

Let  $R_c = 10 \Omega$ ,  $R_a = 5 \Omega$ , and  $R_n = 12.5 \Omega$ . This will lead to (let *d* represent the middle of the wye):

$$R_{ad} = \frac{R_c R_n}{R_a + R_c + R_n} = \frac{10 \times 12.5}{5 + 10 + 12.5} = 4.545 \,\Omega$$
$$R_{cd} = \frac{R_a R_n}{27.5} = \frac{5 \times 12.5}{27.5} = 2.273 \,\Omega$$
$$R_{nd} = \frac{R_a R_c}{27.5} = \frac{5 \times 10}{27.5} = 1.8182 \,\Omega$$

This now leads to the circuit shown in Figure 2.53(c). Looking at the resistance between d and b, we have two series combination in parallel, giving us

$$R_{db} = \frac{(2.273 + 15)(1.8182 + 20)}{2.273 + 15 + 1.8182 + 20} = \frac{376.9}{39.09} = 9.642 \ \Omega$$

This is in series with the 4.545- $\Omega$  resistor, both of which are in parallel with the 30- $\Omega$  resistor. This then gives us the equivalent resistance of the circuit.

$$R_{ab} = \frac{(9.642 + 4.545)30}{9.642 + 4.545 + 30} = \frac{425.6}{44.19} = 9.631 \,\Omega$$

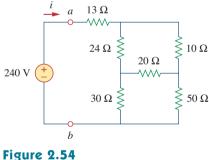
This now leads to

$$i = \frac{v_s}{R_{ab}} = \frac{120}{9.631} = 12.46$$
 A

We note that using two variations on the wye-delta transformation leads to the same results. This represents a very good check.

6. **Satisfactory?** Since we have found the desired answer by determining the equivalent resistance of the circuit first and the answer checks, then we clearly have a satisfactory solution. This represents what can be presented to the individual assigning the problem.

## Practice Problem 2.15



For Practice Prob. 2.15.

So far, we have assumed that connecting wires are perfect conductors (i.e., conductors of zero resistance). In real physical systems, however, the resistance of the connecting wire may be appreciably large, and the modeling of the system must include that resistance. Answer:  $40 \Omega$ , 6 A.

2.8

# <sup>†</sup>Applications

For the bridge network in Fig. 2.54, find  $R_{ab}$  and *i*.

Resistors are often used to model devices that convert electrical energy into heat or other forms of energy. Such devices include conducting wire, light bulbs, electric heaters, stoves, ovens, and loudspeakers. In this section, we will consider two real-life problems that apply the concepts developed in this chapter: electrical lighting systems and design of dc meters.

## 2.8.1 Lighting Systems

Lighting systems, such as in a house or on a Christmas tree, often consist of N lamps connected either in parallel or in series, as shown in Fig. 2.55. Each lamp is modeled as a resistor. Assuming that all the lamps are identical and  $V_o$  is the power-line voltage, the voltage across each lamp is  $V_o$  for the parallel connection and  $V_o/N$  for the series connection. The series connection is easy to manufacture but is seldom used in practice, for at least two reasons. First, it is less reliable; when a lamp fails, all the lamps go out. Second, it is harder to maintain; when a lamp is bad, one must test all the lamps one by one to detect the faulty one.

## chapter

# Methods of Analysis

No great work is ever done in a hurry. To develop a great scientific discovery, to print a great picture, to write an immortal poem, to become a minister, or a famous general—to do anything great requires time, patience, and perseverance. These things are done by degrees, "little by little."

-W. J. Wilmont Buxton

## **Enhancing Your Career**

### **Career in Electronics**

One area of application for electric circuit analysis is electronics. The term *electronics* was originally used to distinguish circuits of very low current levels. This distinction no longer holds, as power semiconductor devices operate at high levels of current. Today, electronics is regarded as the science of the motion of charges in a gas, vacuum, or semiconductor. Modern electronics involves transistors and transistor circuits. The earlier electronic circuits were assembled from components. Many electronic circuits are now produced as integrated circuits, fabricated in a semiconductor substrate or chip.

Electronic circuits find applications in many areas, such as automation, broadcasting, computers, and instrumentation. The range of devices that use electronic circuits is enormous and is limited only by our imagination. Radio, television, computers, and stereo systems are but a few.

An electrical engineer usually performs diverse functions and is likely to use, design, or construct systems that incorporate some form of electronic circuits. Therefore, an understanding of the operation and analysis of electronics is essential to the electrical engineer. Electronics has become a specialty distinct from other disciplines within electrical engineering. Because the field of electronics is ever advancing, an electronics engineer must update his/her knowledge from time to time. The best way to do this is by being a member of a professional organization such as the Institute of Electrical and Electronics Engineers (IEEE). With a membership of over 300,000, the IEEE is the largest professional organization in the world. Members benefit immensely from the numerous magazines, journals, transactions, and conference/symposium proceedings published yearly by IEEE. You should consider becoming an IEEE member.



Troubleshooting an electronic circuit board. © BrandX Pictures/Punchstock

## **3.1** Introduction

Having understood the fundamental laws of circuit theory (Ohm's law and Kirchhoff's laws), we are now prepared to apply these laws to develop two powerful techniques for circuit analysis: nodal analysis, which is based on a systematic application of Kirchhoff's current law (KCL), and mesh analysis, which is based on a systematic application of Kirchhoff's voltage law (KVL). The two techniques are so important that this chapter should be regarded as the most important in the book. Students are therefore encouraged to pay careful attention.

With the two techniques to be developed in this chapter, we can analyze any linear circuit by obtaining a set of simultaneous equations that are then solved to obtain the required values of current or voltage. One method of solving simultaneous equations involves Cramer's rule, which allows us to calculate circuit variables as a quotient of determinants. The examples in the chapter will illustrate this method; Appendix A also briefly summarizes the essentials the reader needs to know for applying Cramer's rule. Another method of solving simultaneous equations is to use *MATLAB*, a computer software discussed in Appendix E.

Also in this chapter, we introduce the use of *PSpice for Windows*, a circuit simulation computer software program that we will use throughout the text. Finally, we apply the techniques learned in this chapter to analyze transistor circuits.

## **3.2** Nodal Analysis

Nodal analysis provides a general procedure for analyzing circuits using node voltages as the circuit variables. Choosing node voltages instead of element voltages as circuit variables is convenient and reduces the number of equations one must solve simultaneously.

To simplify matters, we shall assume in this section that circuits do not contain voltage sources. Circuits that contain voltage sources will be analyzed in the next section.

In *nodal analysis*, we are interested in finding the node voltages. Given a circuit with *n* nodes without voltage sources, the nodal analysis of the circuit involves taking the following three steps.

## Steps to Determine Node Voltages:

- 1. Select a node as the reference node. Assign voltages  $v_1$ ,  $v_2, \ldots, v_{n-1}$  to the remaining n-1 nodes. The voltages are referenced with respect to the reference node.
- 2. Apply KCL to each of the n 1 nonreference nodes. Use Ohm's law to express the branch currents in terms of node voltages.
- 3. Solve the resulting simultaneous equations to obtain the unknown node voltages.

We shall now explain and apply these three steps.

The first step in nodal analysis is selecting a node as the *reference* or *datum node*. The reference node is commonly called the *ground* 

Nodal analysis is also known as the *node-voltage method*.

since it is assumed to have zero potential. A reference node is indicated by any of the three symbols in Fig. 3.1. The type of ground in Fig. 3.1(c) is called a *chassis ground* and is used in devices where the case, enclosure, or chassis acts as a reference point for all circuits. When the potential of the earth is used as reference, we use the *earth ground* in Fig. 3.1(a) or (b). We shall always use the symbol in Fig. 3.1(b).

Once we have selected a reference node, we assign voltage designations to nonreference nodes. Consider, for example, the circuit in Fig. 3.2(a). Node 0 is the reference node (v = 0), while nodes 1 and 2 are assigned voltages  $v_1$  and  $v_2$ , respectively. Keep in mind that the node voltages are defined with respect to the reference node. As illustrated in Fig. 3.2(a), each node voltage is the voltage rise from the reference node to the corresponding nonreference node or simply the voltage of that node with respect to the reference node.

As the second step, we apply KCL to each nonreference node in the circuit. To avoid putting too much information on the same circuit, the circuit in Fig. 3.2(a) is redrawn in Fig. 3.2(b), where we now add  $i_1, i_2$ , and  $i_3$  as the currents through resistors  $R_1, R_2$ , and  $R_3$ , respectively. At node 1, applying KCL gives

$$I_1 = I_2 + i_1 + i_2 \tag{3.1}$$

At node 2,

$$I_2 + i_2 = i_3 \tag{3.2}$$

We now apply Ohm's law to express the unknown currents  $i_1$ ,  $i_2$ , and  $i_3$  in terms of node voltages. The key idea to bear in mind is that, since resistance is a passive element, by the passive sign convention, current must always flow from a higher potential to a lower potential.

Current flows from a higher potential to a lower potential in a resistor.

We can express this principle as

$$i = \frac{v_{\text{higher}} - v_{\text{lower}}}{R}$$
(3.3)

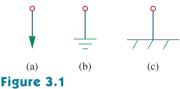
Note that this principle is in agreement with the way we defined resistance in Chapter 2 (see Fig. 2.1). With this in mind, we obtain from Fig. 3.2(b),

$$i_{1} = \frac{v_{1} - 0}{R_{1}} \quad \text{or} \quad i_{1} = G_{1}v_{1}$$

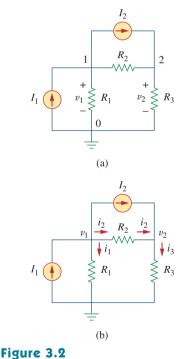
$$i_{2} = \frac{v_{1} - v_{2}}{R_{2}} \quad \text{or} \quad i_{2} = G_{2}(v_{1} - v_{2})$$

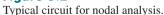
$$i_{3} = \frac{v_{2} - 0}{R_{3}} \quad \text{or} \quad i_{3} = G_{3}v_{2}$$

The number of nonreference nodes is equal to the number of independent equations that we will derive.



Common symbols for indicating a reference node, (a) common ground, (b) ground, (c) chassis ground.





(3.4)

Substituting Eq. (3.4) in Eqs. (3.1) and (3.2) results, respectively, in

$$I_1 = I_2 + \frac{v_1}{R_1} + \frac{v_1 - v_2}{R_2}$$
(3.5)

$$I_2 + \frac{v_1 - v_2}{R_2} = \frac{v_2}{R_3}$$
(3.6)

In terms of the conductances, Eqs. (3.5) and (3.6) become

$$I_1 = I_2 + G_1 v_1 + G_2 (v_1 - v_2)$$
(3.7)

$$I_2 + G_2(v_1 - v_2) = G_3 v_2$$
 (3.8)

The third step in nodal analysis is to solve for the node voltages. If we apply KCL to n-1 nonreference nodes, we obtain n-1 simultaneous equations such as Eqs. (3.5) and (3.6) or (3.7) and (3.8). For the circuit of Fig. 3.2, we solve Eqs. (3.5) and (3.6) or (3.7) and (3.8) to obtain the node voltages  $v_1$  and  $v_2$  using any standard method, such as the substitution method, the elimination method, Cramer's rule, or matrix inversion. To use either of the last two methods, one must cast the simultaneous equations in matrix form. For example, Eqs. (3.7) and (3.8) can be cast in matrix form as

$$\begin{bmatrix} G_1 + G_2 & -G_2 \\ -G_2 & G_2 + G_3 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} I_1 - I_2 \\ I_2 \end{bmatrix}$$
(3.9)

which can be solved to get  $v_1$  and  $v_2$ . Equation 3.9 will be generalized in Section 3.6. The simultaneous equations may also be solved using calculators or with software packages such as MATLAB, Mathcad, Maple, and Quattro Pro.

Calculate the node voltages in the circuit shown in Fig. 3.3(a).

### Solution:

or

or

Consider Fig. 3.3(b), where the circuit in Fig. 3.3(a) has been prepared for nodal analysis. Notice how the currents are selected for the application of KCL. Except for the branches with current sources, the labeling of the currents is arbitrary but consistent. (By consistent, we mean that if, for example, we assume that  $i_2$  enters the 4- $\Omega$  resistor from the left-hand side,  $i_2$  must leave the resistor from the right-hand side.) The reference node is selected, and the node voltages  $v_1$  and  $v_2$ are now to be determined.

At node 1, applying KCL and Ohm's law gives

$$i_1 = i_2 + i_3 \implies 5 = \frac{v_1 - v_2}{4} + \frac{v_1 - 0}{2}$$

Multiplying each term in the last equation by 4, we obtain

$$20 = v_1 - v_2 + 2v_1$$

$$3v_1 - v_2 = 20$$
 (3.1.1)

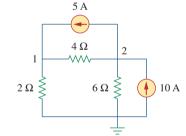
At node 2, we do the same thing and get

$$i_2 + i_4 = i_1 + i_5 \implies \frac{v_1 - v_2}{4} + 10 = 5 + \frac{v_2 - 0}{6}$$

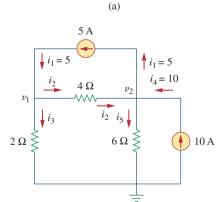
Multiplying each term by 12 results in

$$3v_1 - 3v_2 + 120 = 60 + 2v_2$$

(b)



Example 3.1





Appendix A discusses how to use Cramer's rule.

Now we have two simultaneous Eqs. (3.1.1) and (3.1.2). We can solve the equations using any method and obtain the values of  $v_1$  and  $v_2$ .

**METHOD 1** Using the elimination technique, we add Eqs. (3.1.1) and (3.1.2).

$$4v_2 = 80 \implies v_2 = 20 \text{ V}$$

Substituting  $v_2 = 20$  in Eq. (3.1.1) gives

$$3v_1 - 20 = 20 \implies v_1 = \frac{40}{3} = 13.333 \text{ V}$$

**METHOD 2** To use Cramer's rule, we need to put Eqs. (3.1.1) and (3.1.2) in matrix form as

$$\begin{bmatrix} 3 & -1 \\ -3 & 5 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} 20 \\ 60 \end{bmatrix}$$
(3.1.3)

The determinant of the matrix is

$$\Delta = \begin{vmatrix} 3 & -1 \\ -3 & 5 \end{vmatrix} = 15 - 3 = 12$$

We now obtain  $v_1$  and  $v_2$  as

$$v_{1} = \frac{\Delta_{1}}{\Delta} = \frac{\begin{vmatrix} 20 & -1 \\ 60 & 5 \end{vmatrix}}{\Delta} = \frac{100 + 60}{12} = 13.333 \text{ V}$$
$$v_{2} = \frac{\Delta_{2}}{\Delta} = \frac{\begin{vmatrix} 3 & 20 \\ -3 & 60 \end{vmatrix}}{\Delta} = \frac{180 + 60}{12} = 20 \text{ V}$$

giving us the same result as did the elimination method.

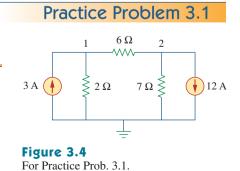
If we need the currents, we can easily calculate them from the values of the nodal voltages.

$$i_1 = 5 \text{ A},$$
  $i_2 = \frac{v_1 - v_2}{4} = -1.6668 \text{ A},$   $i_3 = \frac{v_1}{2} = 6.666 \text{ A}$   
 $i_4 = 10 \text{ A},$   $i_5 = \frac{v_2}{6} = 3.333 \text{ A}$ 

The fact that  $i_2$  is negative shows that the current flows in the direction opposite to the one assumed.

Obtain the node voltages in the circuit of Fig. 3.4.

**Answer:**  $v_1 = -6 \text{ V}, v_2 = -42 \text{ V}.$ 

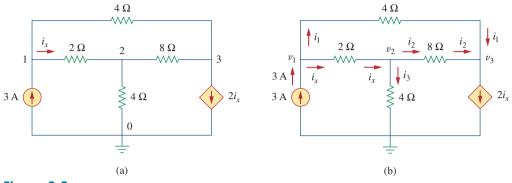


## Example 3.2

Determine the voltages at the nodes in Fig. 3.5(a).

#### **Solution:**

The circuit in this example has three nonreference nodes, unlike the previous example which has two nonreference nodes. We assign voltages to the three nodes as shown in Fig. 3.5(b) and label the currents.



**Figure 3.5** For Example 3.2: (a) original circuit, (b) circuit for analysis.

At node 1,

$$3 = i_1 + i_x \implies 3 = \frac{v_1 - v_3}{4} + \frac{v_1 - v_2}{2}$$

Multiplying by 4 and rearranging terms, we get

$$3v_1 - 2v_2 - v_3 = 12 \tag{3.2.1}$$

At node 2,

$$i_x = i_2 + i_3 \implies \frac{v_1 - v_2}{2} = \frac{v_2 - v_3}{8} + \frac{v_2 - 0}{4}$$

Multiplying by 8 and rearranging terms, we get

$$-4v_1 + 7v_2 - v_3 = 0 \tag{3.2.2}$$

At node 3,

$$i_1 + i_2 = 2i_x \implies \frac{v_1 - v_3}{4} + \frac{v_2 - v_3}{8} = \frac{2(v_1 - v_2)}{2}$$

Multiplying by 8, rearranging terms, and dividing by 3, we get

$$2v_1 - 3v_2 + v_3 = 0 \tag{3.2.3}$$

We have three simultaneous equations to solve to get the node voltages  $v_1$ ,  $v_2$ , and  $v_3$ . We shall solve the equations in three ways.

**METHOD 1** Using the elimination technique, we add Eqs. (3.2.1) and (3.2.3).

$$5v_1 - 5v_2 = 12$$

or

$$v_1 - v_2 = \frac{12}{5} = 2.4 \tag{3.2.4}$$

Adding Eqs. (3.2.2) and (3.2.3) gives

$$-2v_1 + 4v_2 = 0 \quad \Rightarrow \quad v_1 = 2v_2 \tag{3.2.5}$$

Substituting Eq. (3.2.5) into Eq. (3.2.4) yields

$$2v_2 - v_2 = 2.4 \implies v_2 = 2.4, v_1 = 2v_2 = 4.8 \text{ V}$$

From Eq. (3.2.3), we get

$$v_3 = 3v_2 - 2v_1 = 3v_2 - 4v_2 = -v_2 = -2.4$$
 V

Thus,

$$v_1 = 4.8 \text{ V}, \quad v_2 = 2.4 \text{ V}, \quad v_3 = -2.4 \text{ V}$$

**METHOD 2** To use Cramer's rule, we put Eqs. (3.2.1) to (3.2.3) in matrix form.

$$\begin{bmatrix} 3 & -2 & -1 \\ -4 & 7 & -1 \\ 2 & -3 & 1 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \end{bmatrix} = \begin{bmatrix} 12 \\ 0 \\ 0 \end{bmatrix}$$
(3.2.6)

From this, we obtain

$$v_1 = \frac{\Delta_1}{\Delta}, \qquad v_2 = \frac{\Delta_2}{\Delta}, \qquad v_3 = \frac{\Delta_3}{\Delta}$$

where  $\Delta$ ,  $\Delta_1$ ,  $\Delta_2$ , and  $\Delta_3$  are the determinants to be calculated as follows. As explained in Appendix A, to calculate the determinant of a 3 by 3 matrix, we repeat the first two rows and cross multiply.

$$\Delta = \begin{vmatrix} 3 & -2 & -1 \\ -4 & 7 & -1 \\ 2 & -3 & 1 \end{vmatrix} = \begin{vmatrix} 3 & -2 & -1 \\ -4 & 7 & -1 \\ -4 & 7 & -1 \\ -4 & 7 & -1 \\ + \end{vmatrix}$$

$$= 21 - 12 + 4 + 14 - 9 - 8 = 10$$

Similarly, we obtain

Thus, we find

$$v_1 = \frac{\Delta_1}{\Delta} = \frac{48}{10} = 4.8 \text{ V}, \qquad v_2 = \frac{\Delta_2}{\Delta} = \frac{24}{10} = 2.4 \text{ V}$$
  
 $v_3 = \frac{\Delta_3}{\Delta} = \frac{-24}{10} = -2.4 \text{ V}$ 

as we obtained with Method 1.

**METHOD 3** We now use *MATLAB* to solve the matrix. Equation (3.2.6) can be written as

$$AV = B \implies V = A^{-1}B$$

where A is the 3 by 3 square matrix, B is the column vector, and V is a column vector comprised of  $v_1$ ,  $v_2$ , and  $v_3$  that we want to determine. We use MATLAB to determine V as follows:

$$>>A = \begin{bmatrix} 3 & -2 & -1; & -4 & 7 & -1; & 2 & -3 & 1 \end{bmatrix};$$
  
$$>>B = \begin{bmatrix} 12 & 0 & 0 \end{bmatrix}';$$
  
$$>>V = inv(A) * B$$
  
$$= \begin{bmatrix} 4.8000 \\ V = & 2.4000 \\ -2.4000 \end{bmatrix}$$

Thus,  $v_1 = 4.8$  V,  $v_2 = 2.4$  V, and  $v_3 = -2.4$  V, as obtained previously.

Practice Problem 3.2 Fig. 3.6. 2Ω  $\Lambda \Lambda \Lambda$  $4i_{x}$  $3 \Omega$ 2 3 ۸۸۸۸,  $i_x$ Ş 4 A ( 4Ω 6Ω 3.3 \_

Figure 3.6 For Practice Prob. 3.2.

Find the voltages at the three nonreference nodes in the circuit of

**Answer:**  $v_1 = 32 \text{ V}, v_2 = -25.6 \text{ V}, v_3 = 62.4 \text{ V}.$ 

## Nodal Analysis with Voltage Sources

We now consider how voltage sources affect nodal analysis. We use the circuit in Fig. 3.7 for illustration. Consider the following two possibilities.

**CASE 1** If a voltage source is connected between the reference node and a nonreference node, we simply set the voltage at the nonreference node equal to the voltage of the voltage source. In Fig. 3.7, for example,

$$v_1 = 10 \text{ V}$$
 (3.10)

Thus, our analysis is somewhat simplified by this knowledge of the voltage at this node.

**CASE 2** If the voltage source (dependent or independent) is connected between two nonreference nodes, the two nonreference nodes