Solution. When the emitter circuit is open [See Fig. 8.23 (*i*)], the collector-base junction is reverse biased. A small leakage current I_{CBO} flows due to minority carriers.

$\therefore \quad I_{CBO} = 0.2\ \mu A$ *...given*

When base is open [See Fig. 8.23 (*ii*)], a small leakage current I_{CEO} flows due to minority carriers.

$\therefore \quad I_{CEO} = 20\ \mu A$ *. . . given*

We know $I_{CEO} = \dfrac{I_{CBO}}{1-\alpha}$

or $20 = \dfrac{0.2}{1-\alpha}$

$\therefore \quad \alpha = \mathbf{0.99}$

Now $I_C = \alpha I_E + I_{CBO}$

Here $I_C = 1\text{mA} = 1000\ \mu\text{A}\ ;\ \alpha = 0.99\ ;\ I_{CBO} = 0.2\ \mu\text{A}$

$\therefore \quad 1000 = 0.99 \times I_E + 0.2$

or $I_E = \dfrac{1000 - 0.2}{0.99} = \mathbf{1010\ \mu A}$

and $I_B = I_E - I_C = 1010 - 1000 = \mathbf{10\ \mu A}$

Example 8.14. *The collector leakage current in a transistor is 300 μA in CE arrangement. If now the transistor is connected in CB arrangement, what will be the leakage current? Given that β = 120.*

Solution. $I_{CEO} = 300\ \mu\text{A}$

$\beta = 120\ ;\ \alpha = \dfrac{\beta}{\beta+1} = \dfrac{120}{120+1} = 0.992$

Now, $I_{CEO} = \dfrac{I_{CBO}}{1-\alpha}$

$\therefore \quad I_{CBO} = (1-\alpha)\, I_{CEO} = (1 - 0.992) \times 300 = \mathbf{2.4\ \mu A}$

Note that leakage current in *CE* arrangement (*i.e.* I_{CEO}) is much more than in *CB* arrangement (*i.e.* I_{CBO}).

Example 8.15. *For a certain transistor, I_B = 20 μA; I_C = 2 mA and β = 80. Calculate I_{CBO}.*

Solution.

$I_C = \beta I_B + I_{CEO}$

or $2 = 80 \times 0.02 + I_{CEO}$

$\therefore \quad I_{CEO} = 2 - 80 \times 0.02 = 0.4\ \text{mA}$

Now $\alpha = \dfrac{\beta}{\beta+1} = \dfrac{80}{80+1} = 0.988$

$\therefore \quad I_{CBO} = (1-\alpha)\, I_{CEO} = (1 - 0.988) \times 0.4 = \mathbf{0.0048\ mA}$

Example 8.16. *Using diagrams, explain the correctness of the relation $I_{CEO} = (\beta + 1)\, I_{CBO}$.*

Solution. The leakage current I_{CBO} is the current that flows through the base-collector junction when emitter is open as shown is Fig. 8.24. When the transistor is in *CE* arrangement, the *base current (*i.e.* I_{CBO}) is multiplied by β in the collector as shown in Fig. 8.25.

$\therefore \quad I_{CEO} = I_{CBO} + \beta I_{CBO} = (\beta + 1)\, I_{CBO}$

* The current I_{CBO} is amplified because it is forced to flow across the base-emitter junction.

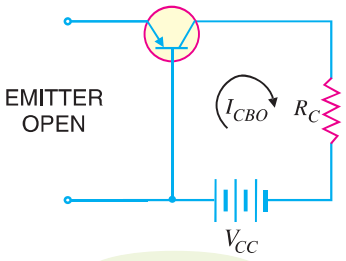


Fig. 8.24

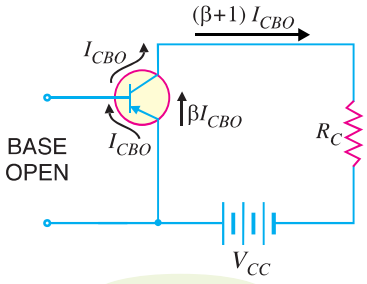


Fig. 8.25

Example 8.17 *Determine V_{CB} in the transistor * circuit shown in Fig. 8.26 (i). The transistor is of silicon and has $\beta = 150$.*

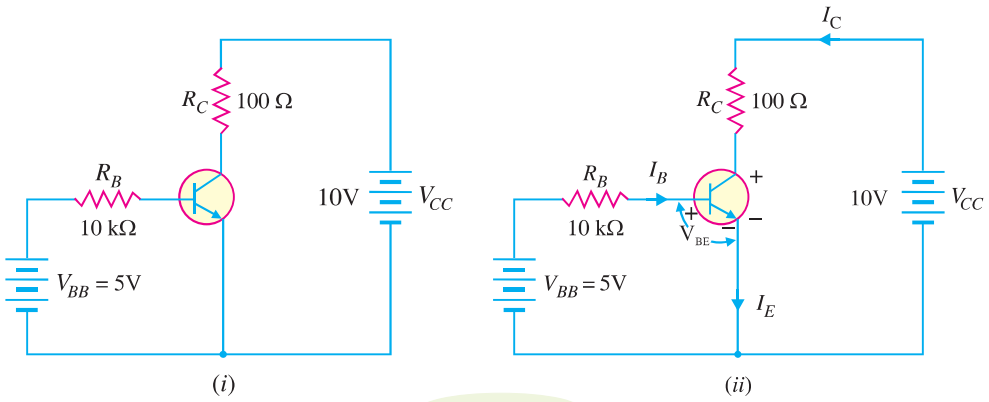


Fig. 8.26

Solution. Fig. 8.26 (*i*) shows the transistor circuit while Fig. 8.26 (*ii*) shows the various currents and voltages along with polarities.

Applying Kirchhoff's voltage law to base-emitter loop, we have,

$$V_{BB} - I_B R_B - V_{BE} = 0$$

or $$I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{5V - 0.7V}{10\ k\Omega} = 430\ \mu A$$

$\therefore$ $$I_C = \beta I_B = (150)(430\ \mu A) = 64.5\ mA$$

Now $$V_{CE} = V_{CC} - I_C R_C$$

$$= 10V - (64.5\ mA)\ (100\Omega) = 10V - 6.45V = 3.55V$$

We know that : $$V_{CE} = V_{CB} + V_{BE}$$

$\therefore$ $$V_{CB} = V_{CE} - V_{BE} = 3.55 - 0.7 = \mathbf{2.85V}$$

Example 8.18. *In a transistor, $I_B = 68\ \mu A$, $I_E = 30\ mA$ and $\beta = 440$. Determine the α rating of the transistor. Then determine the value of I_C using both the α rating and β rating of the transistor.*

Solution.

$$\alpha = \frac{\beta}{\beta + 1} = \frac{440}{440 + 1} = \mathbf{0.9977}$$

* The resistor R_B controls the base current I_B and hence collector current I_C ($= \beta I_B$). If R_B is increased, the base current (I_B) decreases and hence collector current (I_C) will decrease and vice-versa.

$$I_C = \alpha I_E = (0.9977)\ (30\ \text{mA}) = \mathbf{29.93\ mA}$$

Also $$I_C = \beta I_B = (440)\ (68\ \mu\text{A}) = \mathbf{29.93\ mA}$$

Example 8.19. *A transistor has the following ratings : $I_{C\,(max)}$ = 500 mA and β_{max} = 300. Determine the maximum allowable value of I_B for the device.*

Solution.

$$I_{B\,(max)} = \frac{I_{C\,(max)}}{\beta_{max}} = \frac{500\ \text{mA}}{300} = \mathbf{1.67\ mA}$$

For this transistor, if the base current is allowed to exceed 1.67 mA, the collector current will exceed its maximum rating of 500 mA and the transistor will probably be destroyed.

Example 8.20. *Fig. 8.27 shows the open circuit failures in a transistor. What will be the circuit behaviour in each case ?*

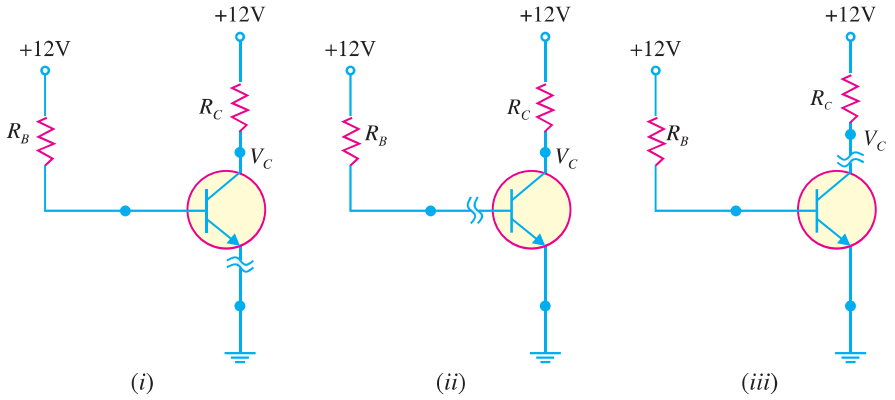


Fig. 8.27

Solution. *Fig 8.27 shows the open circuit failures in a transistor. We shall discuss the circuit behaviour in each case.

(*i*) Open emitter. Fig. 8.27 (*i*) shows an open emitter failure in a transistor. Since the collector diode is not forward biased, it is *OFF* and there can be neither collector current nor base current. Therefore, there will be no voltage drops across either resistor and the voltage at the base and at the collector leads of the transistor will be 12V.

(*ii*) Open-base. Fig. 8.27 (*ii*) shows an open base failure in a transistor. Since the base is open, there can be no base current so that the transistor is in *cut-off*. Therefore, all the transistor currents are 0A. In this case, the base and collector voltages will both be at 12V.

Note. It may be noted that an open failure at either the base or emitter will produce similar results.

(*iii*) Open collector. Fig. 8.27 (*iii*) shows an open collector failure in a transistor. In this case, the emitter diode is still *ON*, so we expect to see 0.7V at the base. However, we will see 12V at the collector because there is no collector current.

Example 8.21. *Fig. 8.28 shows the short circuit failures in a transistor. What will be the circuit behaviour in each case ?*

* The collector resistor R_C controls the collector voltage V_C ($= V_{CC} - I_C R_C$). When R_C increases, V_C decreases and vice-versa.

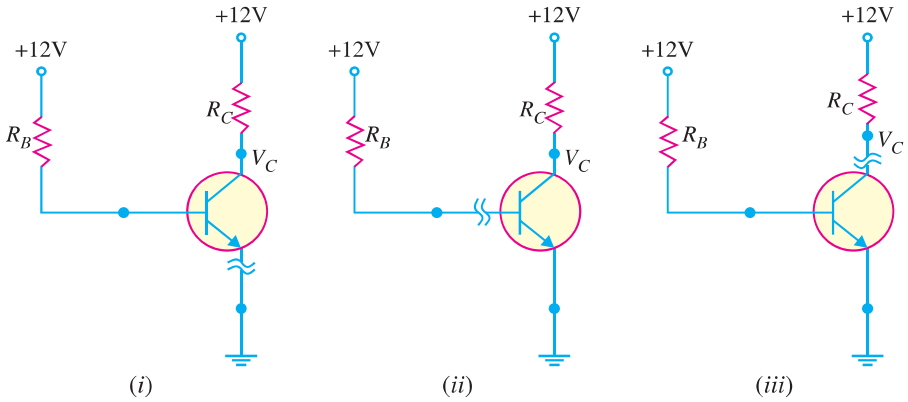


Fig. 8.28

Solution. Fig. 8.28 shows the short circuit failures in a transistor. We shall discuss the circuit behaviour in each case.

(*i*) Collector-emitter short. Fig. 8.28 (*i*) shows a short between collector and emitter. The emitter diode is still forward biased, so we expect to see 0.7V at the base. Since the collector is shorted to the emitter, $V_C = V_E = 0$V.

(*ii*) Base -emitter short. Fig 8.28 (*ii*) shows a short between base and emitter. Since the base is now directly connected to ground, $V_B = 0$. Therefore, the current through R_B will be diverted to ground and there is no current to forward bias the emitter diode. As a result, the transistor will be *cut-off* and there is no collector current. So we will expect the collector voltage to be 12V.

(*iii*) Collector-base short. Fig. 8.28 (*iii*) shows a short between the collector and the base. In this case, the emitter diode is still forward biased so $V_B = 0.7$V. Now, however, because the collector is shorted to the base, $V_C = V_B = 0.7$V.

Note. The collector-emitter short is probably the most common type of fault in a transistor. It is because the collector current (I_C) and collector-emitter voltage (V_{CE}) are responsible for the major part of the power dissipation in the transistor. As we shall see (See Art. 8.23), the power dissipation in a transistor is mainly due to I_C and V_{CE} (*i.e.* $P_D = V_{CE} I_C$). Therefore, the transistor chip between the collector and the emitter is most likely to melt first.

8.12 Characteristics of Common Emitter Connection

The important characteristics of this circuit arrangement are the *input characteristics* and *output characteristics*.

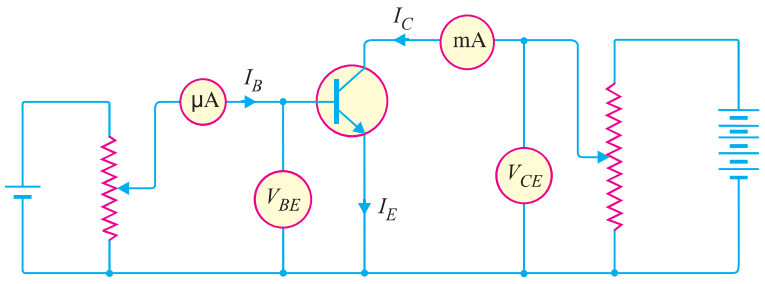


Fig. 8.29

1. Input characteristic. *It is the curve between base current I_B and base-emitter voltage V_{BE} at constant collector-emitter voltage V_{CE}.*

The input characteristics of a *CE* connection can be determined by the circuit shown in Fig. 8.29. Keeping V_{CE} constant (say at 10 V), note the base current I_B for various values of V_{BE}. Then plot the readings obtained on the graph, taking I_B along *y*-axis and V_{BE} along *x*-axis. This gives the input characteristic at V_{CE} = 10V as shown in Fig. 8.30. Following a similar procedure, a family of input characteristics can be drawn. The following points may be noted from the characteristics :

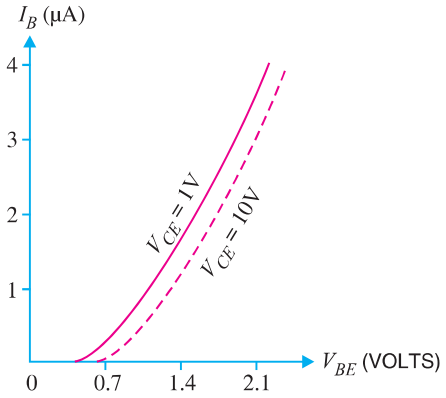


Fig. 8.30

(i) The characteristic resembles that of a forward biased diode curve. This is expected since the base-emitter section of transistor is a diode and it is forward biased.

(ii) As compared to *CB* arrangement, I_B increases less rapidly with V_{BE}. Therefore, input resistance of a *CE* circuit is higher than that of *CB* circuit.

Input resistance. It is the ratio of change in base-emitter voltage (ΔV_{BE}) to the change in base current (ΔI_B) at constant V_{CE} *i.e.*

$$\text{Input resistance,} \quad r_i = \frac{\Delta V_{BE}}{\Delta I_B} \quad \text{at constant } V_{CE}$$

The value of input resistance for a *CE* circuit is of the order of a few hundred ohms.

2. Output characteristic. *It is the curve between collector current I_C and collector-emitter voltage V_{CE} at constant base current I_B.*

The output characteristics of a *CE* circuit can be drawn with the help of the circuit shown in Fig. 8.29. Keeping the base current I_B fixed at some value say, 5 μA, note the collector current I_C for various values of V_{CE}. Then plot the readings on a graph, taking I_C along *y*-axis and V_{CE} along *x*-axis. This gives the output characteristic at I_B = 5 μA as shown in Fig. 8.31 (*i*). The test can be repeated for I_B = 10 μA to obtain the new output characteristic as shown in Fig. 8.31 (*ii*). Following similar procedure, a family of output characteristics can be drawn as shown in Fig. 8.31 (*iii*).

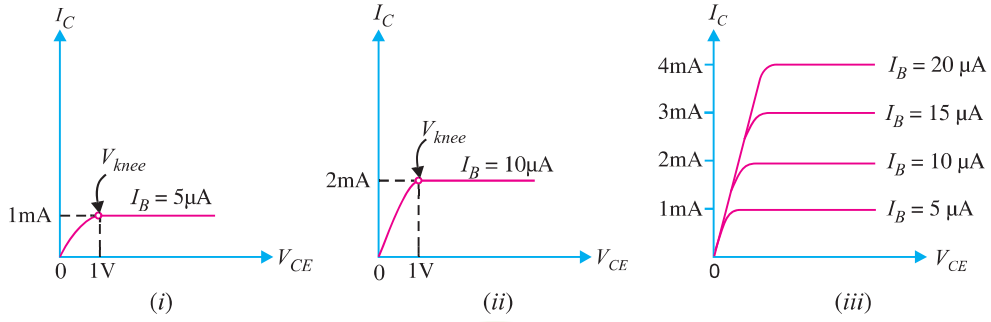


Fig. 8.31

The following points may be noted from the characteristics:

(i) The collector current I_C varies with V_{CE} for V_{CE} between 0 and 1V only. After this, collector current becomes *almost* constant and independent of V_{CE}. This value of V_{CE} upto which collector

current I_C changes with V_{CE} is called the *knee voltage* (V_{knee}). *The transistors are always operated in the region above knee voltage.*

(ii) Above knee voltage, I_C is almost constant. However, a small increase in I_C with increasing V_{CE} is caused by the collector depletion layer getting wider and capturing a few more majority carriers before electron-hole combinations occur in the base area.

(iii) For any value of V_{CE} above knee voltage, the collector current I_C is approximately equal to $\beta \times I_B$.

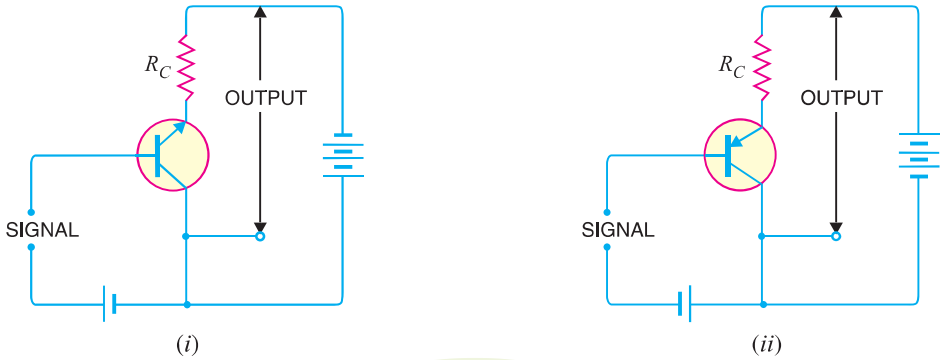
Output resistance. It is the ratio of change in collector-emitter voltage (ΔV_{CE}) to the change in collector current (ΔI_C) at constant I_B *i.e.*

$$\text{Output resistance, } r_o = \frac{\Delta V_{CE}}{\Delta I_C} \text{ at constant } I_B$$

It may be noted that whereas the output characteristics of *CB* circuit are horizontal, they have noticeable slope for the *CE* circuit. Therefore, the output resistance of a *CE* circuit is less than that of *CB* circuit. Its value is of the order of 50 kΩ.

8.13 Common Collector Connection

In this circuit arrangement, input is applied between base and collector while output is taken between the emitter and collector. Here, collector of the transistor is common to both input and output circuits and hence the name common collector connection. Fig. 8.32 (*i*) shows common collector *npn* transistor circuit whereas Fig. 8.32 (*ii*) shows common collector *pnp* circuit.



(*i*) (*ii*)

Fig. 8.32

***(i)* Current amplification factor γ.** In common collector circuit, input current is the base current I_B and output current is the emitter current I_E. Therefore, current amplification in this circuit arrangement can be defined as under :

The ratio of change in emitter current (ΔI_E) to the change in base current (ΔI_B) is known as **current amplification factor** *in common collector (CC) arrangement i.e.*

$$\gamma = \frac{\Delta I_E}{\Delta I_B}$$

This circuit provides about the same current gain as the common emitter circuit as $\Delta I_E \simeq \Delta I_C$. However, its voltage gain is always less than 1.

Relation between γ and α

$$\gamma = \frac{\Delta I_E}{\Delta I_B} \qquad ...(i)$$

$$\alpha = \frac{\Delta I_C}{\Delta I_E} \qquad ...(ii)$$

Now $I_E = I_B + I_C$

or $\Delta I_E = \Delta I_B + \Delta I_C$

or $\Delta I_B = \Delta I_E - \Delta I_C$

Substituting the value of ΔI_B in exp. (*i*), we get,

$$\gamma = \frac{\Delta I_E}{\Delta I_E - \Delta I_C}$$

Dividing the numerator and denominator of R.H.S. by ΔI_E, we get,

$$\gamma = \frac{\frac{\Delta I_E}{\Delta I_E}}{\frac{\Delta I_E}{\Delta I_E} - \frac{\Delta I_C}{\Delta I_E}} = \frac{1}{1-\alpha} \qquad \left(\text{Q } \alpha = \frac{\Delta I_C}{\Delta I_E}\right)$$

$$\therefore \quad \gamma = \frac{1}{1-\alpha}$$

(*ii*) Expression for collector current

We know $I_C = \alpha I_E + I_{CBO}$ (See Art. 8.8)

Also $I_E = I_B + I_C = I_B + (\alpha I_E + I_{CBO})$

$\therefore \quad I_E (1 - \alpha) = I_B + I_{CBO}$

or $I_E = \frac{I_B}{1-\alpha} + \frac{I_{CBO}}{1-\alpha}$

or $I_C \; ; \; I_E = *(\beta + 1) I_B + (\beta + 1) I_{CBO}$

(*iii*) Applications. The common collector circuit has very high input resistance (about 750 kΩ) and very low output resistance (about 25 Ω). Due to this reason, the voltage gain provided by this circuit is always less than 1. Therefore, this circuit arrangement is seldom used for amplification. However, due to relatively high input resistance and low output resistance, this circuit is primarily used for impedance matching *i.e.* for driving a low impedance load from a high impedance source.

8.14 Comparison of Transistor Connections

The comparison of various characteristics of the three connections is given below in the tabular form.

S. No.	Characteristic	Common base	Common emitter	Common collector
1.	Input resistance	Low (about 100 Ω)	Low (about 750 Ω)	Very high (about 750 kΩ)
2.	Output resistance	Very high (about 450 kΩ)	High (about 45 kΩ)	Low (about 50 Ω)
3.	Voltage gain	about 150	about 500	less than 1
4.	Applications	For high frequency applications	For audio frequency applications	For impedance matching
5.	Current gain	No (less than 1)	High (β)	Appreciable

The following points are worth noting about transistor arrangements :

* $\beta = \frac{\alpha}{1-\alpha} \quad \therefore \quad \beta + 1 = \frac{\alpha}{1-\alpha} + 1 = \frac{1}{1-\alpha}$

(*i*) CB Circuit. The input resistance (r_i) of *CB* circuit is low because I_E is high. The output resistance (r_o) is high because of reverse voltage at the collector. It has no current gain ($\alpha < 1$) but voltage gain can be high. The *CB* circuit is seldom used. The only advantage of *CB* circuit is that it provides good stability against increase in temperature.

(*ii*) CE Circuit. The input resistance (r_i) of a *CE* circuit is high because of small I_B. Therefore, r_i for a *CE* circuit is much higher than that of *CB* circuit. The output resistance (r_o) of *CE* circuit is smaller than that of *CB* circuit. The current gain of *CE* circuit is large because I_C is much larger than I_B. The voltage gain of *CE* circuit is larger than that of *CB* circuit. The *CE* circuit is generally used because it has the best combination of voltage gain and current gain. The disadvantage of *CE* circuit is that the leakage current is amplified in the circuit, but bias stabilisation methods can be used.

(*iii*) CC Circuit. The input resistance (r_i) and output resistance (r_o) of *CC* circuit are respectively high and low as compared to other circuits. There is no voltage gain ($A_v < 1$) in a *CC* circuit. This circuit is often used for impedance matching.

8.15 Commonly Used Transistor Connection

Out of the three transistor connections, the common emitter circuit is the most efficient. It is used in about 90 to 95 per cent of all transistor applications. The main reasons for the widespread use of this circuit arrangement are :

(*i*) High current gain. In a common emitter connection, I_C is the output current and I_B is the input current. In this circuit arrangement, collector current is given by :

$$I_C = \beta I_B + I_{CEO}$$

As the value of β is very large, therefore, the output current I_C is much more than the input current I_B. Hence, the current gain in *CE* arrangement is very high. It may range from 20 to 500.

(*ii*) High voltage and power gain. Due to high current gain, the common emitter circuit has the highest voltage and power gain of three transistor connections. This is the major reason for using the transistor in this circuit arrangement.

(*iii*) Moderate output to input impedance ratio. In a common emitter circuit, the ratio of output impedance to input impedance is small (about 50). This makes this circuit arrangement an ideal one for coupling between various transistor stages. However, in other connections, the ratio of output impedance to input impedance is very large and hence coupling becomes highly inefficient due to gross mismatching.

8.16 Transistor as an Amplifier in *CE* Arrangement

Fig. 8.33 shows the common emitter *npn* amplifier circuit. Note that a battery V_{BB} is connected in the input circuit in addition to the signal voltage. This d.c. voltage is known as *bias voltage* and its magnitude is such that it always keeps the emitter-base junction forward *biased regardless of the polarity of the signal source.

Operation. During the positive half-cycle of the **signal, the forward bias across the emitter-base junction is increased. Therefore, more electrons flow from the emitter to the collector *via* the base. This causes an increase in collector current. The increased collector current produces a greater voltage drop across the collector load resistance R_C. However, during the negative half-cycle of the

* If d.c. bias voltage is not provided, then during negative half-cycle of the signal, the emitter-base junction will be reverse biased. This will upset the transistor action.

** Throughout the book, we shall use sine wave signals because these are convenient for testing amplifiers. But it must be realised that signals (*e.g.* speech, music etc.) with which we work are generally complex having little resemblance to a sine wave. However, fourier series analysis tells us that such complex signals may be expressed as a sum of sine waves of various frequencies.

signal, the forward bias across emitter-base junction is decreased. Therefore, collector current decreases. This results in the decreased output voltage (in the opposite direction). Hence, an amplified output is obtained across the load.

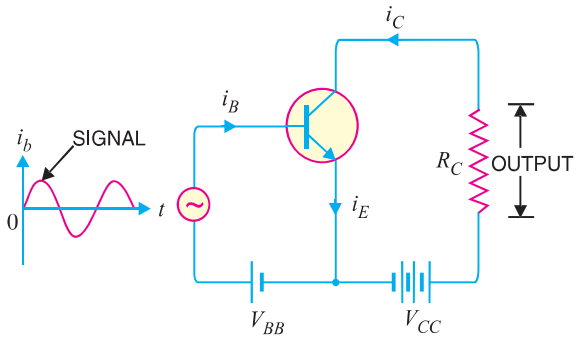


Fig. 8.33

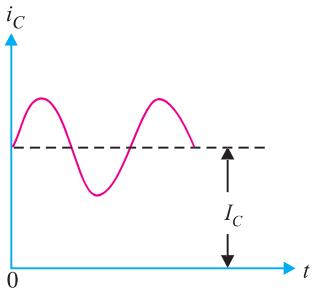


Fig. 8.34

Analysis of collector currents. When no signal is applied, the input circuit is forward biased by the battery V_{BB}. Therefore, a d.c. collector current I_C flows in the collector circuit. This is called *zero signal collector current*. When the signal voltage is applied, the forward bias on the emitter-base junction increases or decreases depending upon whether the signal is positive or negative. During the positive half-cycle of the signal, the forward bias on emitter-base junction is increased, causing total collector current i_C to increase. Reverse will happen for the negative half-cycle of the signal.

Fig. 8.34 shows the graph of total collector current i_C versus time. From the graph, it is clear that total collector current consists of two components, namely ;

(i) The d.c. collector current I_C (zero signal collector current) due to bias battery V_{BB}. This is the current that flows in the collector in the absence of signal.

(ii) The a.c. collector current i_c due to signal.

$\therefore$ Total collector current, $i_C = i_c + I_C$

The useful output is the voltage drop across collector load R_C due to the a.c. component i_c. The purpose of zero signal collector current is to ensure that the emitter-base junction is forward biased at all times. The table below gives the symbols usually employed for currents and voltages in transistor applications.

S. No.	Particular	Instantaneous a.c.	d.c.	Total
1.	Emitter current	i_e	I_E	i_E
2.	Collector current	i_c	I_C	i_C
3.	Base current	i_b	I_B	i_B
4.	Collector-emitter voltage	v_{ce}	V_{CE}	v_{CE}
5.	Emitter-base voltage	v_{eb}	V_{EB}	v_{EB}

8.17 Transistor Load Line Analysis

In the transistor circuit analysis, it is generally required to determine the collector current for various collector-emitter voltages. One of the methods can be used to plot the output characteristics and determine the collector current at any desired collector-emitter voltage. However, a more convenient method, known as *load line method* can be used to solve such problems. As explained later in this section, this method is quite easy and is frequently used in the analysis of transistor applications.

d.c. load line. Consider a common emitter *npn* transistor circuit shown in Fig. 8.35 (*i*) where no signal is applied. Therefore, d.c. conditions prevail in the circuit. The output characteristics of this circuit are shown in Fig. 8.35 (*ii*).

The value of collector-emitter voltage V_{CE} at any time is given by ;

$$V_{CE} = V_{CC} - I_C R_C \qquad ...(i)$$

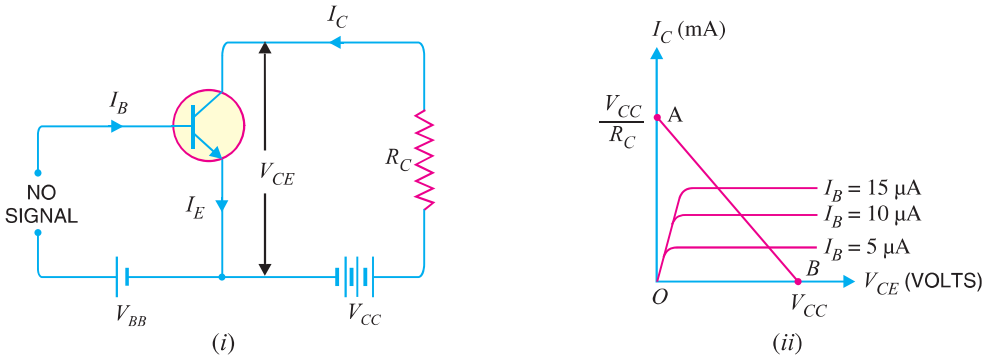


Fig. 8.35

As V_{CC} and R_C are fixed values, therefore, it is a first degree equation and can be represented by a straight line on the output characteristics. This is known as *d.c. load line* and determines the locus of $V_{CE} - I_C$ points for any given value of R_C. To add load line, we need two end points of the straight line. These two points can be located as under :

(*i*) When the collector current $I_C = 0$, then collector-emitter voltage is maximum and is equal to V_{CC} *i.e.*

$$\text{Max. } V_{CE} = V_{CC} - I_C R_C$$
$$= V_{CC} \qquad (\because I_C = 0)$$

This gives the first point B ($OB = V_{CC}$) on the collector-emitter voltage axis as shown in Fig. 8.35 (*ii*).

(*ii*) When collector-emitter voltage $V_{CE} = 0$, the collector current is maximum and is equal to V_{CC}/R_C *i.e.*

$$V_{CE} = V_{CC} - I_C R_C$$

or $$0 = V_{CC} - I_C R_C$$

$\therefore$ $$\text{Max. } I_C = V_{CC}/R_C$$

This gives the second point A ($OA = V_{CC}/R_C$) on the collector current axis as shown in Fig. 8.35 (*ii*). By joining these two points, d.c. *load line AB is constructed.

Importance. The current (I_C) and voltage (V_{CE}) conditions in the transistor circuit are represented by some point on the output characteristics. The same information can be obtained from the load line. Thus when I_C is maximum ($= V_{CC}/R_C$), then $V_{CE} = 0$ as shown in Fig. 8.36. If $I_C = 0$, then V_{CE} is maximum

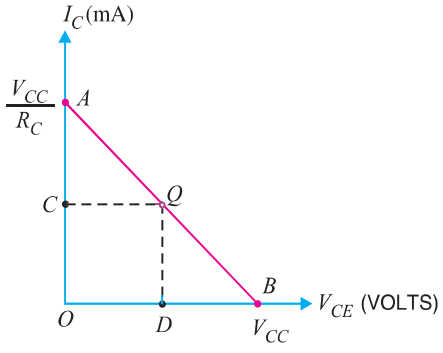


Fig. 8.36

* **Why load line ?** The resistance R_C connected to the device is called load or load resistance for the circuit and, therefore, the line we have just constructed is called the load line.

and is equal to V_{CC}. For any other value of collector current say OC, the collector-emitter voltage $V_{CE} = OD$. It follows, therefore, that load line gives a far more convenient and direct solution to the problem.

Note. If we plot the load line on the output characteristic of the transistor, we can investigate the behaviour of the transistor amplifier. It is because we have the transistor output current and voltage specified in the form of load line equation and the transistor behaviour itself specified implicitly by the output characteristics.

8.18 Operating Point

The zero signal values of I_C and V_{CE} are known as the **operating point**.

It is called operating point because the variations of I_C and V_{CE} take place about this point when signal is applied. It is also called quiescent (silent) point or *Q-point* because it is the point on $I_C - V_{CE}$ characteristic when the transistor is silent *i.e.* in the absence of the signal.

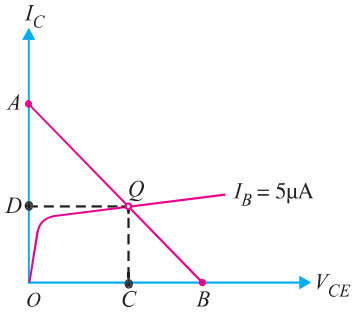


Fig. 8.37

Suppose in the absence of signal, the base current is 5 μA. Then I_C and V_{CE} conditions in the circuit must be represented by some point on $I_B = 5$ μA characteristic. But I_C and V_{CE} conditions in the circuit should also be represented by some point on the d.c. load line AB. The point Q where the load line and the characteristic intersect is the only point which satisfies both these conditions. Therefore, the point Q describes the actual state of affairs in the circuit in the zero signal conditions and is called the operating point. Referring to Fig. 8.37, for $I_B = 5$ μA, the zero signal values are :

$$V_{CE} = OC \text{ volts}$$
$$I_C = OD \text{ mA}$$

It follows, therefore, that the zero signal values of I_C and V_{CE} (*i.e.* operating point) are determined by the point where d.c. load line intersects the proper base current curve.

Example 8.22. *For the circuit shown in Fig. 8.38 (i), draw the d.c. load line.*

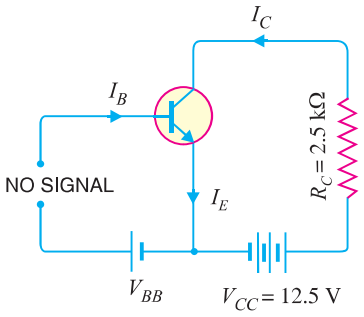
Solution. The collector-emitter voltage V_{CE} is given by ;

$$V_{CE} = V_{CC} - I_C R_C \quad ...(i)$$

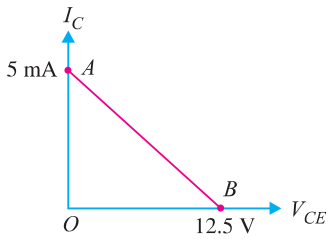
When $I_C = 0$, then,

$$V_{CE} = V_{CC} = 12.5 \text{ V}$$

This locates the point B of the load line on the collector-emitter voltage axis.



(*i*)



(*ii*)

Fig. 8.38